PHILIPS

Data handbook

Electronic components and materials

Integrated circuits

Book IC12 1988

I^2C-bus compatible ICs

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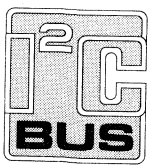
I²C-BUS COMPATIBLE ICs



SELECTION GUIDE

FUNCTIONAL INDEX

Operating temperature range: 0 to 70 °C.
Extended temperature range: –40 to + 85 °C.
Automotive temperature range: –40 to + 110 °C.

Operating temperature range: 0 to 70 °C.
Extended temperature range: −40 to + 85 °C.
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NUMERICAL INDEX

(MICROCONTROLLERS)

Operating temperature range: 0 to 70 °C.
Extended temperature range: −40 to + 85 °C.
Automotive temperature range: −40 to + 110 °C.

type number	description			package code	page
SINGLE-CHIP 8-BIT MICROCONTROLLERS (continued)					
	RAM	ROM			
MAF8442P	128	4K	plus 8-bit LED driver; extended temperature	DIL-20; SOT-146	61
MAF84A42P	128	4K	plus 8-bit LED driver; automotive temperature; reduced frequency	DIL-20; SOT-146	61
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PCB80C552WP	256	—	ROM-less version of PCB83C552	68-PLCC; SOT-188	81
PCB80C652WP	256	—	ROM-less version of PCB83C652	44-PLCC; SOT-187	129
PCB83C552WP	256	8K	PCB80C51 plus additional functions	68-PLCC; SOT-188	81
PCB83C652WP	256	8K	PCB80C51 plus additional functions	44-PLCC; SOT-187	129
PCD3315CP	160	1,2K	telephony microcontroller	DIL-28; SOT-117	167
PCD3315CT	160	1,2K	telephony microcontroller	SO-28; SOT-136A	167
PCD3343D	224	3K	telephony microcontroller	DIL-28; SOT-135A	171
PCD3343P	224	3K	telephony microcontroller	DIL-28; SOT-117	171
PCD3343T	224	3K	telephony microcontroller	SO-28; SOT-136A	171
PCF84C00B	256	—	bond-out version PCF84CXX family	28/28 Piggy-back	211
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PCF84C21P	64	2K	plus 8-bit LED driver; extended temperature	DIL-28; SOT-117	211
PCF84C21T	64	2K	plus 8-bit LED driver; extended temperature	SO-28; SOT-136A	211
PCF84C41P	128	4K	plus 8-bit LED driver; extended temperature	DIL-28; SOT-117	211
PCF84C41T	128	4K	plus 8-bit LED driver; extended temperature	SO-28; SOT-136A	211
PCF84C81P	256	8K	plus 8-bit LED driver; extended temperature	DIL-28; SOT-117	211
PCF84C81T	256	8K	plus 8-bit LED driver; extended temperature	SO-28; SOT-136A	211
SCC68070	68000 CPU; MMU; UART; DMA; timer				303

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NUMERICAL INDEX

(EXCLUDING MICROCONTROLLERS)

FORTHCOMING NEW PRODUCTS

The types listed below are not included in this handbook. Information will be available at a later date.

PCF8580	256 x 8-bit static RAM
PCF8581	256 x 8-bit static RAM
PCF8584	8-bit parallel bus to I^2C bus-protocol converter
PCF84C64	256 RAM, 6 K ROM plus display on screen; 4 x 6-bit DAC; 14-bit DAC and 3-bit ADC
PCF84C430	8-bit microcontroller; 128 RAM, 4 K ROM plus LCD driver
SAA4700; T	dataline 16 decoder
SAA9055	digital SECAM decoder
SAA9062	digital deflection processor ($1f_H$; $1f_V$)
SAA9063	digital deflection processor ($2f_H$; $1f_V$)
SAA9064	digital deflection processor ($2f_H$; $2f_V$)
TDA8425	stereo volume control circuit with spatial and pseudo-stereo sound
TDA8432	analogue deflection processor and sync control
TDA8461	PAL/NTSC colour decoder and RGB processor

GENERAL

Type designation

Rating systems

Handling MOS devices

PRO ELECTRON TYPE DESIGNATION CODE FOR INTEGRATED CIRCUITS

This type nomenclature applies to semiconductor monolithic, semiconductor multi-chip, thin-film, thick-film and hybrid integrated circuits.

A basic number consists of:

THREE LETTERS FOLLOWED BY A SERIAL NUMBER

FIRST AND SECOND LETTER

1. DIGITAL FAMILY CIRCUITS

   The FIRST TWO LETTERS identify the FAMILY (see note 1).

2. SOLITARY CIRCUITS

   The FIRST LETTER divides the solitary circuits into:

   S : Solitary digital circuits
   T : Analogue circuits
   U : Mixed analogue/digital circuits

   The SECOND LETTER is a serial letter without any further significance except 'H' which stands for hybrid circuits.

3. MICROPROCESSORS

   The FIRST TWO LETTERS identify microprocessors and correlated circuits as follows:

   MA : { Microcomputer / Central processing unit }
   MB : Slice processor (see note 2)
   MD : Correlated memories
   ME : Other correlated circuits (interface, clock, peripheral controller, etc.)

4. CHARGE-TRANSFER DEVICES AND SWITCHED CAPACITORS

   The FIRST TWO LETTERS identify the following:

   NH : Hybrid circuits
   NL : Logic circuits
   NM : Memories
   NS : Analogue signal processing, using switched capacitors
   NT : Analogue signal processing, using CTDs
   NX : Imaging devices
   NY : Other correlated circuits

Notes

1. A logic family is an assembly of digital circuits designed to be interconnected and defined by its basic electrical characteristics (such as: supply voltage, power consumption, propagation delay, noise immunity).
2. By 'slice processor' is meant: a functional slice of microprocessor.

THIRD LETTER

It indicates the operating ambient temperature range.
The letters A to G give information about the temperature:

A : temperature range not specified
B : 0 to + 70 °C
C : −55 to + 125 °C
D : −25 to + 70 °C
E : −25 to + 85 °C
F : −40 to + 85 °C
G : −55 to + 85 °C

If a circuit is published for another temperature range, the letter indicating a narrower temperature range may be used or the letter 'A'.

Example: the range 0 to + 75 °C can be indicated by 'B' or 'A'.

SERIAL NUMBER

This may be either a 4-digit number assigned by Pro Electron, or the serial number (which may be a combination of figures and letters) of an existing company type designation of the manufacturer.

To the basic type number may be added:

A VERSION LETTER

Indicates a minor variant of the basic type or the package. Except for 'Z', which means customized wiring, the letter has no fixed meaning. The following letters are recommended for package variants:

C : for cylindrical
D : for ceramic DIL
F : for flat pack
L : for chip on tape
P : for plastic DIL
Q : for QIL
T : for miniature plastic (mini-pack)
U : for uncased chip

Alternatively a TWO LETTER SUFFIX may be used instead of a single package version letter, if the manufacturer (sponsor) wishes to give more information.

FIRST LETTER: General shape

C : Cylindrical
D : Dual-in-line (DIL)
E : Power DIL (with external heatsink)
F : Flat (leads on 2 sides)
G : Flat (leads on 4 sides)
K : Diamond (TO-3 family)
M : Multiple-in-line (except Dual-, Triple-, Quadruple-in-line)
Q : Quadruple-in-line (QIL)
R : Power QIL (with external heatsink)
S : Single-in-line
T : Triple-in-line

SECOND LETTER: Material

C : Metal-ceramic
G : Glass-ceramic (cerdip)
M : Metal
P : Plastic

A hyphen precedes the suffix to avoid confusion with a version letter.

RATING SYSTEMS

The rating systems described are those recommended by the International Electrotechnical Commission (IEC) in its Publication 134.

DEFINITIONS OF TERMS USED

Electronic device. An electronic tube or valve, transistor or other semiconductor device.

Note
This definition excludes inductors, capacitors, resistors and similar components.

Characteristic. A characteristic is an inherent and measurable property of a device. Such a property may be electrical, mechanical, thermal, hydraulic, electro-magnetic, or nuclear, and can be expressed as a value for stated or recognized conditions. A characteristic may also be a set of related values, usually shown in graphical form.

Bogey electronic device. An electronic device whose characteristics have the published nominal values for the type. A bogey electronic device for any particular application can be obtained by considering only those characteristics which are directly related to the application.

Rating. A value which establishes either a limiting capability or a limiting condition for an electronic device. It is determined for specified values of environment and operation, and may be stated in any suitable terms.

Note
Limiting conditions may be either maxima or minima.

Rating system. The set of principles upon which ratings are established and which determine their interpretation.

Note
The rating system indicates the division of responsibility between the device manufacturer and the circuit designer, with the object of ensuring that the working conditions do not exceed the ratings.

ABSOLUTE MAXIMUM RATING SYSTEM

Absolute maximum ratings are limiting values of operating and environmental conditions applicable to any electronic device of a specified type as defined by its published data, which should not be exceeded under the worst probable conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device, taking no responsibility for equipment variations, environmental variations, and the effects of changes in operating conditions due to variations in the characteristics of the device under consideration and of all other electronic devices in the equipment.

The equipment manufacturer should design so that, initially and throughout life, no absolute maximum value for the intended service is exceeded with any device under the worst probable operating conditions with respect to supply voltage variation, equipment component variation, equipment control adjustment, load variations, signal variation, environmental conditions, and variations in characteristics of the device under consideration and of all other electronic devices in the equipment.

DESIGN MAXIMUM RATING SYSTEM

Design maximum ratings are limiting values of operating and environmental conditions applicable to a bogey electronic device of a specified type as defined by its published data, and should not be exceeded under the worst probable conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device, taking responsibility for the effects of changes in operating conditions due to variations in the characteristics of the electronic device under consideration.

The equipment manufacturer should design so that, initially and throughout life, no design maximum value for the intended service is exceeded with a bogey device under the worst probable operating conditions with respect to supply voltage variation, equipment component variation, variation in characteristics of all other devices in the equipment, equipment control adjustment, load variation, signal variation and environmental conditions.

DESIGN CENTRE RATING SYSTEM

Design centre ratings are limiting values of operating and environmental conditions applicable to a bogey electronic device of a specified type as defined by its published data, and should not be exceeded under normal conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device in average applications, taking responsibility for normal changes in operating conditions due to rated supply voltage variation, equipment component variation, equipment control adjustment, load variation, signal variation, environmental conditions, and variations in the characteristics of all electronic devices.

The equipment manufacturer should design so that, initially, no design centre value for the intended service is exceeded with a bogey electronic device in equipment operating at the stated normal supply voltage.

HANDLING MOS DEVICES

Though all our MOS integrated circuits incorporate protection against electrostatic discharges, they can nevertheless be damaged by accidental over-voltages. In storing and handling them, the following precautions are recommended.

Caution

Testing or handling and mounting call for special attention to personal safety. Personnel handling MOS devices should normally be connected to ground via a resistor.

Storage and transport

Store and transport the circuits in their original packing. Alternatively, use may be made of a conductive material or special IC carrier that either short-circuits all leads or insulates them from external contact.

Testing or handling

Work on a conductive surface (e.g. metal table top) when testing the circuits or transferring them from one carrier to another. Electrically connect the person doing the testing or handling to the conductive surface, for example by a metal bracelet and a conductive cord or chain. Connect all testing and handling equipment to the same surface.
Signals should not be applied to the inputs while the device power supply is off. All unused input leads should be connected to either the supply voltage or ground.

Mounting

Mount MOS integrated circuits on printed circuit boards *after* all other components have been mounted. Take care that the circuits themselves, metal parts of the board, mounting tools, and the person doing the mounting are kept at the same electric (ground) potential. If it is impossible to ground the printed-circuit board the person mounting the circuits should touch the board before bringing MOS circuits into contact with it.

Soldering

Soldering iron tips, including those of low-voltage irons, or soldering baths should also be kept at the same potential as the MOS circuits and the board.

Static charges

Dress personnel in clothing of non-electrostatic material (no wool, silk or synthetic fibres). After the MOS circuits have been mounted on the board proper handling precautions should still be observed. Until the sub-assemblies are inserted into a complete system in which the proper voltages are supplied, the board is no more than an extension of the leads of the devices mounted on the board. To prevent static charges from being transmitted through the board wiring to the device it is recommended that conductive clips or conductive tape be put on the circuit board terminals.

Transient voltages

To prevent permanent damage due to transient voltages, do not insert or remove MOS devices, or printed-circuit boards with MOS devices, from test sockets or systems with power on.

Voltage surges

Beware of voltage surges due to switching electrical equipment on or off, relays and D.C. lines.

DEVICE DATA

Microcontrollers

Excluding Microcontrollers

SINGLE-CHIP 8-BIT MICROCONTROLLER

DESCRIPTION

The MAB84X1 family of microcontrollers is fabricated in NMOS. The family consists of 5 devices:

- MAB8401 – 128 bytes RAM, external program memory, with 8-bit LED-driver (10mA), emulation of MAB/F8422/42* possible
- MAB/MAF8411 – 1K byte ROM/64 bytes RAM plus 8-bit LED-driver
- MAB/MAF8421 – 2K bytes ROM/64 bytes RAM plus 8-bit LED-driver
- MAB/MAF8441 – 4K bytes ROM/128 bytes RAM plus 8-bit LED-driver
- MAB/MAF8461 – 6K bytes ROM/128 bytes RAM plus 8-bit LED-driver

Each version has 20 quasi-bidirectional I/O port lines, one serial I/O line, one single-level vectored interrupt, an 8-bit timer/event counter and on-board clock oscillator and clock circuits. Two 20-pin versions, MAB/F8422 and MAB/F8442* are also available.

This microcontroller family is designed to be an efficient controller as well as an arithmetic processor. The instruction set is based on that of the MAB8048. The microcontrollers have extensive bit handling abilities and facilities for both binary and BCD arithmetic.

For detailed information see the "8-bit Single-chip Microcontrollers user manual".

* See data sheet on MAB/F8422/42.

Features

- 8-bit: CPU, ROM, RAM and I/O in a single 28-lead DIL package
- 1K, 2K, 4K or 6K ROM bytes plus a ROM-less version
- 64 or 128 RAM bytes
- 20 quasi-bidirectional I/O port lines
- Two testable inputs: one of which can be used to detect zero cross-over, the other is also the external interrupt input
- Single level vectored interrupts: external, timer/event counter, serial I/O
- Serial I/O that can be used in single or multi-master systems (serial I/O data via an existing port line and clock via a dedicated line)
- 8-bit programmable timer/event counter
- Internal oscillator, generated with inductor, crystal, ceramic resonator or external source
- Over 80 instructions (based on MAB8048) all of 1 or 2 cycles
- Single 5 V power supply (± 10%)
- Operating temperature ranges:

0 to + 70 °C	MAB84X1 family
−40 to + 85 °C	MAF84X1 family only
−40 to + 110 °C	MAF84AX1 family only

PACKAGE OUTLINES

MAB8401B: 28-lead 'Piggy-back' package (with up to 28-pin EPROM on top).
MAB8401WP: 68-lead plastic leaded chip-carrier (PLCC) (SOT-188).
MAB/MAF8411/21/41/61P: 28-lead DIL; plastic (SOT-117).
MAF84A11/21/41/61P: 28-lead DIL; plastic (SOT-117).
MAB8411/21/41/61T: 28-lead mini-pack; plastic (SO-28; SOT-136A).

PINNING

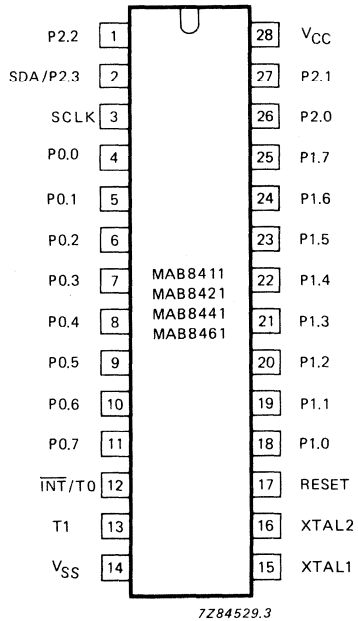
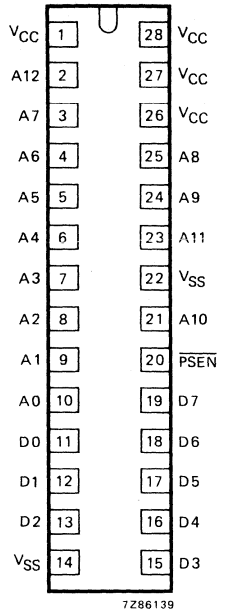


Fig. 1 Pinning diagram for mask-programmable devices MAB8411, MAB8421, MAB8441, MAB8461 and for MAB8401 'Piggy-back' version bottom pinning (for top pinning see Fig. 2).

PINNING DESIGNATION

V_{SS}	14	**Ground**
V_{CC}	28	**Power supply,** + 5 V
P0.0 – P0.7	4 – 11	**Port 0,** 8-bit quasi-bidirectional I/O port
P1.0 – P1.7	18 – 25	**Port 1,** 8-bit quasi-bidirectional I/O port with 8-bit LED driver
P2.0 – P2.3	26, 27, 1, 2	**Port 2,** 4-bit quasi-bidirectional I/O port; SDA/P2.3 is the serial data I/O in serial I/O mode
SCLK	3	Bidirectional clock for serial I/O
$\overline{INT}$/T0	12	External interrupt input (sensitive to a negative-going edge min LOW > 7 clock pulses, min HIGH > 4 clock pulses), testable using the JT0 or JNT0 instructions.
T1	13	Input pin, testable using the JT1 or JNT1 instructions. It can be designated as event counter input using the STRT CNT instruction. It can also be used to detect zero cross-over of slowly moving a.c. inputs.
RESET	17	Input to initialize the processor (active HIGH).
XTAL1	15	Connection to timing component (crystal) that determines the frequency of the internal oscillator. It is also the input for an external clock source.
XTAL2	16	Connection to other side of the timing component.

MAB8401B (top pinning)



PIN DESIGNATION

designation	pin	function
V_{SS}	14, 22	**Ground**
V_{CC}	1, 26–28	**Power supply,** + 5 V
A0–A12	10–3, 25, 24, 21, 23, 2	Address outputs
D0–D7	11–13, 15–19	Data inputs
$\overline{PSEN}$	20	Program store enable

Fig. 2 Pinning diagram for MAB8401B 'Piggy-back' version top pinning (for bottom pinning see Fig. 1); to access a 2732 or 2764 EPROM.

Note

Access times for ROMS/EPROMS to be below 1 μs.

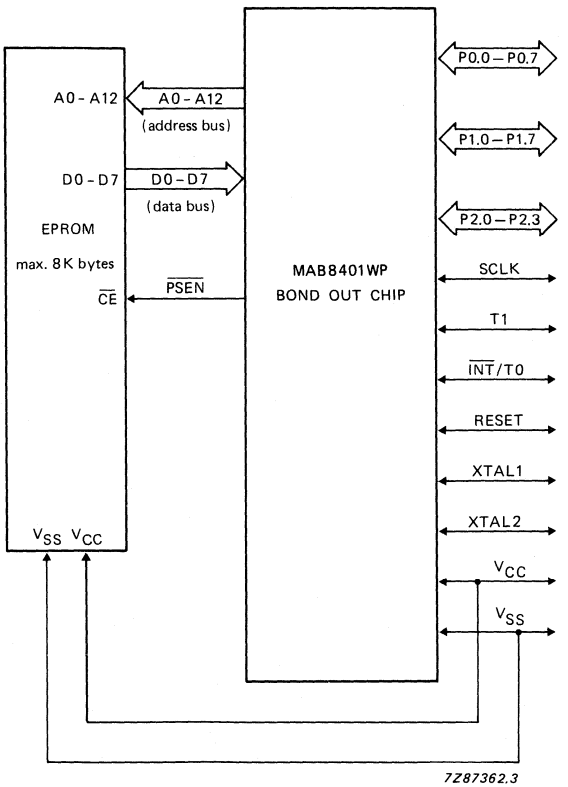


Fig. 2a Connection of EPROM to 'Piggy-back' package MAB8401B.

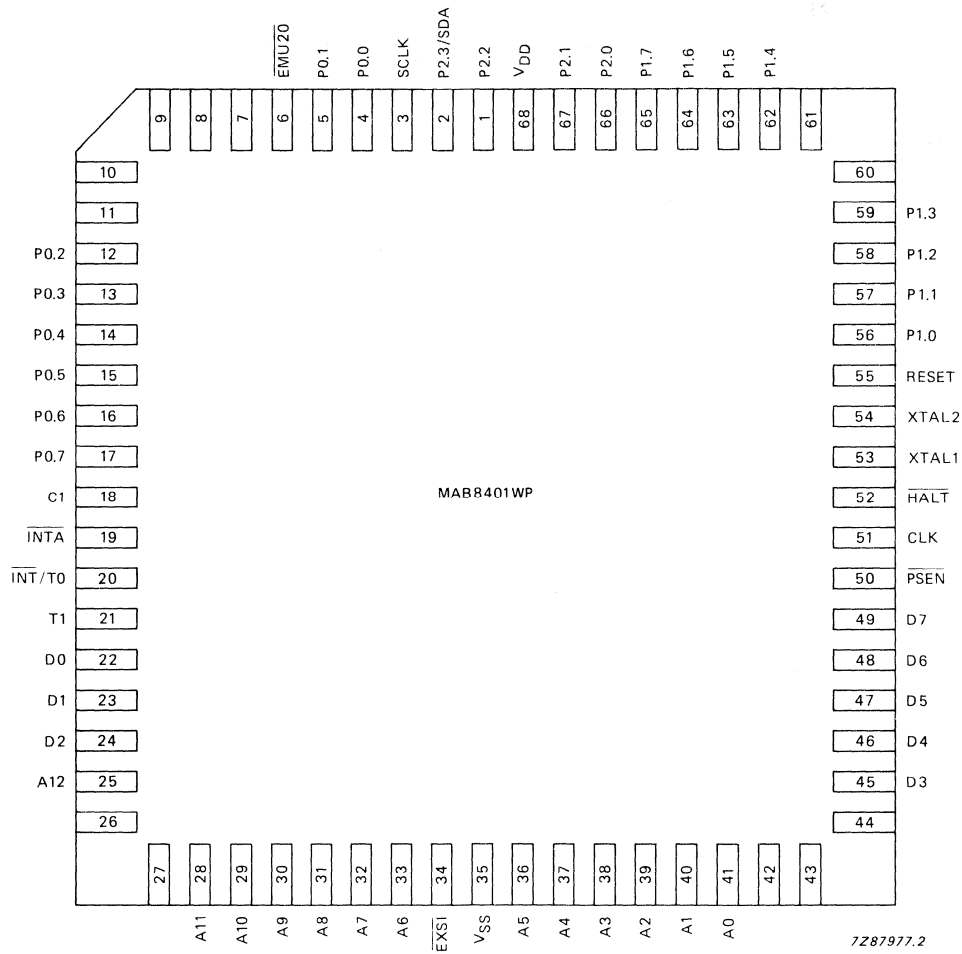


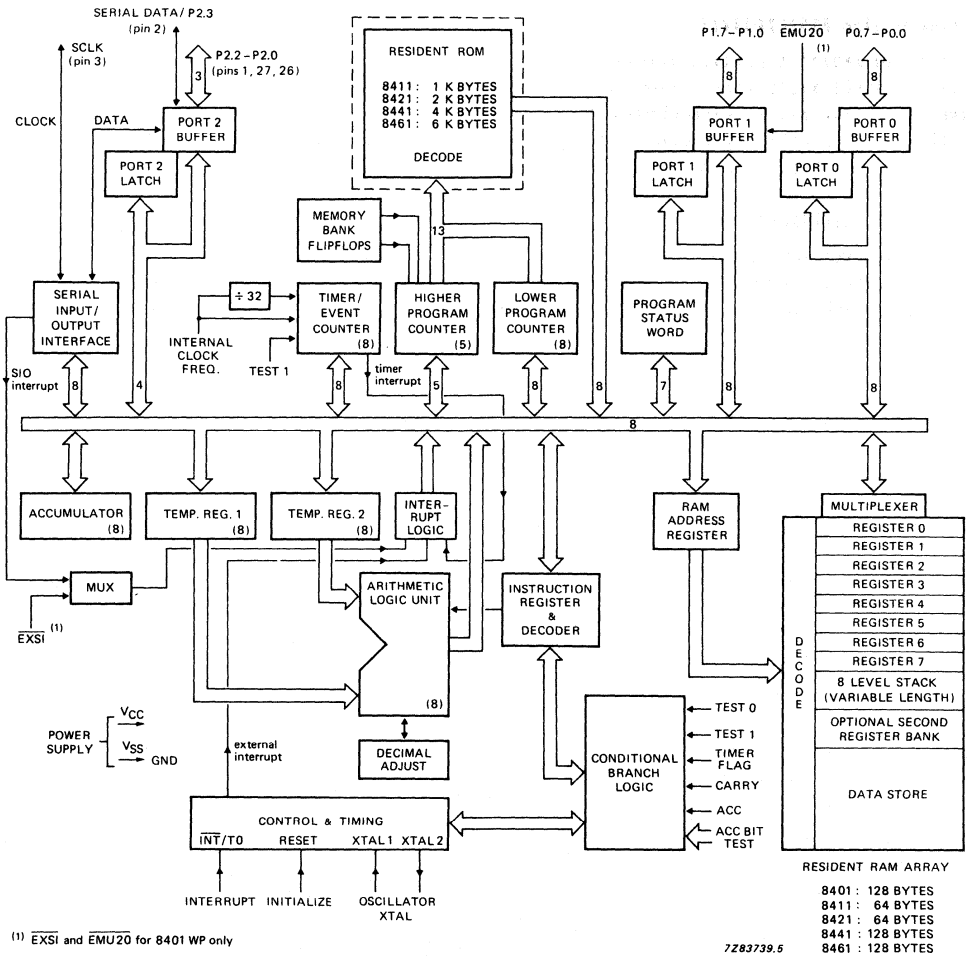
Fig. 3 Pinning diagram; PLCC.

CHIP CARRIER DESIGNATION

designation	pad no.	function
V_{SS}	35	**Ground**
V_{CC}	68	**Power supply**, + 5 V
P0.0 – P0.7	4–5, 12–17	**Port 0,** 8-bit quasi-bidirectional I/O port
P1.0 – P1.7	56–59, 62–65	**Port 1,** 8-bit quasi-bidirectional I/O port with 8-bit LED driver
P2.0 – P2.3	66, 67, 1, 2	**Port 2,** 4-bit quasi-bidirectional I/O port; SDA/P2.3 is the serial data I/O in serial I/O mode
SCLK	3	Bidirectional clock for serial I/O
$\overline{INT}$/T0	20	External interrupt input (sensitive to a negative-going edge), testable using the JT0 or JNT0 instructions

T1	21	Input pin, testable using the JT1 or JNT1 instructions. It can be designated as event counter input using the STRT CNT inctruction. It can also be used to detect zero cross-over of slowly moving a.c. inputs.
RESET	55	Input to initialize the processor (active HIGH)
XTAL1	53	Connection to timing component (e.g. crystal) that determines the frequency of the internal oscillator. It is also the input for an external clock source.
XTAL2	54	Connection to other side of the timing component
$\overline{EXSI}$	34	External serial I/O interrupt (active-LOW) for emulation of MAB/F8422/42.
A0–A12	41–36, 33–28 25	Program memory address outputs (active HIGH); A0 = LSB, A12 = MSB. Address output change after begin ϕ3 of TS8.
D0–D7	22–24, 45–49	Data input lines (active HIGH) used for reading external program memory. D0 = LSB, D7 = MSB.
CLK	51	Clock output buffered from XTAL2. On the positive-going edge the (internal) ϕ clock goes HIGH.
$\overline{PSEN}$	50	Program store enable. This signal is used for enabling the external EPROM (e.g. on the 'Piggy-back' version). For emulation, it enables the emulation memory and it indicates machine cycles. Active LOW during TS9,*TS10 of each machine cycle and TS1 of the following machine cycle.
$\overline{C1}$	18	Cycle 1 indication output (active LOW). During emulation, this signal indicates the opcode fetch cycle (useful for external instruction decoding, real-time trace). Active from start of TS10 of the cycle preceding cycle 1, until the start of TS10 of cycle 1.
$\overline{HALT}$	52	Halt input (active LOW). If activated, the current instruction is finished and the microcontroller stops execution (HALT mode). The next program counter address is available on the address bus. Program counter and timer/event counter are no longer updated. The serial I/O finishes the current transmit/receive action and goes into the idle state. Interrupts are *not* sampled in the HALT mode, they are only sampled when the microcontroller is running. Interrupt routines can be single-stepped as a normal program.
$\overline{INTA}$	19	Interrupt acknowledge output (active LOW). It indicates any interrupt acception. Active from start of TS8 of the interrupted cycle, until start of TS7 of the second cycle of the (internally forced 'CALL vector address' instruction. During $\overline{INTA}$ active, the address bus shows the address that has been saved in the stack (return address); the C1 output indicates opcode fetch cycles as if a user CALL was executed.
$\overline{EMU20}$	6	Emulate 20-pin version MAB/F8422/42 (active-LOW).

*TS = Time slot, where 10 TS = 1 cycle



(1) EXSI and EMU20 for 8401 WP only

Fig. 4a Block diagram of the MAB84X1 family.

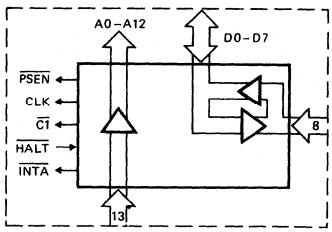


Fig. 4b Replacement for dotted part in Fig. 4a for the MAB8401WP bond-out version.

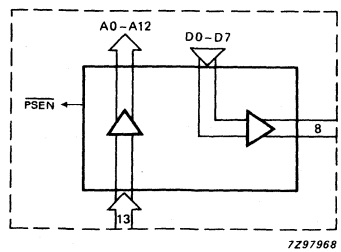


Fig. 4c Replacement of dotted part in Fig. 4a for the MAB8401B 'Piggy-back' version.

FUNCTIONAL DESCRIPTION (for more detail see Microcontroller Users Manual)

Bond-out version MAB8401WP

The bond-out version is a microcontroller that contains no on-board ROM, but has all address and data lines brought out to access an external ROM or EPROM. Thus, this version has more pins than the standard microcontrollers with on-board ROM. It has all the features of the other members of the MAB84X1 family, including emulation facilities for the MAB/F8422/42 (20-pin version). It can address 8K bytes of external ROM. The RAM has 128 bytes.

Piggy-back version MAB8401B

The Piggy-back version is a special package that has standard pinning to the bottom which facilitates insertion as a mask-programmed device. An EPROM is mounted on top in an additional socket. Thus, the total package height is greater than the standard DIL package. Emulation of the 8422/42 is not possible.

Program and data memory

The program memory (ROM) is mask-programmed at our factory. Because the MAB84X1 family offers a range of ROM capacities to suit the application, ROM expansion is not required. Figure 5 shows the program memory map. Program memory is arranged in banks of 2K bytes, that are selected by SEL MB instructions.

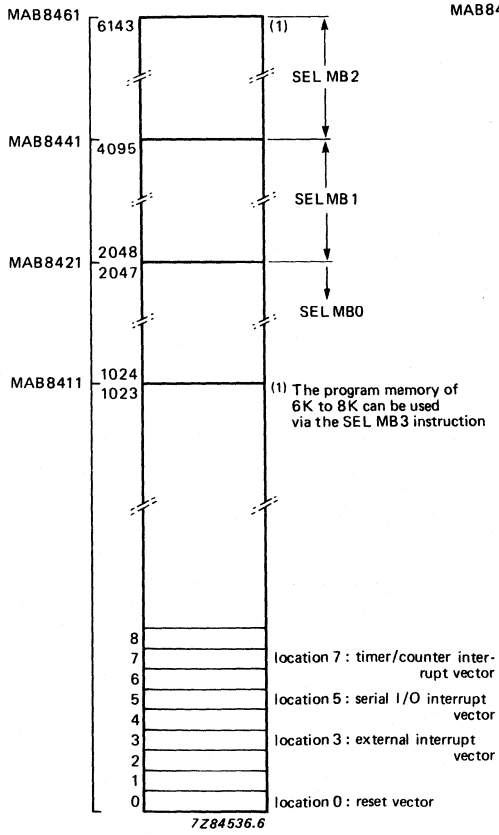


Fig. 5 The program memory map.

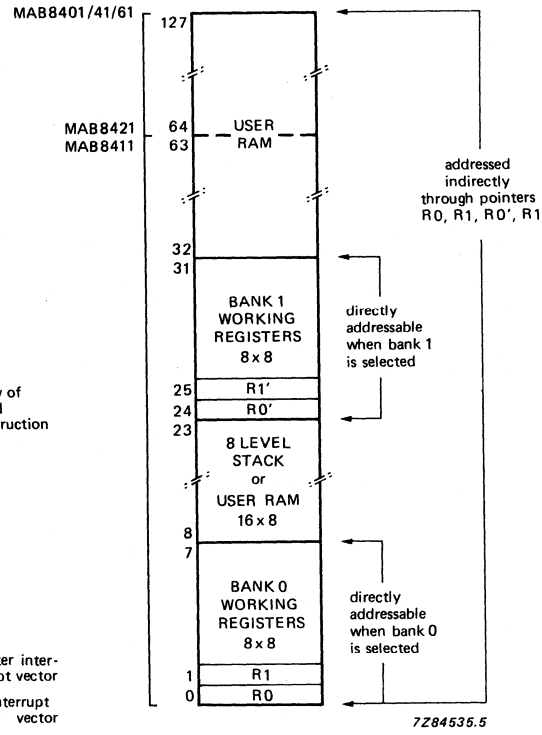


Fig. 6 The data memory map.

FUNCTIONAL DESCRIPTION (continued)

The data memory (RAM) consists of 64 or 128 bytes (8-bit words). All locations are indirectly addressable using RAM pointer registers and up to 16 designated location can be addressed directly. The memory also includes an 8-level program counter stack addressed by a 3-bit stack pointer. Figure 6 shows the data memory map.

On-chip peripheral functions

In addition to the CPU and memories, an interrupt system, I/O facilities, and an 8-bit timer/event counter are integrated on-chip to assist the CPU in repetitions, complicated or time-critical tasks. The I/O facilities include the I/O pins, parallel ports and a serial I/O port, consisting of a data line SDA shared with a parallel port line (P2.3), and a dedicated clock line SCLK.

I/O facilities

The MAB84XX family has 23 I/O lines arranged as:

- Two parallel ports of 8 lines (P0.0–P0.7, P1.0–P1.7). Each line of Port 1 can sink 10 mA.
- A parallel port of 4 lines (P2.0–P2.3).
- A serial I/O consisting of a data line shared with a parallel port line (P2.3) and a separate clock line SCLK;
- An external interrupt and test input $\overline{\text{INT}}$/T0, which when used as a test input can be tested by the conditional jump instructions JT0 or JNT0;
- A test input T1, which can alter program sequences when tested by conditional jump instructions JT1 or JNT1. T1 can also be used as an input to the timer/event counter or to detect zero cross-over of slowly moving AC signals.

All parallel port lines are available in three optional output configurations (except P2.3 – option 1 only):

- Option 1; open drain output without pull-up transistor (Fig. 7(a))
- Option 2; open drain output with pull-up transistor (Fig. 7(b))
- Option 3; push-pull output with pull-up transistor (Fig. 7(c))

If the inputs and outputs on a port are mixed (mixed-mode), the inputs should be options 1 or 2 but not option 3. This prevents cross-currents via TR2 and an external connection to ground, while switching the output on the same port and in parallel, masking the inputs with logic 1 s.

The MAB84X1 family serial I/O interface has been designed to eliminate the heavy processing load imposed upon a normal microcontroller performing serial data transfer. Whereas a normal microcontroller must regularly monitor the serial data bus for the presence of data, the serial I/O interface detects, receives and converts the serial data stream into a parallel format without interrupting the execution of the current program. An interrupt is sent to the microcontroller only when a complete byte is received. Then, the microcontroller reads the data byte in one instruction. Likewise, for transmission, the serial I/O interface performs parallel to serial conversion and subsequent serial output of the data and the microcontroller is only interrupted in the execution of its programmed tasks when a complete byte has been transmitted. The design of the serial I/O interface allows any number of MAB84X1 family devices and peripheral circuits with I^2C bus compatibility to be interconnected by the two-line serial bus. This is achieved by allocating a specific 7-bit address to each device and ensuring that a device reacts only to a message preceded by its own address or the 'general call' address.

Address recognition is performed by the interface hardware so that the microcontroller need only be interrupted when a valid address is received. This saves significant processing time and memory space compared to a conventional microcontroller with a software serial interface. When the address facility is not required, for instance in a system with only two microcontrollers, direct data transfer is possible. In multi-master systems, an automatically invoked arbitration procedure prevents two or more devices transmitting simultaneously.

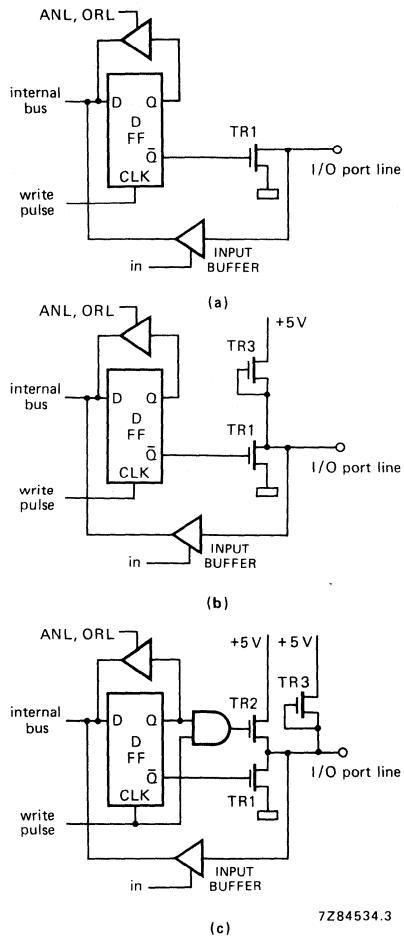


Fig. 7 Quasi-bidirectional I/O interface with (a) open drain output without pull-up transistor, (b) open drain output with pull-up transistor, (c) push-pull output with pull-up transistor.

Serial I/O interface

Figure 8 shows the serial I/O interface. The clock line of the serial bus has exclusive use of pin 3 (SCLK) while the data line shares pin 2 (serial data) with the I/O line P2.3 of port 2. When the serial I/O is enabled, P2.3 is disabled as a parallel port line (P2.3 and SCLK only open drain).

The microcontroller and interface communicate via the internal microcontroller bus and the Serial Interrupt Request line. Data and information controlling the operation of the interface are stored in four registers:

- data shift register S0,
- serial I/O interface status word S1,
- serial clock control word S2,
- address register S0'

FUNCTIONAL DESCRIPTION (continued)

Serial I/O interface (continued)

Data shift register S0

S0 is the shift register that converts serial data to parallel format and vice versa. A pending interrupt is generated only after a complete byte has been transmitted, or after a complete data byte, specific or general call address has been received. The most significant bit is transmitted first.

Serial I/O interface status word S1

S1 provides information about the state of the interface and stores interface control information from the microcontroller. The four most significant bits are common to both read and write instructions, with a separate 4 read-only control bits and 4 write-only interface status bits.

MST and TRX

These bits determine the operating mode of the serial I/O interface (Table 2).

Table 1 Operating modes of the serial I/O interface.

MST	TRX	mode
0	0	slave receiver
1	0	master receiver
0	1	slave transmitter
1	1	master transmitter

BB: Bus Busy

This bit indicates the status of the bus.

PIN: Pending Interrupt Not

PIN = '0' indicates that there is an interrupt pending. This causes a Serial Interrupt Request when the serial interrupt mechanism is enabled.

ESO: Enable Serial Output

The ESO flag enables/disables the serial I/O interface: ESO = logic 1 enables
ESO = logic 0 disables

BC0, BC1 and BC2

These bits indicate the number of bits received or transmitted in a serial data stream.

Bits ES0, BC0, BC1 and BC2 can only be written via software.

AL: Arbitration Lost

The AL flag is set via the hardware when the serial I/O interface, as a master transmitter, loses the bus arbitration procedure.

AAS: Addressed As Slave

This flag is set via the hardware when the interface detects either its own address or the 'general call' address as the first byte of a transfer and if the interface has been programmed to operate in the address recognition mode.

AD0: Address Zero

This flag is set via the hardware after the general call address is detected when the interface is operating in the address recognition mode.

LRB: Last Received Bit

This contains either the last data bit received or, for a transmitting device in the acknowledge mode, the acknowledge from the receiving device.

Bits AL, AAS, AD0 and LRB can only be read via software.

Serial clock control register S2

Bits 0 to 4 of S2 are used to set the frequency of the serial clock signal. When a 4,43 MHz crystal is used, the frequency of the serial clock can be varied between 100 kHz and 720 Hz. An asymmetrical clock with a HIGH to LOW ratio of 3 to 1 is produced by setting bit 5. The asymmetrical clock allows a microcontroller more time per clock period for sampling the data line, making the timing of this action less critical. Bit 6 is used to activate the acknowledge mode of the serial I/O. S2 is a write-only register.

Address register S0'

The address register contains the 7-bit address back-up latches and the bit (ALS) used to enable/disable the address recognition mode. Only when ES0 = 0 can the address register be written using the MOV S0,A and MOV S0,#data instructions.

Serial I/O interrupt logic

The interrupt logic is enabled by the EN SI instruction and disabled by DIS SI. When the interrupt logic is enabled, a pending interrupt results in a serial I/O interrupt to the controller, causing a jump to location 5 in the ROM. When the logic is disabled, the presence of an interrupt is still indicated by the PIN bit in register S1. Therefore, an interrupt can still be serviced but a vectored interrupt will not occur.

Interrupt system

External events and real-time on-chip peripherals require servicing by the CPU asynchronous to the execution of any particular section of code. To tie the asynchronous activities of these functions to normal program execution, three single-level nested interrupts are provided.

Each interrupt vectors to a separate location in the program memory for its service program. Each source can be individually enabled or disabled. When more than one interrupt occurs simultaneously, their priority will be: (1) external, (2) serial I/O and, (3) timer/event counter. An additional external interrupt can be created using the timer/event counter interrupt.

FUNCTIONAL DESCRIPTION (continued)

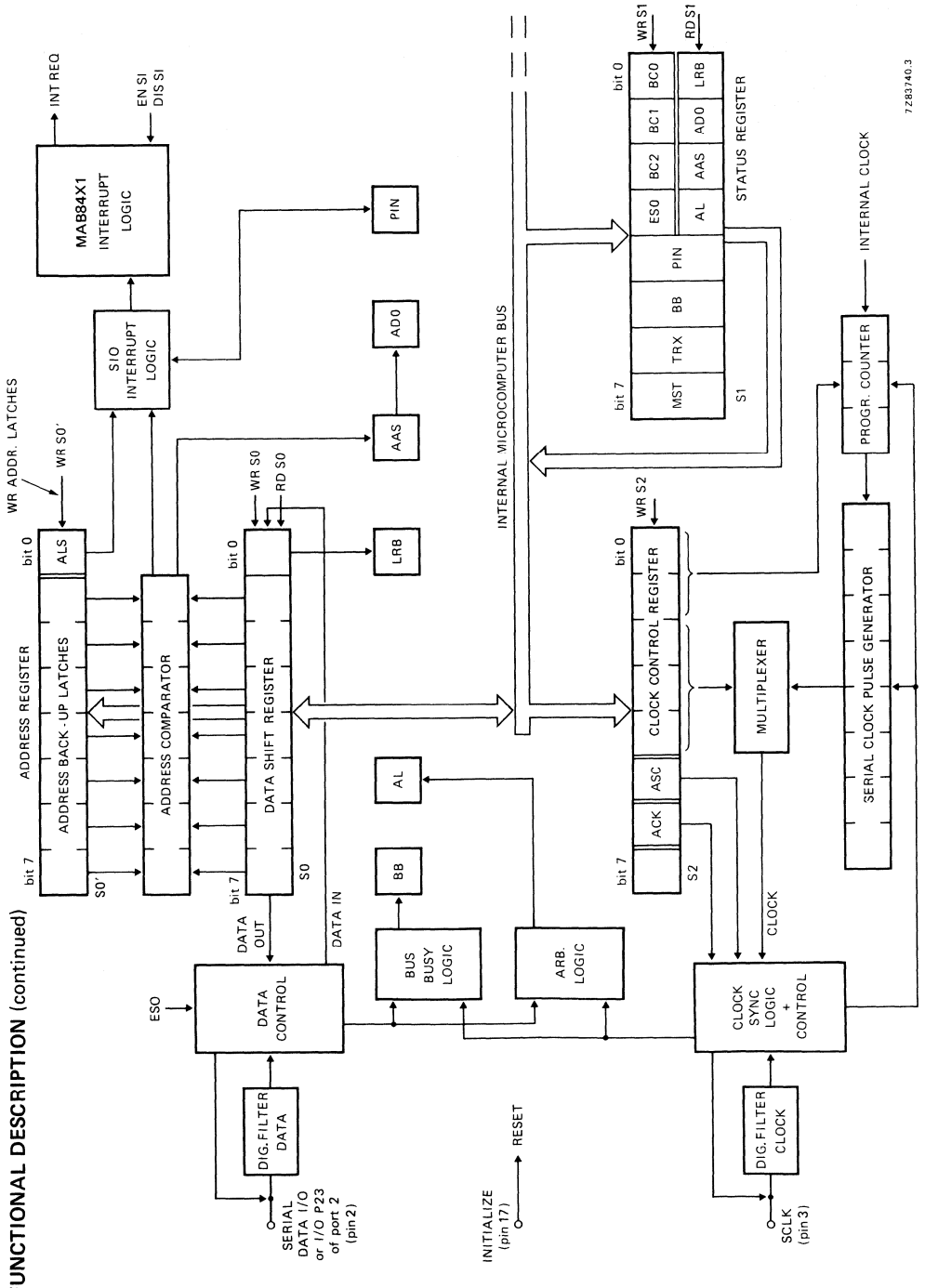


Fig. 8 The serial I/O interface.

Test input T1

The T1 input line can be used as:

- a test input for branch instructions,
- an input for zero voltage cross-over detection,
- an external input to the event counter.

An internal pull-up transistor is provided as a ROM mask option. This is useful when the input is from a switch or standard TTL output.

When T1 is used as a test input, the JT1 or JNT1 instructions test for a HIGH or a LOW respectively.

When used for zero-cross detection purposes, the T1 input must be coupled through a capacitor of typical value 1 μF and operation carried out using the T1 input without the pull-up transistor. The maximum input voltage amplitude is 3 V (peak-to-peak), with a maximum operational frequency of 1 kHz. The T1 input has an on-chip DC offset circuit which self-biases the input to its exact switching level of 1 V. As a consequence a small change will cause a digital transition to occur. The switching level of the T1 input circuit is within the bias voltage of ± 135 mV. Upon each positive cycle on the pin, the event counter is incremented and an overflow will set the timer flag TF. Zero cross-over detection used in conjunction with the timer/event counter interrupt, is useful in thyristor control of power equipment. Figure 9 illustrates, (a) the input waveform, (b) the input diagram and (c) the on-chip self-stabilized bias.

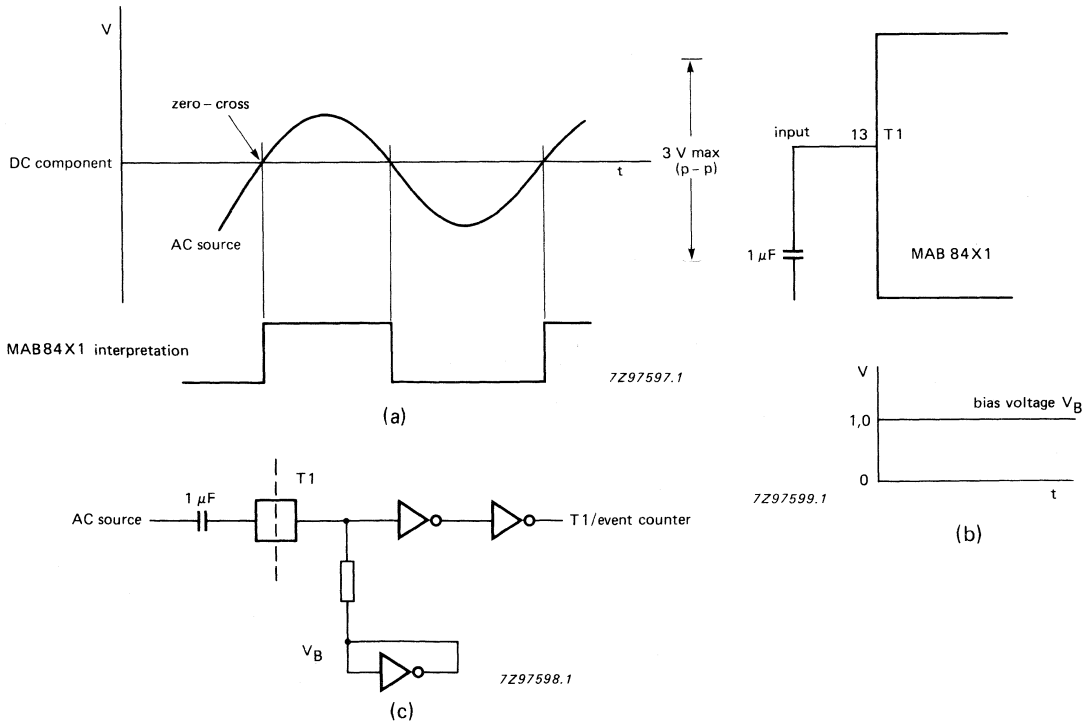


Figure 9 Zero-cross detection circuitry; (a) input waveform, (b) input diagram, (c) on-chip self-stabilized bias.

The operation of T1 as an input to the timer/event counter is described under the heading Timer/event counter.

High current outputs

Ten pins are provided that can sink high currents:

– P2.3 (serial data), pin 2	5 mA at 0,45 V (open drain),
– SCLK, pin 3	5 mA at 0,45 V (open drain),
– P1.0 – P1.7 *	10 mA at 1 V

* P1.0 to P1.7 may be connected in parallel if their logic outputs are always the same.

FUNCTIONAL DESCRIPTION (continued)

Timer/event counter

An 8-bit binary up-counter is provided. This can count external events, machine cycles divided by 32, or machine cycles directly. When used as a timer, the input to the counter is either the overflow or input of a 5-bit prescaler. When used as an event counter, LOW to HIGH transitions on T1 (pin 13) are counted. The maximum rate at which the counter may be incremented is once every machine cycle (200 kHz for a 5 μs machine cycle). Figure 10 illustrates the timer/event counter.

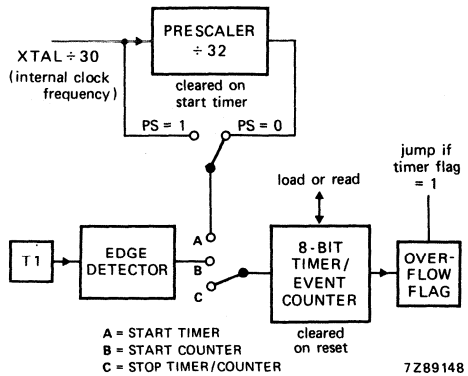


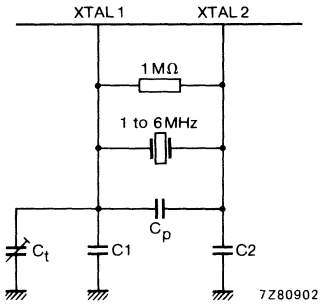
Fig. 10 The timer/event counter.

Differences between the MAB8021 and MAB8048 microcontrollers, and the MAB84X1 family.

	8021	8048	8401, 8411 8421, 8441, 8461
ROM capacity (bytes)	1K	1K	ROMless, 1K, 2K, 4K, 6K
RAM capacity (bytes)	64	64	128, 64, 64, 128, 128
paralel I/O lines	8 + 8 + 4	8 + 8 + 8	8 + 8 + 4
single inputs	1	3	2
serial I/O	no	no	yes, 2-line multi-transmitter
timer	8 bit	8 bit	8 bit
prescaler	mod. 32	mod. 32	mod. 1 & mod. 32
machine cycle time (μs)	10	2,5	5
for clock (MHz)	3	6	6
instruction set	8021	8048	8048 with omissions; 5 new serial I/O instructions; 2 new register instructions; 2 new control instructions; 1 new cond. branch instruction
interrupts	none	2 external timer/ event counter	3 external serial I/O timer/event counter
no. of pins (DIL)	28	40	68 (PLCC), 28

OSCILLATOR CIRCUITRY

Clock frequency is determined by using the internal oscillator or by connecting an external clock to XTAL1. Where the internal oscillator is used, the frequency is set by a crystal between XTAL1 and XTAL2, or by a ceramic resonator or an inductor, each with two associated capacitors, between XTAL1 and XTAL2 (see Fig. 11a). A machine cycle consists of 10 states, each state being 3 oscillator periods. The common 6 MHz crystal gives a 5 μs machine cycle. The MAB84X1 family has dynamic logic, and therefore, for adequate refreshing the oscillator frequency must be at least 1 MHz.



1. Crystal – AT-cut
2. Ceramic resonator
   C1 = C2 = 27 pF
   C1 may be trimmed
   $C_p \leqslant 6{,}75$ pF (parasitic capacitance)

Fig. 11a Quartz crystal or ceramic resonator mode.

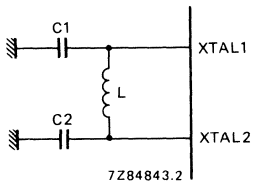


Fig. 11b LC pi-network.

LC oscillator timing

frequency	C1 = C2	L
3,0 MHz	33 pF	100 μH
4,0 MHz	33 pF	56 μH
4,4 MHz	33 pF	47 μH
5,0 MHz	33 pF	33 μH
6,0 MHz	33 pF	22 μH

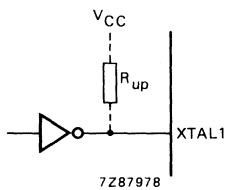


Fig. 11c External drive.

Drive XTAL1
Leave XTAL2 open

Driver may be high-speed CMOS or any TTL
t_r, $t_f < 10$ ns

PROGRAM STATUS WORD

The program status word (PSW) is an 8-bit word in the CPU which stores information about the current status of the microcontroller (Fig. 12). The PSW bits are:

bits 0, 1 and 2 – stack pointer bits (SP_0, SP_1, SP_2);

bit 3 – prescaler select (PS); 0 = divide-by-32; 1 = no prescaling;

bit 4 – working register bank select (RBS):
0 = register bank 0
1 = register bank 1;

bit 5 – not used (1);

bit 6 – auxiliary carry (AC):
half-carry bit is generated by an ADD instruction and used by the decimal adjust instruction DA A;

bit 7 – carry (CY):
the carry flag indicates that the previous operation has resulted in an overflow of the accumulator.

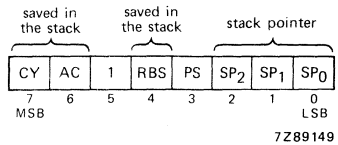


Fig. 12 Program status word.

All bits can be read using MOV A, PSW and bit 3 can be written with MOV PSW, A.

Bits 6 and 7 can be set and cleared by CPU operation. Bit 4 is changed by the SEL RB instruction, bit 3 by the MOV PSW,A instruction, and bits 0, 1 and 2 by the CALL, RET or RETR instructions and when an interrupt occurs. Bits 4, 6 and 7 are stored in the program counter stack during sub-routine and interrupt calls. These bits are restored to the PSW with RETR (return and restore) instruction.

Note: The RET instruction has no restore feature and should not be used at the end of an interrupt because this would leave any further interrupts disabled.

The MAB84X1 family has arithmetic, logical and branching capabilities. The DA A, SWAP A, and XCHD instructions simplify BCD arithmetic and the handling of nibbles. The MOVP A,@A instruction permits efficient table look up from the current ROM page.

The conditional branch logic within the processor enables several conditions, internal and external to the processor, to be tested by the user's program. Table 2 lists the conditional branch instructions used to change the program execution sequence. The DJNZ instruction decrements a designated register and branches if the contents are not zero. This instruction makes the register an efficient program loop counter. The JMPP @A instruction allows multiway branches to destinations indirectly addressed by the contents of the accumulator.

Table 2 Conditional branches

TEST	JUMP CONDITION	JUMP INSTRUCTION
accumulator	0 or non-zero	JZ, JNZ
accumulator bit test	1	JB0 to JB7
carry flag	0 or 1	JNC, JC
timer overflow flag	1	JTF
test input $\overline{INT}$	0 or 1	JNT0, JT0
test input T1	0 or 1	JNT1, JT1
test flag 0	1	JF0
test flag 1	1	JF1
register	non-zero	DJNZ

RESET

A positive-going signal on the RESET input:

- sets the program counter to zero,
- selects location 0 of memory bank 0, and register bank 0,
- sets the stack pointer to zero ('000'B); pointing to RAM address 8,
- disable the interrupts (external, timer and serial I/O),
- stops the timer/event counter, then sets it to zero,
- sets the timer prescaler to divide-by-32,
- resets the timer flag,
- sets all ports to logic '1' (input mode),
- sets the serial I/O to slave receiver mode and disables serial I/O.

Automatic reset at power-up may be obtained by connecting the RESET pin to V_{CC} through a 1 μF capacitor C, together with a diode to V_{SS} (cathode to RESET pin). This arrangement is satisfactory, if both the voltage (V_{CC}) rise time and the oscillator start-up time do not exceed either 1 or 10 ms respectively.

The power-on reset circuit is shown in figure 13. At power-on the current drawn by RESET commences to charge the capacitor C. The difference between this increasing capacitor voltage and V_{CC} is known as V_{RESET}. The charging circuit is designed to hold V_{RESET} above the lower threshold of a Schmitt trigger arrangement long enough to effect a complete reset. The minimum time required; is the oscillator start-up time plus two machine cycles.

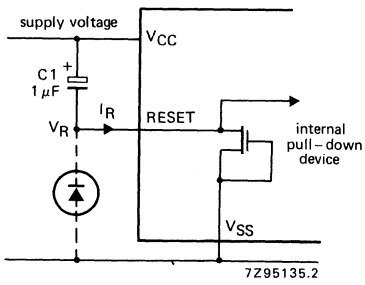


Fig. 13 Typical power-on reset circuitry.

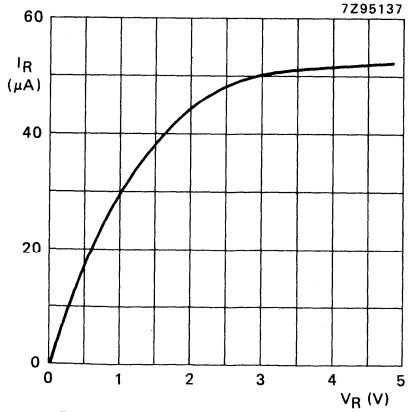


Fig. 14 Power-on reset input characteristics (typical).

INSTRUCTION SET

The instruction set consists of over 80 one and two byte instructions and is based on the MAB8048 instruction set. New instructions include those for serial I/O operation and memory bank selection. Program code efficiency is high because all ROM locations on a 256 byte page require only a single byte address.

Table 3 gives the instruction set of the MAB84X1 family and Table 4 shows the instruction map. The following symbols and abbreviations are used.

Note: During development of software on a PMDS or similar system, it is important to ensure that no jump instruction (direct or indirect), outreaches the final address range of the device.

symbol	description
A	the accumulator
AC	the auxiliary carry flag
addr	program memory address (11-bits)
Bb	bit designation (b = 0–7)
BS	the bank switch
C	carry flag
CLK	clock signal
CNT	event counter
D	nibble designation (4-bits)
DBF	program memory bank flip-flop
data	number or expression (8-bits)
F0, F1	flags 0 and 1
I	interrupt
$\overline{\text{INT}}$	external interrupt
P	'in-page' operation designation
Pp	port designation (p = 1, 2 or 4–7)
PSW	program status word
Rr	register designation (r = 0, 1 or 0–7)
SP	stack pointer
T	timer
TF	timer flag
T0, T1	test 0 and 1 inputs
#	immediate data prefix
@	indirect address prefix
$	current value of program counter
←	is replaced by
↔	is exchanged with

Table 3 MAB84XX family instruction set

	mnemonic	opcode (hex.)	bytes/ cycles	description	function		notes
ACCUMULATOR	ADD A, Rr	6*	1/1	Add register contents to A	(A)←(A) + (Rr)	r = 0–7	1
	ADD A, @Rr	60 61	1/1	Add RAM data, addressed by Rr, to A	(A)←(A) + ((R0)) (A)←(A) + ((R1))		1
	ADD A, #data	03 data	2/2	Add immediate data to A	(A)←(A) + data		1
	ADDC A, Rr	7*	1/1	Add carry and register contents to A	(A)←(A) + (Rr) + (C)	r = 0–7	1
	ADDC A, @Rr	70 71	1/1	Add carry and RAM data, addressed by Rr, to A	(A)←(A) + ((R0)) + (C) (A)←(A) + ((R1)) + (C)		1
	ADDC A, #data	13 data	2/2	Add carry and immediate data to A	(A)←(A) + data + (C)		1
	ANL A, Rr	5*	1/1	'AND' Rr with A	(A)←(A) AND (Rr)	r = 0–7	
	ANL A, @Rr	50 51	1/1	'AND' RAM data, addressed by Rr, with A	(A)←(A) AND ((R0)) (A)←(A) AND ((R1))		
	ANL A, #data	53 data	2/2	'AND' immediate data with A	(A)←(A) AND data		
	ORL A, Rr	4*	1/1	'OR' Rr with A	(A)←(A) OR (Rr)	r = 0–7	
	ORL A, @Rr	40 41	1/1	'OR' RAM data, addressed by Rr, with A	(A)←(A) OR ((R0)) (A)←(A) OR ((R1))		
	ORL A, #data	43 data	2/2	'OR' immediate data with A	(A)←(A) OR data		
	XRL A, Rr	D*	1/1	'XOR' Rr with A	(A)←(A) XOR (Rr)	r = 0–7	
	XRL A, @Rr	D0 D1	1/1	'XOR' RAM, addressed by Rr, with A	(A)←(A) XOR ((R0)) (A)←(A) XOR ((R1))		
	XRL A, #data	D3 data	2/2	'XOR' immediate data with A	(A)←(A) XOR data		
	INC A	17	1/1	increment A by 1	(A)←(A) + 1		
	DEC A	07	1/1	decrement A by 1	(A)←(A) – 1		
	CLR A	27	1/1	clear A to zero	(A)←0		
	CPL A	37	1/1	one's complement A	(A)←NOT(A)		
	RL A	E7	1/1	rotate A left	$(A_{n+1})\leftarrow(A_n)$ $(A_0)\leftarrow(A_7)$	n = 0–6	

	mnemonic	opcode (hex.)	bytes/ cycles	description	function	notes
ACCUMULATOR (cont.)	RLC A	F7	1/1	rotate A left through carry	$(A_{n+1}) \leftarrow A_n$ n = 0–6 $(A_0) \leftarrow (C)$, $(C) \leftarrow (A_7)$	2
	RR A	77	1/1	rotate A right	$(A_n) \leftarrow (A_{n+1})$ n = 0–6 $(A_7) \leftarrow (A_0)$	
	RRC A	67	1/1	rotate A right through carry	$(A_n) \leftarrow (A_{n+1})$ n = 0–6 $(A_7) \leftarrow (C)$, $(C) \leftarrow (A_0)$	2
	DA A	57	1/1	decimal adjust A		2
	SWAP A	47	1/1	swap nibbles of A	$(A_{4-7}) \leftrightarrow (A_{0-3})$	
DATA MOVES	MOV A, Rr	F*	1/1	move register contents to A	(A)←(Rr) r = 0–7	
	MOV A, @Rr	F0 F1	1/1	move RAM data, addressed by Rr, to A	(A)←((R0)) (A)←((R1))	
	MOV A, #data	23 data	2/2	move immediate data to A	(A)←data	
	MOV Rr, A	A*	1/1	move accumulator contents to register	(Rr)←(A) r = 0–7	
	MOV @Rr, A	A0 A1	1/1	move accumulator contents to RAM location addressed by Rr	((R0))←(A) ((R1))←(A)	
	MOV Rr, #data	B* data	2/2	move immediate data to Rr	(Rr)←data	
	MOV @Rr, #data	B0 data B1 data	2/2	move immediate data to RAM location addressed by Rr	((R0))←data ((R1))←data	
	XCH A, Rr	2*	1/1	exchange accumulator contents with Rr	(A)↔(Rr) r = 0–7	
	XCH A, @Rr	20 21	1/1	exchange accumulator contents with RAM data addressed by Rr	(A)↔((R0)) (A)↔((R1))	
	XCHD A, @Rr	30 31	1/1	exchange lower nibbles of A and RAM data addressed by Rr	$(A_{0-3}) \leftrightarrow ((R0_{0-3}))$ $(A_{0-3}) \leftrightarrow ((R1_{0-3}))$	
	MOV A, PSW	C7	1/1	move PSW contents to accumulator	(A)←(PSW)	
	MOV PSW, A	D7	1/1	move accumulator bit 3 to PSW_3	$(PSW_3) \leftarrow (A_3)$	3
	MOVP A, @A	A3	1/2	move indirectly addressed data in current page to A	$(PC_{0-7}) \leftarrow (A)$, $(A) \leftarrow ((PC))$	

FLAGS	CLR C	97	1/1	clear carry bit	(C)←0		2
	CPL C	A7	1/1	complement carry bit	(C)←NOT(C)		2
REGISTER	INC Rr	1*	1/1	increment register by 1	(Rr)←(Rr) + 1	r = 0–7	
	INC @Rr	10 11	1/1	increment RAM data, addressed by Rr, by 1	((R0))←((R0)) + 1 ((R1))←((R1)) + 1		
	DEC Rr	C*	1/1	decrement register by 1	(Rr)←(Rr) −1	r = 0–7	
	DEC @Rr	C0 C1	1/1	decrement RAM data, addressed by Rr, by 1	((R0))←((R0)) −1 ((R1))←((R1)) −1		
BRANCH	JMP addr	● 4 address	2/2	unconditional jump within a 2K bank	(PC_{8-10})←$addr_{8-10}$ (PC_{0-7})←$addr_{0-7}$ (PC_{11-12})←MBFF 0–1		
	JMPP @A	B3	1/2	indirect jump within a page	(PC_{0-7})←((A))		
	DJNZ Rr, addr	E* address	2/2	decrement Rr by 1 and jump if not zero to addr	(Rr)←(Rr) −1 if (Rr) not zero (PC_{0-7})←addr	r = 0–7	
	DJNZ @Rr, addr	E0 address	2/2	decrement RAM data, addressed by Rr, by 1 and jump if not zero to addr	((R0))←((R0)) −1 if ((R0)) not zero (PC_{0-7})←addr		
		E1 address			((R1))←((R1)) −1 if ((R1)) not zero (PC_{0-7})←addr		
	JBb addr	▲ 2 address	2/2	jump to addr if Acc. bit b = 1	if b = 1: (PC_{0-7})←addr	b = 0–7	
	JC addr	F6 address	2/2	jump to addr if C = 1	if C = 1: (PC_{0-7})←addr		
	JNC addr	E6 address	2/2	jump to addr if C = 0	if C = 0: (PC_{0-7})←addr		
	JZ addr	C6 address	2/2	jump to addr if A = 0	if A = 0: (PC_{0-7})←addr		
	JNZ addr	96 address	2/2	jump to addr if A is NOT zero	if A≠0: (PC_{0-7})←addr		
	JT0 addr	36 address	2/2	jump to addr if T0 = 1	if T0 = 1: (PC_{0-7})←addr		
	JNT0 addr	26 address	2/2	jump to addr if T0 = 0	if T0 = 0: (PC_{0-7})←addr		
	JT1 addr	56 address	2/2	jump to addr if T1 = 1	if T1 = 1: (PC_{0-7})←addr		
	JNT1 addr	46 address	2/2	jump to addr if T1 = 0	if T1 = 0: (PC_{0-7})←addr		
	JTF addr	16 address	2/2	jump to addr if Timer Flag = 1	if TF = 1: (PC_{0-7})←addr		4
	JNTF addr	06 address	2/2	jump to addr if Timer Flag = 0	if TF = 0: (PC_{0-7})←addr		

	mnemonic	opcode (hex.)	bytes/ cycles	description	function	notes
TIMER/EVENT COUNTER	MOV A, T	42	1/1	move timer/event counter contents to accumulator	(A)←(T)	
	MOV T, A	62	1/1	move accumulator contents to timer/event counter	(T)←(A)	
	STRT CNT	45	1/1	start event counter		
	STRT T	55	1/1	start timer		
	STOP TCNT	65	1/1	stop timer/event counter		
	EN TCNTI	25	1/1	enable timer/event counter interrupt		
	DIS TCNTI	35	1/1	disable timer/event counter interrupt		
CONTROL	EN I	05	1/1	enable external interrupt		
	DIS I	15	1/1	disable external interrupt		
	SEL RB0	C5	1/1	select register bank 0	(RBS)←0	5
	SEL RB1	D5	1/1	select register bank 1	(RBS)←1	5
	SEL MB0	E5	1/1	select program memory bank 0	(MBFF0)←0, (MBFF1)←0	
	SEL MB1	F5	1/1	select program memory bank 1	(MBFF0)←1, (MBFF1)←0	
	SEL MB2	A5	1/1	select program memory bank 2	(MBFF0)←0, (MBFF1)←1	
	SEL MB3	B5	1/1	select program memory bank 3	(MBFF0)←1, (MBFF1)←1	
SUBROUTINE	CALL addr	▲ 4 address	2/2	jump to subroutine	((SP))←(PC), ($PSW_{4, 6, 7}$) (SP)←(SP) + 1 (PC_{9-10})←$addr_{8-10}$ (PC_{0-7})←$addr_{0-7}$ (PC_{11-12})←MBFF 0–1	6
	RET	83	1/2	return from subroutine	(SP)←(SP) – 1 (PC)←((SP))	6
	RETR	93	1/2	return from interrupt and restore bits 4, 6, 7 of PSW	(SP)←(SP) – 1 ($PSW_{4, 6, 7}$) + (PC)←((SP))	6

PARALLEL INPUT/OUTPUT	IN A, Pp	08 09 0A	1/2	input port p data to accumulator	(A)←(P0) (A)←(P1) (A)←(P2)	7
	OUTL Pp, A	38 39 3A	1/2	output accumulator data to port p	(P0)←(A) (P1)←(A) (P2)←(A)	
	ANL Pp, #data	98 data 99 data 9A data	2/2	AND port p data with immediate data	(P0)←(P0) AND data (P1)←(P1) AND data (P2)←(P2) AND data	
	ORL Pp, #data	88 data 89 data 8A data	2/2	OR port p data with immediate data	(P0)←(P0) OR data (P1)←(P1) OR data (P2)←(P2) OR data	
	OUTL PO,A	90	1/2	Output accumulator data to port ϕ	(P0)←(A)	9
SERIAL INPUT/OUTPUT	MOV A, S_n	0C 0D	1/2	move serial I/O register contents to accumulator	(A)←(S0) (A)←(S1)	8
	MOV S_n, A	3C 3D 3E	1/2	move accumulator contents to serial I/O register	(S0)←(A) (S1)←(A) (S2)←(A)	
	MOV S_n, #data	9C data 9D data 9E data	2/2	move immeidate date to serial I/O register	(S0)←data (S1)←data (S2)←data	
	EN SI	85	1/1	enable serial I/O interrupt		
	DIS SI	95	1/1	disable serial I/O interrupt		
	NOP	00	1/1	no operation		

Notes to Table 3.

1. PSW CY, AC affected
2. PSW CY affected
3. PSW PS affected
4. Execution of JTF and JNTF instructions resets the Timer Flag (TF).
5. PSW RBS affected
6. PSW SP_0, SP_1, SP_2 affected
7. (A) = 1111 P2.3, P2.2, P2,1, P2,0.
8. (S1) has a different meaning for read and write operation, see serial I/O interface.
9. Only for software-transfer from the MAB8021.

* : 8, 9, A, B, C, D, E, F
● : 0, 2, 4, 6, 8, A, C, E
▲ : 1, 3, 5, 7, 9, B, D, F

Table 4 MAB84X1 family instruction set

first hexadecimal character of opcode ↓ / second hexadecimal character of opcode →

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	NOP			ADD A, # data	JMP page 0	EN I	JNTF addr	DEC A	IN A,Pp 0	1	2		0	MOV A,Sn 1		
1	INC @Rr 0	1	JB0 addr	ADDC A, # data	CALL page 0	DIS I	JTF addr	INC A	0	1	2	INC Rr 3	4	5	6	7
2	XCH A, @Rr 0	1		MOV A, # data	JMP page 1	EN TCNTI	JNT0 addr	CLR A	0	1	2	XCH A,Rr 3	4	5	6	7
3	XCHD A, @Rr 0	1	JB1 addr		CALL page 1	DIS TCNTI	JT0 addr	CPL A	OUTL Pp,A 0	1	2		MOV Sn,A 0	1	2	
4	ORL A, @Rr 0	1	MOV A, T	ORL A, # data	JMP page 2	STRT CNT	JNT1 addr	SWAP A	0	1	2	ORL A,Rr 3	4	5	6	7
5	ANL A, @Rr 0	1	JB2 addr	ANL A, # data	CALL page 2	STRT T	JT1 addr	DA A	0	1	2	ANL A,Rr 3	4	5	6	7
6	ADD A, @Rr 0	1	MOV T, A		JMP page 3	STOP TCNT		RRC A	0	1	2	ADD A,Rr 3	4	5	6	7
7	ADDC A, @Rr 0	1	JB3 addr		CALL page 3			RR A	0	1	2	ADDC A,Rr 3	4	5	6	7
8				RET	JMP page 4	EN SI			ORL Pp, # data 0	1	2					
9	OUTL PO, A		JB4 addr	RETR	CALL page 4	DIS SI	JNZ addr	CLR C	ANL Pp, # data 0	1	2		MOV Sn, # data 0	1	2	
A	MOV @Rr, A 0	1		MOVP A, @A	JMP page 5	SEL MB2		CPL C	0	1	2	MOV Rr, A 3	4	5	6	7
B	MOV @Rr, # data 0	1	JB5 addr	JMPP @A	CALL page 5	SEL MB3			0	1	2	MOV Rr, # data 3	4	5	6	7
C	DEC @Rr 0	1			JMP page 6	SEL RB0	JZ addr	MOV A, PSW	0	1	2	DEC Rr 3	4	5	6	7
D	XRL A, @Rr 0	1	JB6 addr	XRL A, # data	CALL page 6	SEL RB1		MOV PSW, A	0	1	2	XRL A, Rr 3	4	5	6	7
E	DJNZ @Rr, addr 0	1			JMP page 7	SEL MB0	JNC addr	RL A	0	1	2	DJNZ Rr, addr 3	4	5	6	7
F	MOV A, @Rr 0	1	JB7 addr		CALL page 7	SEL MB1	JC addr	RLC A	0	1	2	MOV A, Rr 3	4	5	6	7

Table 5 shows the additional MAB84X1 family instructions (including the five for serial I/O operation) that are not part of the MAB8048 instruction set.

Table 5 MAB84X1 family instructions not in the MAB8048 instruction set

serial I/O	register	control	conditional branch

MOV A, S_n
MOV S_n, A
MOV S_n, #data
EN SI
DIS SI
	DEC @Rr
	DJNZ @Rr, addr
		SEL MB2
		SEL MB3
			JNTF addr

Table 6 shows the MAB8048 instructions omitted from the MAB84X1 family instruction set.

Table 6 MAB8048 instructions not in the MAB84X1 family instruction set

data moves	flags	branch	control

MOVX A, @R
MOVX @R, A
MOVP3 A, @A
MOVD A, P
MOVD P, A
ANLD P, A
ORLD P, A
	CLR F0
	CPL F0
	CLR F1
	CPL F1
		* JNI addr
		JF0 addr
		JF1 addr
		
		* replaced by
		JT0 JNT0.
			ENT0 CLK

ABSOLUTE MAXIMUM RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Stress above those listed under 'Absolute maximum ratings' may cause permanent damage to the device. This is a stress rating only and functional operation of the device, at these, or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

parameter	symbol	min.	max.	unit
Input voltage on any pin with respect to ground (V_{SS})	V_I	−0,5	+7	V
Total power dissipation				
SOT-117, 28-lead DIL	P_{tot}	–	1	W
SOT-136, 28-lead DIL	P_{tot}	–	0,6	W
Input/output current for all pins except port 1	I_I, I_O	–	10	mA
Input/output current for port 1	I_I, I_O	–	20	mA
Storage temperature	T_{stg}	−65	+150	°C
Operating temperature				
standard	T_{amb}	0	+70	°C
extended	T_{amb}	−40	+85	°C
automotive	T_{amb}	−40	+110	°C

DC CHARACTERISTICS

V_{CC} = 5 V (10%); V_{SS} = 0 V; all voltages with respect to V_{SS} unless otherwise specified

parameter	conditions	symbol	min.	max.	unit
Supply current					
MAB	0 to + 70 °C	I_{CC}	–	85	mA
MAF	–40 to + 85 °C	I_{CC}	–	100	mA
MAF84A	–40 to + 110 °C	I_{CC}	–	100	mA
Inputs					
Input voltage LOW (except P2.3 and SCLK)		V_{IL}	–0,5	0,8	V
Input voltage LOW (P2.3 and SCLK)		V_{IL1}	–0,5	1,5	V
Input voltage HIGH (all inputs except XTAL1, P2.3 and SCLK)		V_{IH}	2	V_{CC} + 0,5	V
Input voltage HIGH (XTAL1, P2,3 and SCLK)		V_{IH1}	3,0	V_{CC} + 0,5	V
Outputs					
Output voltage LOW (P0.0–P0.7)	I_{OL} = 1,6 mA	V_{OL}	–	0,45	V
Output voltage LOW (P1.0–P1.7 for 8401/11/21/41/61)	I_{OL12} = 10 mA	V_{OL12}	–	1,0	V
Output voltage LOW (P2.0–P2.2)	I_{OL2} = 1,6 mA	V_{OL2}	–	0,45	V
Output voltage LOW (P2.3, SCLK)	I_{OL3} = 5 mA	V_{OL3}	–	0,45	V
Output voltage LOW (non-standard pins of bond-out versions)	I_{OL4} = 0,4 mA	V_{OL4}	–	0,45	V
Output voltage HIGH (all outputs unless open drain)	I_{OH} = –50 μA	V_{OH}	2,4	–	V
Output leakage current	$V_{SS} < V_I < V_{CC}$	$\pm I_{OL}$	–	10	μA

AC CHARACTERISTICS (all versions except bond-out)

V_{CC} = 5 V ± 10%; V_{SS} = 0 V.

parameter	symbol		min.	max.	unit
Frequency	f_{XTAL}	MAB/MAF84X1	1	6	MHz
		MAF84AX1	1	5	MHz
Cycle time	t_{CY}	MAB/MAF84X1	5	30	μs
		MAF84AX1	6	30	μs

AC CHARACTERISTICS (bond-out versions)

V_{CC} = 5 V ± 10%; V_{SS} = 0 V.

parameter	symbol	min.	max.	unit
f_{CL} = 6 MHz				
Control pulse duration $\overline{PSEN}$ (9CP)	t_{CC}	1,5	9	μs
Address to $\overline{PSEN}$ L set-up (1CP)	t_{AS}	167	–	ns
Data to $\overline{PSEN}$ H set-up (1CP + 120 ns)	t_{DS}	600	–	ns
Data hold time	t_{DR}	0	–	ns
Address to data-in (10CP–t_{DS})	t_{AD}	–	1,07	μs
Time from $\overline{PSEN}$ L to C1 (3CP)	t_{PC}	500	–	ns
Time from $\overline{INTA}$ L to $\overline{PSEN}$ (3CP)	t_{IP0}	500	–	ns
Time from $\overline{INTA}$ H to $\overline{PSEN}$ (6CP)	t_{IP1}	1	–	μs
$\overline{HALT}$ set-up to $\overline{PSEN}$ (15CP)	t_{HS}	2,5	–	μs
$\overline{HALT}$ hold time from $\overline{PSEN}$ (3CP)	t_{HH}	500	–	ns

Note: CP = clock pulse.

T1 ZERO-CROSS CHARACTERISTICS

T_{amb} = 0 to + 70 °C; V_{CC} = 5 V ± 10%, V_{SS} = 0 V; C_L = 80 pF

parameter	conditions	symbol	min.	max.	unit
Zero-cross detection input (T1) peak-topeak	AC coupled, C = 1,0 μF	$V_{ZX(p-p)}$	1	3	V
Zero-cross accuracy	50 Hz sine wave	A_{ZX}	–	± 135	mV
Zero-cross detection input frequency (T1)		F_{ZX}	0,05	1	kHz

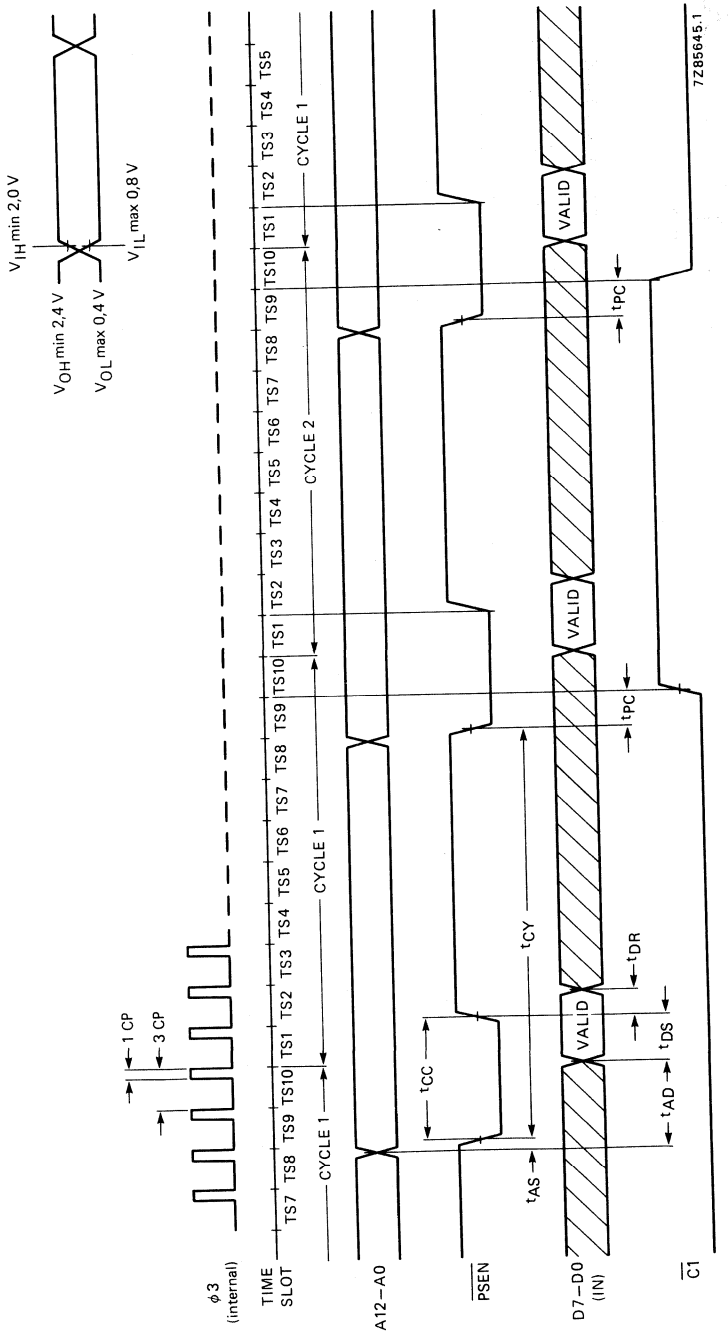


Fig. 15 Memory access timing MAB8401B/WP and I/O voltage parameters.

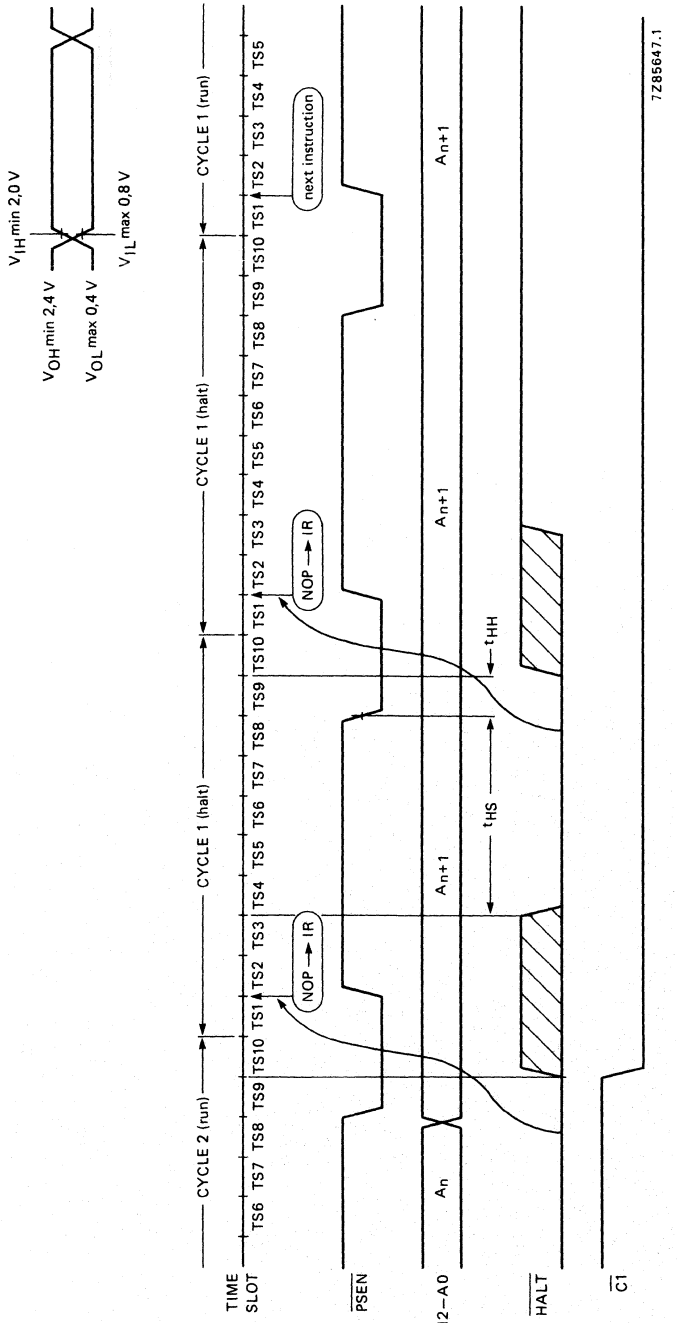


Fig. 16 $\overline{HALT}$ timing MAB8401WP and I/O voltage parameters.

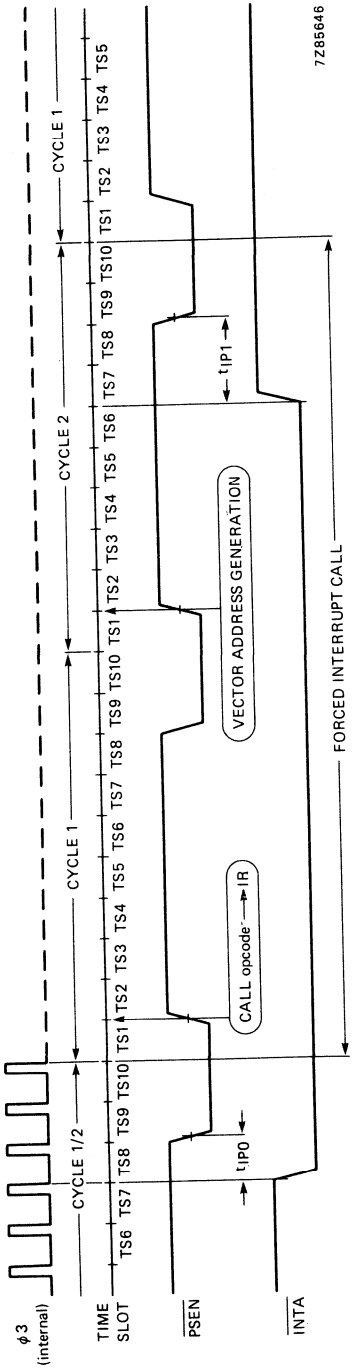


Fig. 17 $\overline{\text{INTA}}$ timing MAB8401WP.

SINGLE-CHIP 8-BIT MICROCONTROLLER

DESCRIPTION

The MAB8422/8442 is a high-performance microcontroller incorporating dedicated hardware, memory capacity and I/O lines. This dedication means a microcontroller can be economically installed in high-volume products where its main function is control.

The MAB8422/8442 is a 20 pin, single-chip 8-bit microcontroller that has been developed from the 28 pin MAB8421/8441 microcontrollers. The versions are:

- MAB8422 - 2K x 8 ROM/64 bytes RAM
- MAB8442 - 4K x 8 ROM/128 bytes RAM

Each version has 15 I/O port lines comprising one 8-bit parallel port (P0), one 2-bit parallel port (P1.0 and P1.1 that are shared with the serial I/O lines SDA and SCL), one 3-bit parallel port (P2.0 - P2.2) and two input lines ($\overline{INT}$/T0 and T1).

The serial I/O interface is I^2C compatible and therefore the MAB8422/8442 can operate as a slave or a master in single and multi-master systems. Conversion from parallel to serial data when transmitting, and vice versa when receiving, is done mainly in software. There is a minimum of hardware for the serial I/O implemented. This hardware is controlled by the status of the SDA and SCL lines and can be read or written under software control. Standard software for I^2C-bus control is available upon request. For detailed information see the user manual 'Single-chip 8-bit microcontrollers'.

Features

- 8-bit: CPU, ROM, RAM and I/O
- 20 pin package
- MAB8422: 2K x 8 ROM/64 bytes RAM
- MAB8442: 4K x 8 ROM/128 bytes RAM
- 13 quasi-bidirectional I/O port lines
- Two testable inputs T1 and $\overline{INT}$/T0
- High current output on P0 (I_{OL} = 10 mA at V_{OL} = 1 V)
- One interrupt line combined with the testable input line $\overline{INT}$/T0
- Single-level interrupts: external, timer/event counter, serial I/O
- I^2C-compatible serial I/O that can be used in single or multi-master systems (serial I/O data and clock via P1.0 and P1.1 port lines, respectively)
- 8-bit programmable timer/event counter
- Internal oscillator, generated with inductor, crystal, ceramic resonator or external source
- Over 80 instructions (based on MAB8048)
- All instructions 1 or 2 cycles, cycle time dependent on oscillator frequency
- Single power supply
- Operating temperature ranges: 0 to +70 °C (MAB84X2)
  −40 to +85 °C (MAF84X2)
  −40 to +110 °C (MAF84AX2)

PACKAGE OUTLINES

MAB/MAF84X2, MAF84AX2: 20-lead DIL; plastic (SOT-146).

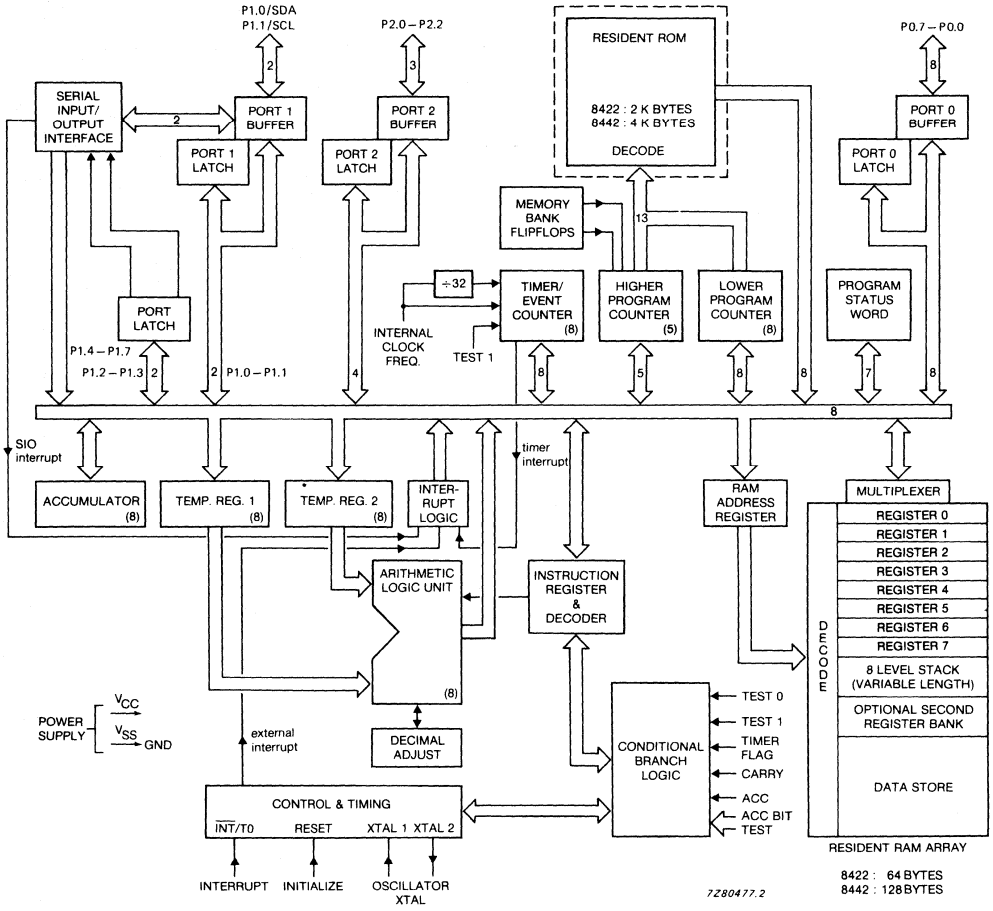


Fig. 1 Block diagram of the MAB8422/8442.

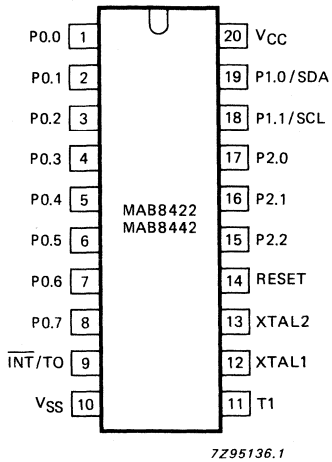


Fig. 2 Pinning diagram.

PINNING

Designation	Pin number	Function
P0.0 - P0.7	1-8	8-bit quasi-bidirectional I/O port (Port 0 high current output).
$\overline{INT}$/T0	9	External interrupt input (sensitive to a negative going edge) and/or input, testable using the JT0 or JNT0 instructions.
V_{SS}	10	Ground.
T1	11	Input pin, testable using the JT1 or JNT1 instructions. It can be designated as event counter input using the STRT CNT instruction. It can also be used to detect zero cross-over of slowly moving a.c. inputs.
XTAL1	12	Connection to timing component that determines the frequency of the internal oscillator. It is also the input for an external clock source.
XTAL2	13	Connection to the other side of the timing component.
RESET	14	Input to initialize the processor (active HIGH).
P2.0-P2.2	17-15	Quasi-bidirectional port.
P1.1/SCL	18	Quasi-bidirectional port in parallel port mode. Serial clock in serial I/O mode.
P1.0/SDA	19	Quasi-bidirectional port in parallel port mode. Serial data I/O in serial I/O mode.
V_{CC}	20	Power supply.

FUNCTIONAL DESCRIPTION

Program and data memory

The non-volatile program memory (ROM), as shown in Fig. 3, is arranged in two banks of 2K bytes, that are selected by SEL MB instructions, and each bank is further divided into 256-byte pages. Only the unconditional jump instructions (JMP and CALL) can be used to cross page boundaries. Memory bank boundaries can also be crossed using these instructions provided that the appropriate memory bank has been selected.

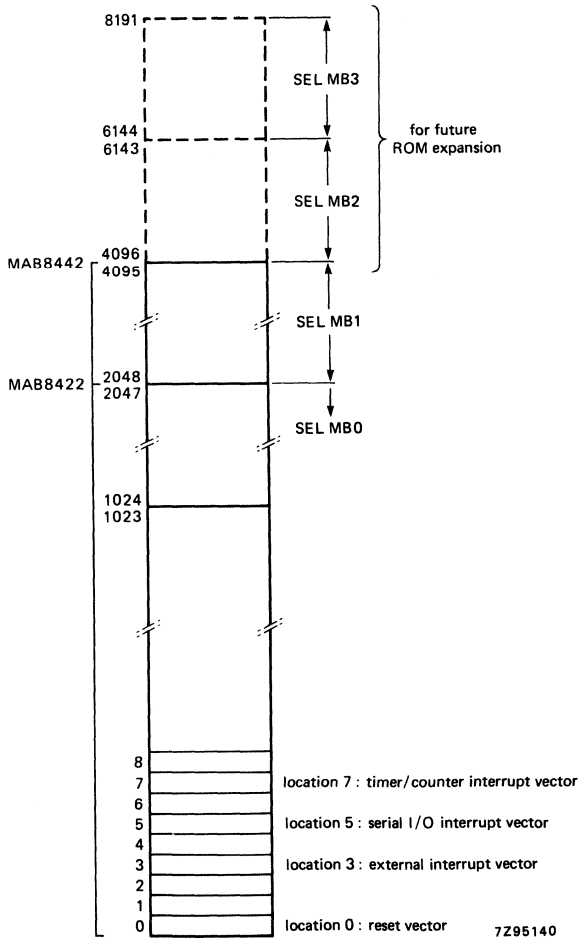


Fig. 3 Program memory map.

In the volatile data memory (RAM), all locations are indirectly addressable using RAM pointer registers and up to 16 designated locations can be addressed directly. The memory also includes an 8-level program counter stack addressed by a 3-bit stack pointer and two register banks, each with 8 registers. The data memory is shown in Fig. 4.

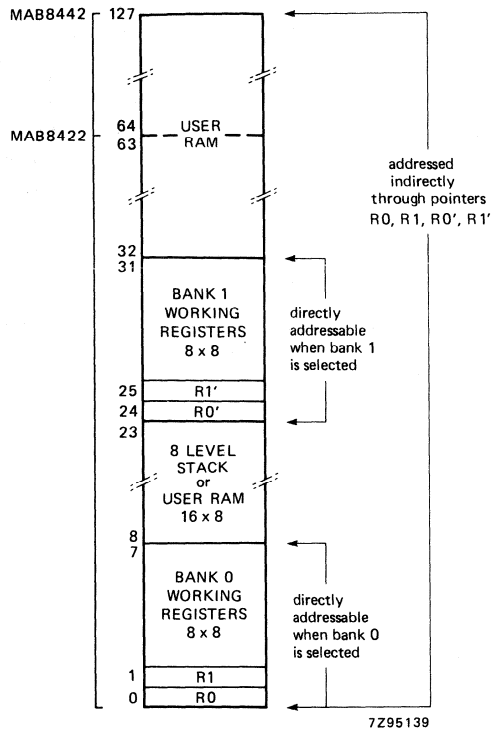


Fig. 4 Data memory map.

Instruction set

The instruction set consists of over 80 one and two byte instructions. It is identical to the MAB84X1 instruction set except that the instructions MOV Sn, A, MOV A, Sn and MOV Sn, #data are not used. Program code efficiency is high because all RAM locations on a 256 byte page require only a single byte address.

On-chip peripheral functions

In addition to the CPU and memories, an interrupt system, I/O facilities, and an 8-bit timer/event counter are integrated on-chip to assist the CPU in repetitious, complicated or time-critical tasks. The I/O facilities include the I/O pins, parallel ports and a serial I/O port sharing the two pins of the parallel port P1.

FUNCTIONAL DESCRIPTION (continued)

I/O facilities (see Fig. 5)

The MAB8422/8442 has 13 I/O lines and 2 testable inputs arranged as:

- An 8 line parallel port P0.0-P0.7, high current outputs with three optional output configurations:
  - A push-pull output with pull-up (Fig. 5 (a))
  - Open drain with pull-up (Fig. 5 (b))
  - Open drain without pull-up (Fig. 5 (c))
- A 2 line parallel/serial port P1.0/SDA and P1.1/SCL, open-drain without pull-up, as output configuration. Schmitt-trigger input. After RESET, P1.0/SDA and P1.1/SCL will be in the parallel port mode. To stay in this mode the internal port latches, P1.4 and P1.3 must be kept in the logic '1' state. Inputs P1.2-P1.7 are not valid in the parallel port mode. After a RESET, the microcontroller remains in the parallel port mode until the serial I/O mode is enabled.
- A 3 line parallel port P2.0-P2.2 with the same output configurations as P0.0-P0.7 but without high-current output;
- An external interrupt and test input INT/T0, which when used as a test input can be tested by the conditional jump instructions JT0 and JNT0;
- A test input T1, tested by the conditional jump instructions JT1 and JNT1. T1 can also be used as an input to the timer/event counter or to detect zero cross-over of slowly moving AC signals. This test or input line can be ordered with port option 5(b) or 5(c).

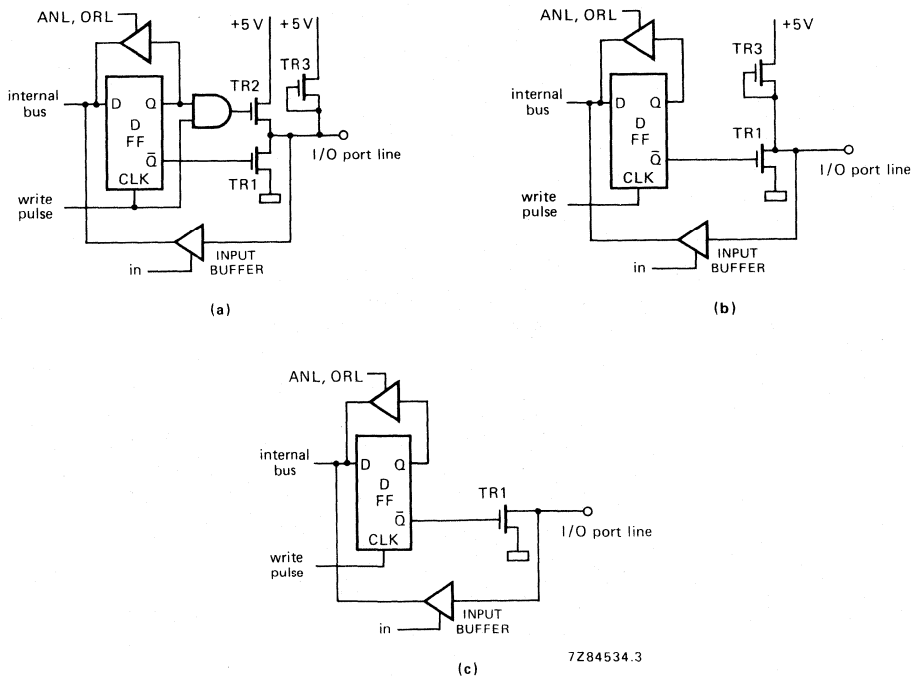


Fig. 5 Port option configurations.

Test input T1

The T1 input line can be used as:

- a test input for branch instructions,
- an input for zero voltage cross-over detection,
- an external input to the event counter.

An internal pull-up transistor is provided as a ROM mask option. This is useful when the input is from a switch or standard TTL output.

When T1 is used as a test input, the JT1 or JNT1 instructions test for a HIGH or a LOW respectively.

Zero cross-over detection

When used for zero-cross detection purposes, the T1 input must be coupled through a capacitor of typical value 1 μF and operation carried out using the T1 input without the pull-up transistor. The maximum input voltage amplitude is 3 V (peak-to-peak), with a maximum operational frequency of 1 kHz. The T1 input has an on-chip DC offset circuit which self-biases the input near to its exact switching level of 1 V. As a consequence a small change will cause a digital transition to occur. The switching level of the T1 input circuit is within the bias voltage of ±135 mV. Upon each positive cycle on the pin, the event counter is incremented and an overflow will set the timer flag TF. Zero cross-over detection used in conjunction with the timer/event counter interrupt, is useful in thyristor control of power equipment. Figure 6 illustrates, (a) the input waveform, (b) the input diagram and (c) the on-chip self-stabilized bias.

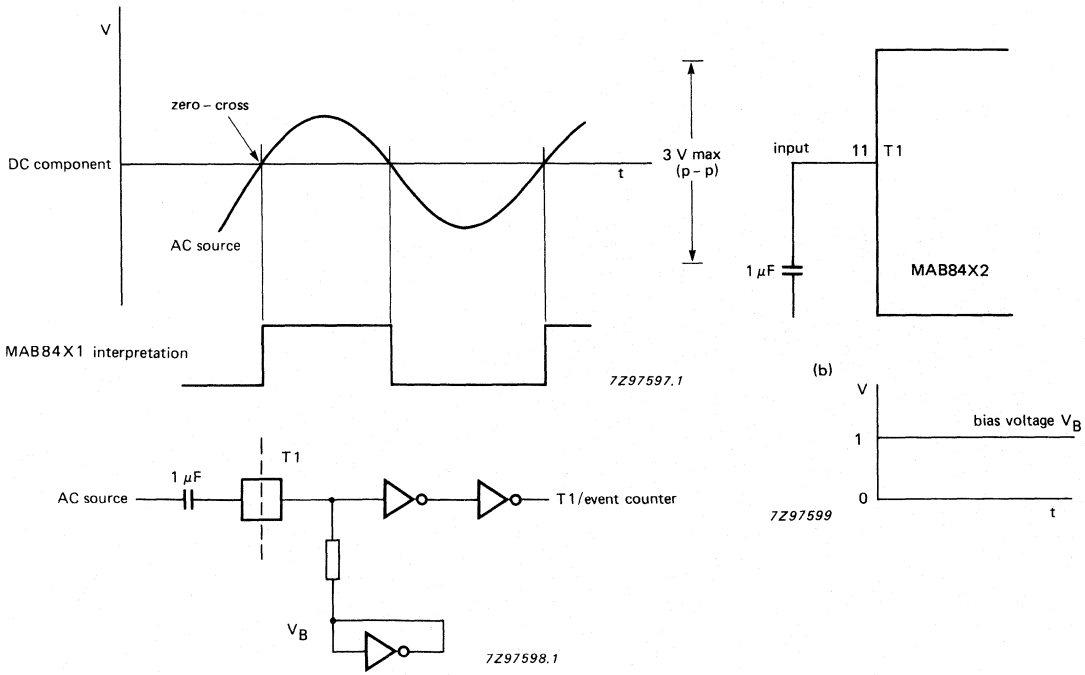


Fig. 6 Zero-cross voltage detection circuitry.

FUNCTIONAL DESCRIPTION (continued)

Timer/event counter

An 8-bit binary up-counter is provided. This can count external events, modulo-32 machine cycles, or machine cycles directly. When used as a timer, the input to the counter is either the overflow or input of a 5-bit prescaler. When used as an event counter, LOW to HIGH transitions on T1 (pin 13) are counted. The maximum rate at which the counter may be incremented is once every machine cycle (200 kHz for a 5 μs machine cycle). Fig. 7 illustrates the timer/event counter.

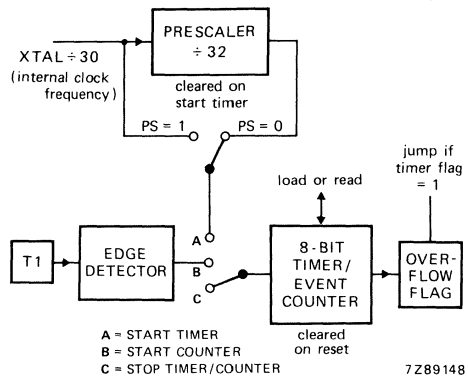


Fig. 7 Timer/event counter.

Interrupt system

External events and real-time on-chip peripherals require servicing by the CPU asynchronous to the execution of any particular section of code. To tie the asynchronous activities of these functions to normal program execution a multiple-source, single-level nested interrupt system is provided.

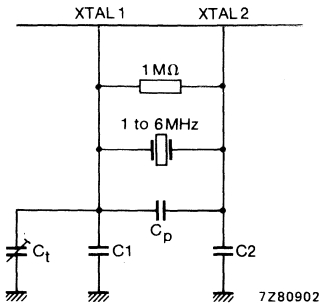
The MAB8422/8442 handles interrupts from three sources as follows:

- $\overline{\text{INT}}$/T0; externally via pin 9
- $\overline{\text{SIOINT}}$; from the internal serial I/O port
- TCNT interrupt; from the internal timer/event counter.

Each interrupt vectors to a separate location in the program memory for its service program. Each source can be individually enabled or disabled. When more than one interrupt occurs simultaneously, their priority will be: (1) external, (2) serial I/O and, (3) timer/event counter. An additional external interrupt can be created using the timer/event counter interrupt.

OSCILLATOR CIRCUITRY (see Fig. 8)

The clock frequency is determined by using the internal oscillator or by connecting an external clock to XTAL1. Where the internal oscillator is used the frequency is set by a crystal, a ceramic resonator or an inductor (each with associated capacitors) between XTAL1 and XTAL2. A machine cycle consists of 10 states, each state being 3 oscillator periods. The MAB8422/8442 has a dynamic logic, and therefore, for adequate refreshing the oscillator frequency must be at least 1 MHz.



1. Crystal - AT-cut
2. Ceramic resonator
   $C_1 = C_2 = 27$ pF
   C_t is optional
   $C_p < 6{,}75$ pF (parasitic capacitance)

Fig. 8(a) Quartz crystal or ceramic resonator mode.

If the frequency has to be trimmed, then a trimmer capacitor C_t should be connected in parallel with the fixed capacitor C_1.

Table 1 shows the LC values for timing generation with the LC oscillator.

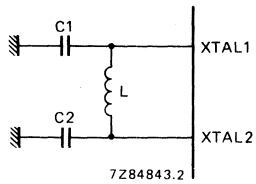
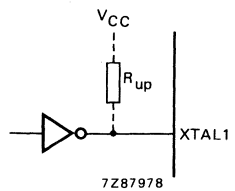


Fig. 8(b) LC pi-network.

Table 1 LC oscillator timing

frequency	C1 = C2	L
3,0 MHz	33 pF	100 μH
4,0 MHz	33 pF	56 μH
4,4 MHz	33 pF	47 μH
5,0 MHz	33 pF	33 μH
6,0 MHz	33 pF	22 μH



Drive XTAL1
Leave XTAL2 open

Driver may be high-speed CMOS or any TTL
t_r, $t_f < 10$ ns

Fig. 9 External drive.

RESET

A positive-going signal on the RESET input:

- sets the program counter to zero,
- selects location 0 of memory bank 0, and register bank 0,
- sets the stack pointer to zero (000); pointing to RAM address 8,
- disables the interrupts (external), timer and serial I/O),
- stops the timer/event counter, then sets it to zero,
- sets the timer prescaler to modulo-32,
- resets the timer flag,
- sets all ports to logic '1' (input mode),
- sets ports P1.0/SDA and P1.1/SCL to the parallel part mode and disables the serial I/O.

Automatic reset at power-up may be obtained by connecting the RESET pin to V_{CC} through a 1 μF capacitor C1, together with a diode to V_{SS} (cathode to RESET pin). This arrangement is satisfactory, if both the voltage (V_{CC}) rise time and the oscillator start-up time do not exceed either 1 or 10 ms respectively.

The power-on reset circuit is shown in Fig. 11; the input characteristics are shown in Fig. 12. At power-on the current drawn by RESET commences to charge the capacitor C1. The difference between this increasing capacitor voltage and V_{CC} is known as V_{RESET}. The charging circuit is designed to hold V_{RESET} above the lower threshold of a schmitt trigger arrangement, long enough to effect a complete reset. The minimum time required is the oscillator start-up time, plus two machine cycles.

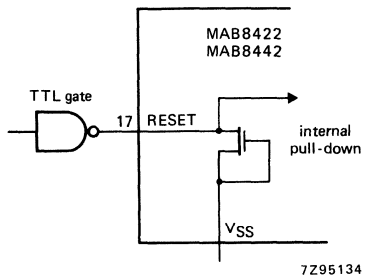


Fig. 10 External reset.

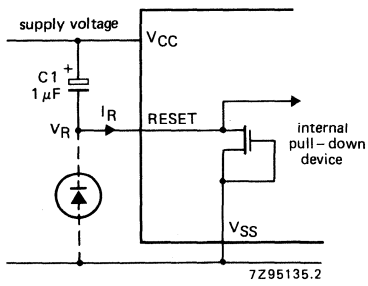


Fig. 11 Power-on reset circuitry.

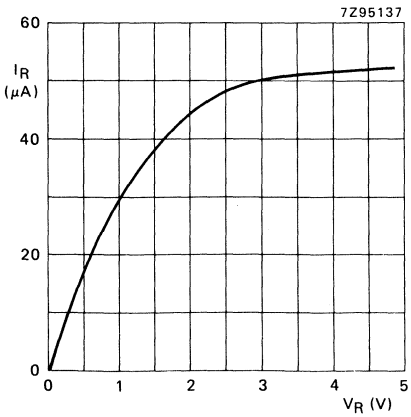


Fig. 12 Power-on reset input characteristics.

INSTRUCTION SET

The instruction set consists of over 80 one and two byte instructions and is based on the MAB8048 instruction set. New instructions include those for serial I/O operation and memory bank selection. Program code efficiency is high because all ROM locations on a 256 byte page require only a single byte address.

Table 2 gives the instruction set of the MAB84X2 family and Table 3 shows the instruction map. The following symbols and abbreviations are used.

symbol	description
A	the accumulator
AC	the auxiliary carry flag
addr	program memory address (11-bits)
Bb	bit designation (b = 0–7)
BS	the bank switch
C	carry flag
CLK	clock signal
CNT	event counter
D	nibble designation (4-bits)
DBF	program memory bank flip-flop
data	number of expression (8-bits)
F0, F1	flags 0 and 1
I	interrupt
$\overline{\text{INT}}$	external interrupt
P	'in-page' operation designation
Pp	port designation (p = 1, 2 or 4–7)
PSW	program status word
Rr	register designation (r = 0, 1 or 0–7)
SP	stack pointer
T	timer
TF	timer flag
T0, T1	test 0 an 1 inputs
#	immediate data prefix
@	indirect address prefix
S	current value of program counter
←	is replaced by
↔	is exchanged with

Table 2 Instruction set

	mnemonic	opcode (hex.)	bytes/ cycles	description	function		notes
ACCUMULATOR	ADD A, Rr	6*	1/1	Add register contents to A	(A)←(A) + (Rr)	r = 0–7	1
	ADD A, @Rr	60 61	1/1	Add RAM data, addressed by Rr, to A	(A)←(A) + ((R0)) (A)←(A) + ((R1))		1
	ADD A, #data	03 data	2/2	Add immediate data to A	(A)←(A) + data		1
	ADDC A, Rr	7*	1/1	Add carry and register contents to A	(A)←(A) + (Rr) + (C)	r = 0–7	1
	ADDC A, @Rr	70 71	1/1	Add carry and RAM data, addressed by Rr, to A	(A)←(A) + ((R0)) + (C) (A)←(A) + ((R1)) + (C)		1
	ADDC A, #data	13 data	2/2	Add carry and immediate data to A	(A)←(A) + data + (C)		1
	ANL A, Rr	5*	1/1	'AND' Rr with A	(A)←(A) AND (Rr)	r = 0–7	
	ANL A, @Rr	50 51	1/1	'AND' RAM data, addressed by Rr, with A	(A)←(A) AND ((R0)) (A)←(A) AND ((R1))		
	ANL A, #data	53 data	2/2	'AND' immediate data with A	(A)←(A) AND data		
	ORL A, Rr	4*	1/1	'OR' Rr with A	(A)←(A) OR (Rr)	r = 0–7	
	ORL A, @Rr	40 41	1/1	'OR' RAM data, addressed by Rr, with A	(A)←(A) OR ((R0)) (A)←(A) OR ((R1))		
	ORL A, #data	43 data	2/2	'OR' immediate data with A	(A)←(A) OR data		
	XRL A, Rr	D*	1/1	'XOR' Rr with A	(A)←(A) XOR (Rr)	r = 0–7	
	XRL A, @Rr	D0 D1	1/1	'XOR' RAM, addressed by Rr, with A	(A)←(A) XOR ((R0)) (A)←(A) XOR ((R1))		
	XRL A, #data	D3 data	2/2	'XOR' immediate data with A	(A)←(A) XOR data		
	INC A	17	1/1	increment A by 1	(A)←(A) + 1		
	DEC A	07	1/1	decrement A by 1	(A)←(A) −1		
	CLR A	27	1/1	clear A to zero	(A)←0		
	CPL A	37	1/1	one's complement A	(A)←NOT(A)		
	RL A	E7	1/1	rotate A left	$(A_{n+1})\leftarrow(A_n)$ $(A_0)\leftarrow(A_7)$	n = 0–6	

	mnemonic	opcode (hex.)	bytes/ cycles	description	function		notes
ACCUMULATOR (cont.)	RLC A	F7	1/1	rotate A left through carry	$(A_{n+1}) \leftarrow A_n$ $(A_0) \leftarrow (C), (C) \leftarrow (A_7)$	n = 0–6	2
	RR A	77	1/1	rotate A right	$(A_n) \leftarrow (A_{n+1})$ $(A_7) \leftarrow (A_0)$	n = 0–6	
	RRC A	67	1/1	rotate A right through carry	$(A_n) \leftarrow (A_{n+1})$ $(A_7) \leftarrow (C), (C) \leftarrow (A_0)$	n = 0–6	2
	DA A	57	1/1	decimal adjust A			2
	SWAP A	47	1/1	swap nibbles of A	$(A_{4-7}) \leftrightarrow (A_{0-3})$		
DATA MOVES	MOV A, Rr	F*	1/1	move register contents to A	(A)←(Rr)	r = 0–7	
	MOV A, @Rr	F0 F1	1/1	move RAM data, addressed by Rr, to A	(A)←((R0)) (A)←((R1))		
	MOV A, #data	23 data	2/2	move immediate data to A	(A)←data		
	MOV Rr, A	A*	1/1	move accumulator contents to register	(Rr)←(A)	r = 0–7	
	MOV @Rr, A	A0 A1	1/1	move accumulator contents to RAM location addressed by Rr	((R0))←(A) ((R1))←(A)		
	MOV Rr, #data	B* data	2/2	move immediate data to Rr	(Rr)←data		
	MOV @Rr, #data	B0 data B1 data	2/2	move immediate data to RAM location addressed by Rr	((R0))←data ((R1))←data		
	XCH A, Rr	2*	1/1	exchange accumulator contents with Rr	(A)↔(Rr)	r = 0–7	
	XCH A, @Rr	20 21	1/1	exchange accumulator contents with RAM data addressed by Rr	(A)↔((R0)) (A)↔((R1))		
	XCHD A, @Rr	30 31	1/1	exchange lower nibbles of A and RAM data addressed by Rr	$(A_{0-3}) \leftrightarrow ((R0_{0-3}))$ $(A_{0-3}) \leftrightarrow ((R1_{0-3}))$		
	MOV A, PSW	C7	1/1	move PSW contents to accumulator	(A)←(PSW)		
	MOV PSW, A	D7	1/1	move accumulator bit 3 to PSW_3	$(PSW_3) \leftarrow (A_3)$		3
	MOVP A, @A	A3	1/2	move indirectly addressed data in current page to A	$(PC_{0-7}) \leftarrow (A), (A) \leftarrow ((PC))$		

Table 2 Instruction set (continued)

FLAGS	CLR C	97	1/1	clear carry bit	(C)←0	2
	CPL C	A7	1/1	complement carry bit	(C)←NOT(C)	2
REGISTER	INC Rr	1*	1/1	increment register by 1	(Rr)←(Rr) + 1 r = 0–7	
	INC @Rr	10 11	1/1	increment RAM data, addressed by Rr, by 1	((R0))←((R0)) + 1 ((R1))←((R1)) + 1	
	DEC Rr	C*	1/1	decrement register by 1	(Rr)←(Rr) – 1 r = 0–7	
	DEC @Rr	C0 C1	1/1	decrement RAM data, addressed by Rr, by 1	((R0))←((R0)) – 1 ((R1))←((R1)) – 1	
BRANCH	JMP addr	• 4 address	2/2	unconditional jump within a 2 K bank	(PC_{8-10})←$addr_{8-10}$ (PC_{0-7})←$addr_{0-7}$ (PC_{11-12})←MBFF 0–1	
	JMPP @A	B3	1/2	indirect jump within a page	(PC_{0-7})←((A))	
	DJNZ Rr, addr	E* address	2/2	decrement Rr by 1 and jump if not zero to addr	(Rr)←(Rr) – 1 r = 0–7 if (Rr) not zero (PC_{0-7})←addr	
	DJNZ @Rr, addr	E0 address	2/2	decrement RAM data, addressed by Rr by 1 and jump if not zero to addr	((R0))←((R0)) – 1 if ((R0)) not zero (PC_{0-7})←addr	
		E1 address			((R1))←((R1)) – 1 if ((R1)) not zero (PC_{0-7})←addr	
	JBb addr	▲ 2 address	2/2	jump to addr if Acc. bit b = 1	if b = 1 : (PC_{0-7})←addr b = 0–7	
	JC addr	F6 address	2/2	jump to addr if C = 1	if C = 1 : (PC_{0-7})←addr	
	JNC addr	E6 address	2/2	jump to addr if C = 0	if C = 0 : (PC_{0-7})←addr	
	JZ addr	C6 address	2/2	jump to addr if A = 0	if A = 0 : (PC_{0-7})←addr	
	JNZ addr	96 address	2/2	jump to addr if A is NOT zero	if A ≠ 0 : (PC_{0-7})←addr	
	JT0 addr	36 address	2/2	jump to addr if T0 = 1	if T0 = 1: (PC_{0-7})←addr	
	JNT0 addr	26 address	2/2	jump to addr if T0 = 0	if T0 = 0: (PC_{0-7})←addr	
	JT1 addr	56 address	2/2	jump to addr if T1 = 1	if T1 = 1: (PC_{0-7})←addr	
	JNT1 addr	46 address	2/2	jump to addr if T1 = 0	if T1 = 0: (PC_{0-7})←addr	
	JTF addr	16 address	2/2	jump to addr if Timer Flag = 1	if TF = 1: (PC_{0-7})←addr	4
	JNTF addr	06 address	2/2	jump to addr if Timer Flag = 0	if TF = 0: (PC_{0-7})←addr	

	mnemonic	opcode (hex.)	bytes/ cycles	description	function	notes
TIMER/EVENT COUNTER	MOV A, T	42	1/1	move timer/event counter contents to accumulator	(A)←(T)	
	MOV T, A	62	1/1	move accumulator contents to timer/event counter	(T)←(A)	
	STRT CNT	45	1/1	start event counter		
	STRT T	55	1/1	start timer		
	STOP TCNT	65	1/1	stop timer/event counter		
	EN TCNTI	25	1/1	enable timer/event counter interrupt		
	DIS TCNTI	35	1/1	disable timer/event counter interrupt		
CONTROL	EN I	05	1/1	enable external interrupt		
	DIS I	15	1/1	disable external interrupt		
	SEL RB0	C5	1/1	select register bank 0	(RBS)←0	5
	SEL RB1	D5	1/1	select register bank 1	(RBS)←1	5
	SEL MB0	E5	1/1	select program memory bank 0	(MBFF0)←0, (MBFF1)←0	
	SEL MB1	F5	1/1	select program memory bank 1	(MBFF0)←1, (MBFF1)←0	
	SEL MB2	A5	1/1	select program memory bank 2	(MBFF0)←0, (MBFF1)←1	
	SEL MB3	B5	1/1	select program memory bank 3	(MBFF0)←1, (MBFF1)←1	
SUBROUTINE	CALL addr	▲ 4 address	2/2	jump to subroutine	((SP))←(PC), ($PSW_{4, 6, 7}$) (SP)←(SP) + 1 (PC_{8-10})←$addr_{8-10}$ (PC_{0-7})←$addr_{0-7}$ (PC_{11-12})←MBFF 0–1	6
	RET	83	1/2	return from subroutine	(SP)←(SP) – 1 (PC)←((SP))	6
	RETR	93	1/2	return from interrupt and restore bits 4, 6, 7 of PSW	(SP)←(SP) – 1 ($PSW_{4, 6, 7}$) + (PC)←((SP))	6

Table 2 Instruction set (continued)

PARALLEL INPUT/OUTPUT	IN A, Pp	08 09 0A	1/2	input port p data to accumulator	(A)←(P0) (A)←(P1) (A)←(P2)	7
	OUTL Pp, A	38 39 3A	1/2	output accumulator data to port p	(P0)←(A) (P1)←(A) (P2)←(A)	
	ANL Pp, #data	98 data 99 data 9A data	2/2	AND port p data with immediate data	(P0)←(P0) AND data (P1)←(P1) AND data (P2)←(P2) AND data	
	ORL Pp, #data	88 data 89 data 8A data	2/2	OR port p data with immediate data	(P0)←(P0) OR data (P1)←(P1) OR data (P2)←(P2) OR data	
	OUTL PO,A	90	1/2	Output accumulator data to port ϕ	(P0)←(A)	8
SERIAL INPUT/OUTPUT	EN SI	85	1/1	enable serial I/O interrupt		
	DIS SI	95	1/1	disable serial I/O interrupt		
	NOP	00	1/1	no operation		

Notes to Table 2.

1. PSW CY, AC affected
2. PSW CY affected
3. PSW PS affected
4. Execution of JTF and JNTF instructions resets the Timer Flag (TF).
5. PSW RBS affected
6. PSW SP_0, SP_1, SP_2 affected
7. (A) = 1111 P2.3, P2.2, P2.1, P2.0.
8. Only for software-transfer from the MAB8021.

* : 8, 9, A, B, C, D, E, F
● : 0, 2, 4, 6, 8, A, C, E
▲ : 1, 3, 5, 7, 9, B, D, F

TABLE 3 MAB8422/8442 INSTRUCTION MAP

first hexadecimal character of opcode ↓

second hexadecimal character of opcode →

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	NOP			ADD A, # data	JMP page 0	EN I	JNTF addr	DEC A	IN A,Pp 0	1	2					
1	INC ∂Rr 0	1	JB0 addr	ADDC A, # data	CALL page 0	DIS I	JTF addr	INC A	0	1	2	INC Rr 3	4	5	6	7
2	XCH A, ∂Rr 0	1		MOV A, # data	JMP page 1	EN TCNTI	JNT0 addr	CLR A	0	1	2	XCH A,Rr 3	4	5	6	7
3	XCHD A,∂Rr 0	1	JB1 addr		CALL page 1	DIS TCNTI	JT0 addr	CPL A	OUTL Pp,A 0	1	2					
4	ORL A, ∂Rr 0	1	MOV A, T	ORL A, # data	JMP page 2	STRT CNT	JNT1 addr	SWAP A	0	1	2	ORL A,Rr 3	4	5	6	7
5	ANL A, ∂Rr 0	1	JB2 addr	ANL A, # data	CALL page 2	STRT T	JT1 addr	DA A	0	1	2	ANL A,Rr 3	4	5	6	7
6	ADD A, ∂Rr 0	1	MOV T, A		JMP page 3	STOP TCNT		RRC A	0	1	2	ADD A,Rr 3	4	5	6	7
7	ADDC A, ∂Rr 0	1	JB3 addr		CALL page 3			RR A	0	1	2	ADDC A,Rr 3	4	5	6	7
8				RET	JMP page 4	EN SI			ORL Pp,# data 0	1	2					
9	OUTL PO, A		JB4 addr	RETR	CALL page 4	DIS SI	JNZ addr	CLR C	ANL Pp,# data 0	1	2					
A	MOV ∂Rr, A 0	1		MOVP A, ∂A	JMP page 5	SEL MB2		CPL C	0	1	2	MOV Rr, A 3	4	5	6	7
B	MOV ∂Rr, # data 0	1	JB5 addr	JMPP ∂A	CALL page 5	SEL MB3			0	1	2	MOV Rr, # data 3	4	5	6	7
C	DEC ∂Rr 0	1			JMP page 6	SEL RB0	JZ addr	MOV A, PSW	0	1	2	DEC Rr 33	4	5	6	7
D	XRL A, ∂Rr 0	1	JB6 addr	XRL A, # data	CALL page 6	SEL RB1		MOV PSW, A	0	1	2	XRL A,Rr 3	4	5	6	7
E	DJNZ ∂Rr, addr 0	1			JMP page 7	SEL MB0	JNC addr	RL A	0	1	2	DJNZ Rr, addr 3	4	5	6	7
F	MOV A, ∂Rr 0	1	JB7 addr		CALL page 7	SEL MB1	JC addr	RLC A	0	1	2	MOV A, Rr 3	4	5	6	7

ABSOLUTE MAXIMUM RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Input voltage on any pin with respect to ground (V_{SS})	V_I	−0,5	+7	V
Total power dissipation	P_{tot}	–	1	W
Input/output current for all pins except port 0	I_I, I_O	–	10	mA
Input/output current for port 0	I_I, I_O	–	20	mA
Storage temperature	T_{stg}	−65	+150	°C
Operating temperature				
standard	T_{amb}	0	+70	°C
extended	T_{amb}	−40	+85	°C
automotive	T_{amb}	−40	+110	°C

DC CHARACTERISTICS

V_{CC} = 5 V (± 10%); V_{SS} = 0 V

parameter	conditions	symbol	min.	max.	unit
Supply current					
MAB8422/42	at 0 °C	I_{CC}	–	70	mA
MAF8422/42	at −40 °C	I_{CC}	–	90	mA
MAF84A22/42	at −40 °C	I_{CC}	–	90	mA
Inputs					
Input voltage LOW (except P1.0/SDA and P1.1/SCL)		V_{IL}	−0,5	0,8	V
Input voltage LOW (P1.0/SDA and P1.1/SCL)		V_{IL1}	−0,5	1,5	V
Input voltage HIGH all inputs except XTAL1, P1.0/SDA and P1.1/SCL		V_{IH}	2,0	V_{CC} + 0,5	V
Input voltage HIGH to XTAL1, P1.0/SDA and P1.1/SCL		V_{IH1}	3,0	V_{CC} + 0,5	V
Outputs					
Output voltage LOW (P0 only)	I_{OL} = 10 mA	V_{OL}		1,0	V
Output voltage LOW (P1.0/SDA and P1.1/SCL)	I_{OL} = 5 mA	V_{OL1}		0,45	V
Output voltage LOW (P0 and P2)	I_{OL} = 1,6 mA	V_{OL2}		0,45	V
Output voltage HIGH (all outputs unless open-drain)	I_{OH} = −50 μA	V_{OH}	2,4		V
Output leakage current	$V_{CC} > V_I > V_{SS}$	± I_{OL}		10	μA

AC CHARACTERISTICS

parameter	symbol	min.	max.	unit
Frequency				
MAB/MAF8422/42	f_{XTAL}	1	6	MHz
MAF84A22/42	f_{XTAL}	1	5	MHz
Cycle time				
MAB/MAF8422/42	t_{CY}	5	30	μs
MAF84A22/42	t_{CY}	6	30	μs

T1 ZERO-CROSS CHARACTERISTICS

T_{amb} = 0 to + 70 °C; V_{CC} = 5 V ± 10%; V_{SS} = 0 V; C_L = 80 pF

parameter	conditions	symbol	min.	max.	unit
Zero-cross detection input (T1) peak-to-peak	AC coupled, C = 1 μF	$V_{ZX(p-p)}$	1	3	V
Zero-cross accuracy	50 Hz sine wave	A_{ZX}	–	± 135	mV
Zero-cross detection input frequency (T1)		F_{ZX}	0,05	1	kHz

SINGLE-CHIP 8-BIT MICROCONTROLLER

GENERAL DESCRIPTION

The PCB83C552 single-chip 8-bit microcontroller is manufactured in an advanced CMOS process and is a derivative of the PCB80C51 microcontroller family. The PCB83C552 has the same instruction set as the PCB80C51. Two versions of the derivative exist although the generic term "PCB83C552" is used to refer to both family members:

- PCB83C552: 8 K bytes mask-programmable ROM, 256 bytes RAM
- PCB80C552: ROM-less version of the PCB83C552

This I/O intensive device provides architectural enhancements to function as a controller in the field of automotive electronics, specifically engine management and gear box control.

The PCB83C552 contains a non-volatile 8 K x 8 read-only program memory, a volatile 256 x 8 read/write data memory, six 8-bit I/O ports, two 16-bit timer/event counters (identical to the timers of the 80C51), an additional 16-bit timer coupled to capture and compare latches, a fifteen-source, two-priority-level, nested interrupt structure, an 8-input ADC, a dual DAC pulse width modulated interface, two serial interfaces (UART and I^2C-bus), a 'watchdog' timer and on-chip oscillator and timing circuits. For systems that require extra capability, the PCB83C552 can be expanded using standard TTL compatible memories and logic.

The device also functions as an arithmetic processor having facilities for both binary and BCD arithmetic plus bit-handling capabilities. The instruction set consists of over 100 instructions: 49 one-byte, 45 two-byte and 17 three-byte. With a 12 MHz crystal, 58% of the instructions are executed in 1 μs and 40% in 2 μs. Multiply and divide instructions require 4 μs.

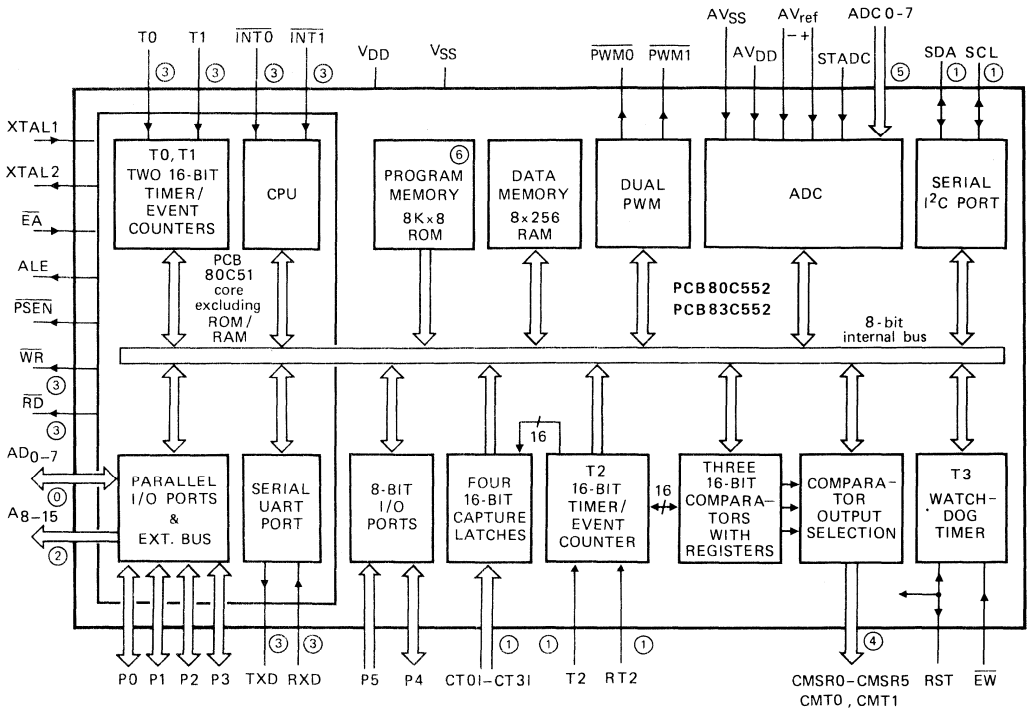
Features

- 80C51 central processing unit
- 8 K x 8 ROM, expandable externally to 64 K bytes
- 256 x 8 RAM, expandable externally to 64 K bytes
- Two standard 16-bit timer/counters
- An additional 16-bit timer/counter coupled to four capture registers and three compare registers
- A 10-bit ADC with 8 multiplexed analogue inputs
- Two 8-bit resolution, Pulse Width Modulated outputs
- Five 8-bit I/O ports plus one 8-bit input port shared with analogue inputs
- I^2C-bus serial I/O port with byte orientated master and slave functions
- Full-duplex UART compatible with the standard PCB80C51
- On-chip watchdog timer

- **A version for extended temperature range is in preparation**

PACKAGE OUTLINE

PCB83C552, PCB80C552: 68-lead PLCC; plastic, leaded-chip-carrier (SOT-188).



⓪ alternative function of port 0
① alternative function of port 1
② alternative function of port 2
③ alternative function of port 3
④ alternative function of port 4
⑤ alternative function of port 5
⑥ not present in PCB80C552

7Z97647.3

POWER SUPPLY
V_{DD} + 5 V MAIN SUPPLY
V_{SS} GROUND

Fig. 1 Block diagram.

DEVELOPMENT DATA

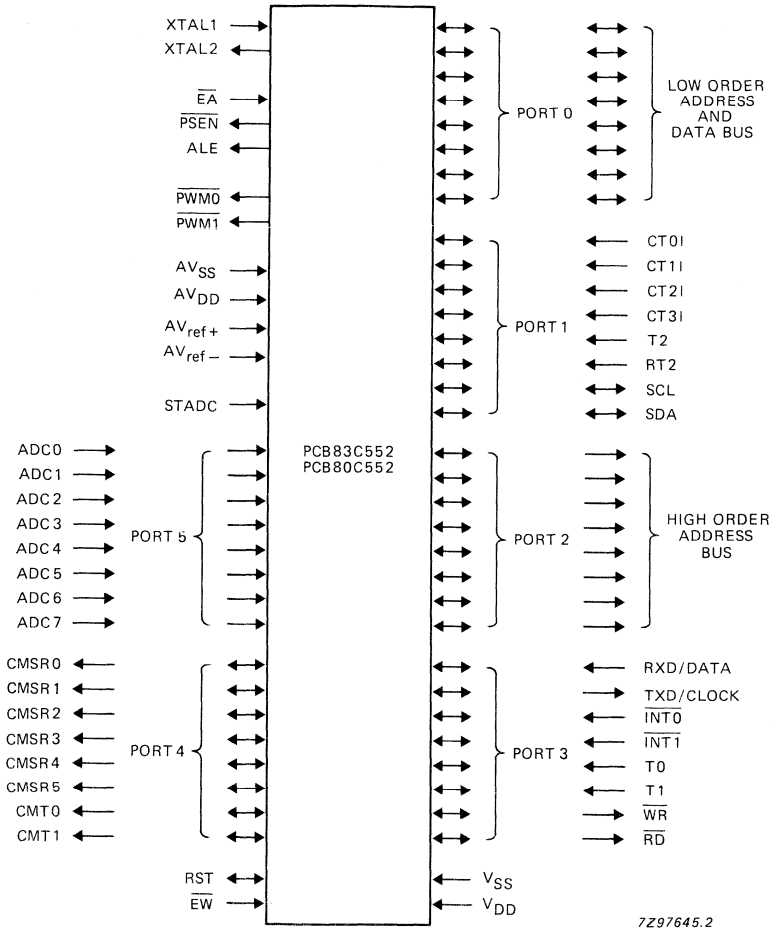


Fig. 2 Functional diagram.

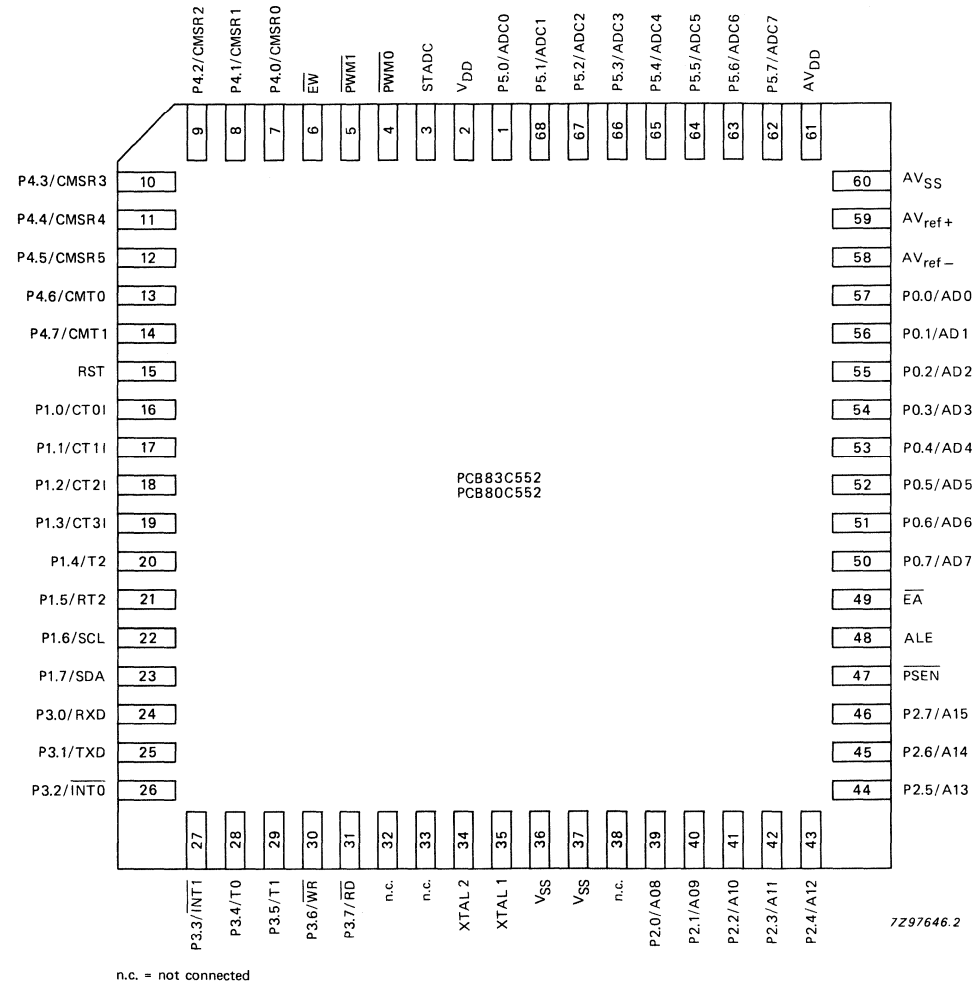


Fig. 3 Pinning diagram for PCB83C552.

DEVELOPMENT DATA

PINNING

2	V_{DD}	**Digital power supply**: + 5 V power supply pin during normal operation, Idle mode and Power-down mode
3	STADC	**Start ADC operation**: Input starting analogue to digital conversion (ADC operation can also be started by software)
4	$\overline{PWM0}$	**Pulse width** modulation output 0
5	$\overline{PWM1}$	**Pulse width** modulation output 1
6	$\overline{EW}$	**Enable watchdog timer**: Enable for T3 watchdog timer and disable Power-down mode
7-14	P4.0-P4.7	**Port 4** 8-bit quasi-bidirectional I/O port

Port pin	Alternative function	
P4.0	CMSR0	Timer T2: compare and set/reset outputs on a match with timer T2
P4.1	CMSR1	
P4.2	CMSR2	
P4.3	CMSR3	
P4.4	CMSR4	
P4.5	CMSR5	
P4.6	CMT0	Timer T2: compare and toggle outputs on a match with timer T2
P4.7	CMT1	

15	RST	**Reset**: Input to reset the PCB83C552. It also provides a reset pulse as output when timer T3 overflows.
16-23	P1.0-P1.7	**Port 1** 8-bit quasi-bidirectional I/O port

Port pin	Alternative function	
P1.0	CT0I	Capture timer input signals for timer T2
P1.1	CT1I	
P1.2	CT2I	
P1.3	CT3I	
P1.4	T2	: T2 event input
P1.5	RT2	: T2 timer reset signal. Rising edge triggered
P1.6	SCL	: Serial port clock line I^2C-bus
P1.7	SDA	: Serial port data line I^2C-bus

24-31	P3.0-P3.7	**Port 3** 8-bit quasi-bidirectional I/O port

Port pin	Alternative function	
P3.0	RXD	: Serial input port
P3.1	TXD	: Serial output port
P3.2	$\overline{INT0}$	: External interrupt
P3.3	$\overline{INT1}$	: External interrupt
P3.4	T0	: Timer 0 external input
P3.5	T1	: Timer 1 external input
P3.6	$\overline{WR}$	: External data memory write strobe
P3.7	$\overline{RD}$	: External data memory read strobe

32, 33 Not connected

PINNING (continued)

34	XTAL2	**Crystal input 2:** output of the inverting amplifier that forms the oscillator. Left open-circuit when an external oscillator clock is used.
35	XTAL1	**Crystal input 1:** input to the inverting amplifier that forms the oscillator, and input to the internal clock generator. Receives the external oscillator clock signal when an external oscillator is used.
36, 37	V_{SS}	**Two digital** ground pins
38		Not connected
39-46	P2.0-P2.7	**Port 2** 8-bit quasi-bidirectional I/O port Port pin — Alternative function P2.0-P2.7 — High-order address byte for external memory (A08-A15)
47	$\overline{PSEN}$	**Program store enable:** active LOW read strobe to external program memory
48	ALE	**Address latch enable:** latches the low byte of the address during accesses to external memory. It is activated every six oscillator periods. During an external data memory access one ALE pulse is skipped. ALE can drive up to 8 LSTTL inputs and handles CMOS inputs without an external pull-up.
49	$\overline{EA}$	**External access:** When $\overline{EA}$ is held at TTL level HIGH, the CPU executes out of the internal program ROM provided the program counter is less than 8192. When $\overline{EA}$ is held at TTL LOW level, the CPU executes out of external program memory. $\overline{EA}$ is not allowed to float.
50-57	P0.7-P0.0	**Port 0** 8-bit binary I/O port Port pin — Alternative function P0.7-P0.0 — Multiplexed low-order address and data bus of external memory (AD7-AD0)
58	AV_{ref-}	**Low end** of analogue to digital conversion reference resistor
59	AV_{ref+}	**High end** of analogue to digital conversion reference resistor
60	AV_{SS}	**Analogue** ground
61	AV_{DD}	**Analogue** power supply
62-68,1	P5.7-P5.0	**Port 5** 8-bit input port Port pin — Alternative function P5.0-P5.7 — Eight input channels to ADC (ADC0-ADC7)

To avoid a 'latch-up' effect at power-on, the voltage on any pin at any time must not be higher or lower than V_{DD} + 0,5 V or V_{SS} – 0,5 V respectively.

FUNCTIONAL DESCRIPTION

General

The PCB83C552 is a stand-alone high-performance microcontroller designed for use in real-time applications such as instrumentation, industrial control and specific automotive control applications.

The device provides in addition to the 80C51 standard functions, a number of dedicated hardware functions for these applications.

The PCB83C552 is a control-oriented CPU with on-chip program and data memory. It can be extended with external program memory up to 64 K bytes. It can also access up to 64 K bytes of external data memory. For systems requiring extra capability, the PCB83C552 can be expanded using standard memories and peripherals.

The PCB83C552 has two software selectable modes of reduced activity for further power reduction – Idle and Power-down. The Idle mode freezes the CPU while allowing the RAM, timers, serial ports and interrupt system to continue functioning. The Power-down mode saves the RAM contents but freezes the oscillator causing all other chip functions to be inoperative.

Memory organisation

The central processing unit (CPU) manupilates operands in three memory spaces; these are the 64 K-byte external data memory, 256-byte internal data memory and the 64 K-byte internal and external program memory. The internal data memory address space is sub-divided into the 256-byte internal data RAM and 128-byte Special Function Register (SFR) address spaces, as shown in Fig. 4. Figures 5(a) and (b) show the Special Function Register memory map. Internal RAM locations 0-127 are directly and indirectly addressable. Internal RAM locations 128-255 are only indirectly addressable. The special function register locations 128-255 are only directly addressable.

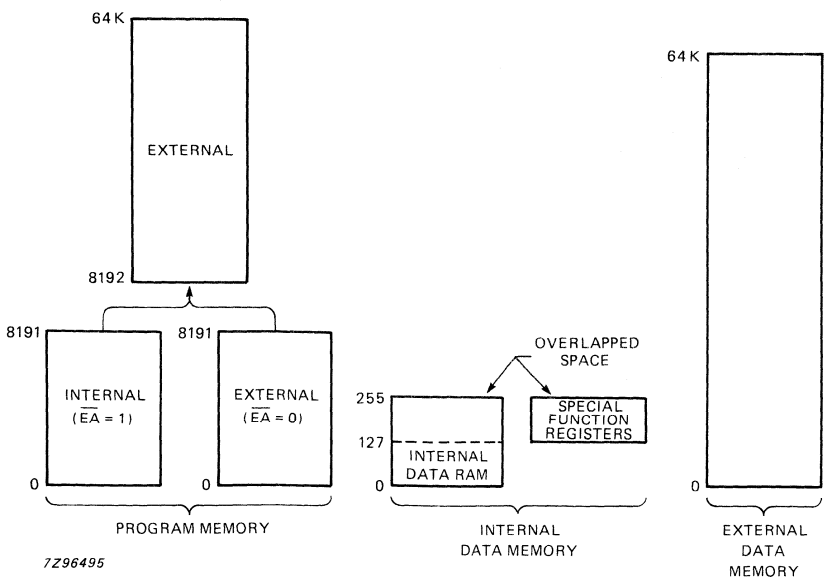
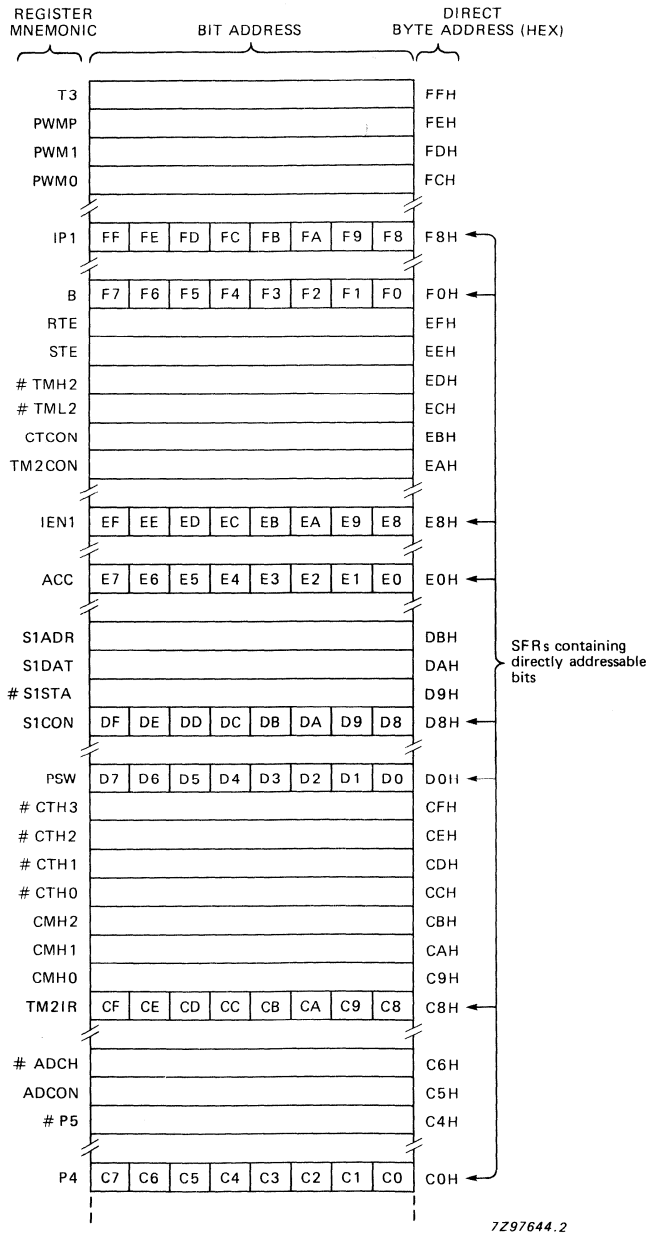


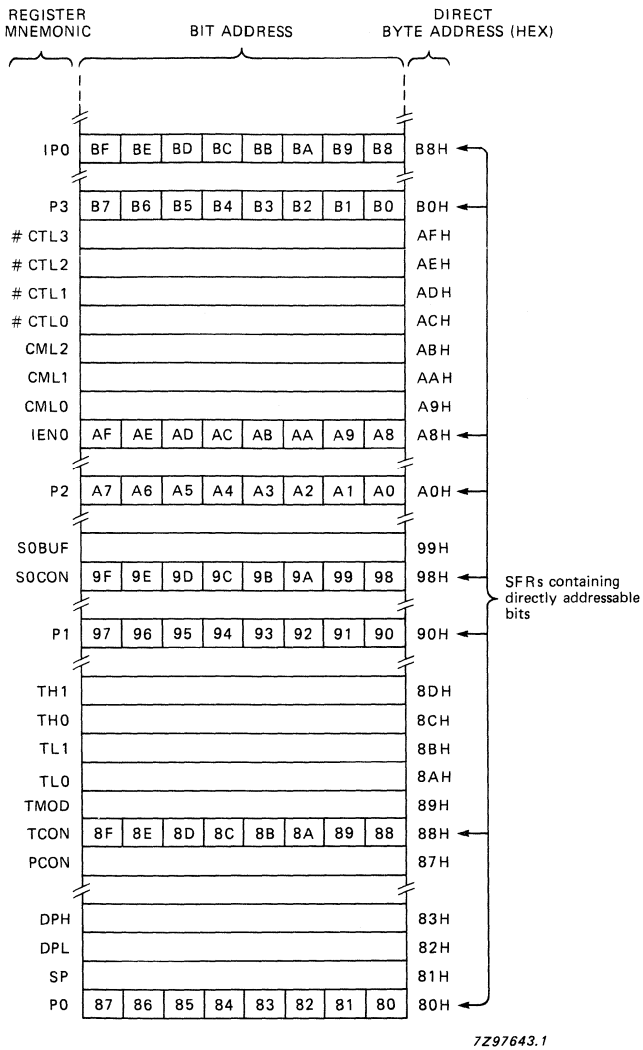
Fig. 4 Memory map.

FUNCTIONAL DESCRIPTION (continued)



# denotes read only registers

Fig. 5(a) Special Function Register memory map (continued in Fig. 5(b)).



# denotes read only registers

Fig. 5(b) Special Function Register memory map (continued from Fig. 5(a)).

FUNCTIONAL DESCRIPTION (continued)

The internal data RAM contains four register banks (each with eight registers), 128 addressable bits, a scratchpad area and the stack. The stack depth is limited by the available internal data RAM and its location is determined by the 8-bit stack pointer. All registers except the program counter and the four 8-register banks reside in the special function register address space. These memory mapped registers include arithmetic registers, pointers, I/O ports, interrupt system registers, ADC and PWM registers, timers and serial port registers. There are 128 addressable bit locations in the SFR address space.

The PCB83C552 contains 256 bytes of internal data RAM and 56 special function registers. It provides a non-paged program memory address space to accommodate relocatable code. Conditional branches are performed relative to the program counter. The register-indirect jump permits branching relative to a 16-bit base register with an offset provided by an 8-bit index register. 16-bit jumps and calls permit branching to any location in the contiguous 64 K program memory address space.

Addressing

The PCB83C552 has five methods for addressing source operands:

- Register
- Direct
- Register-Indirect
- Immediate
- Base-Register plus Index-Register-Indirect

The first three methods can be used for addressing destination operands. Most instructions have a "destination/source" field that specifies the data type, addressing methods and operands involved. For operations other than MOVs, the destination operand is also a source operand.

Access to memory addressing is as follows:

- Registers in one of the four 8-register banks through Register, Direct, or Register-Indirect
- 256 bytes of internal data RAM through Direct or Register-Indirect. Bytes 0-127 may be addressed directly/indirectly. Bytes 128-255 share their address locations with the SFR registers and so may only be addressed indirectly as data RAM
- Special function registers through Direct at address locations 128-255
- External data memory through Register-Indirect
- Program memory look-up tables through Base-Register plus Index-Register-Indirect

Instruction set

The PCB83C552 uses the powerful instruction set of the PCB80C51. Additional special function registers are incorporated to control the on-chip peripherals. The instruction set consists of 49 single-byte, 45 two-byte and 17 three-byte instructions. When using a 12 MHz oscillator, 64 instructions execute in 1 μs and 45 instructions execute in 2 μs. Multiply and divide instructions execute in 4 μs.

I/O facilities

The PCB83C552 has six 8-bit ports. Ports 0 - 3 are the same as in the 80C51, with the exception of the additional functions of port 1. The parallel I/O function of port 4 is equal to that of ports 1, 2 and 3. Port 5 has a parallel input port function, but has no function as an output port. Port lines P1.7 and P1.6 may be selected as the SDA and SCL lines of serial port SIO1 (I^2C). Because the I^2C-bus may be active while the device is disconnected from V_{DD}, these pins are provided with open drain drivers. Pins P1.7 and P1.6 do not have pull-up devices when used as ports.

Ports 0, 1, 2, 3, 4 and 5 perform the following alternative functions:

- Port 0: provides the multiplexed low-order address and data bus used for expanding the PCB83C552 with standard memories and peripherals.
- Port 1: port 1 is used for a number of special functions;
  - 4 capture inputs
  - external counter input
  - external counter reset input
  - SCL and SDA for the I^2C interface

Bits whose alternate function is not used may be used as normal bidirectional I/O pins.

- Port 2: provides the high-order address bus when expanding the PCB83C552 with external program memory and/or external data memory.
- Port 3: pins can be configured individually to provide:
  - external interrupt request inputs
  - counter inputs
  - serial port receiver input and transmitter output
  - control signals to READ and WRITE external data memory

The generation or use of a Port 3 pin as an alternative function is carried out automatically by the PCB83C552 provided the associated Special Function Register bit is set high.

- Port 4: can be configured to provide signals indicating a match between timer counter T2 and its compare registers.
- Port 5: may be used in conjunction with the ADC interface. Unused analogue inputs can be used as digital inputs. As port 5 lines may be used as inputs to the ADC, these digital inputs have an inherent hysteresis to prevent the input logic from drawing too much current from the power lines when driven by analogue signals. Channel to channel crosstalk should be taken into consideration when both digital and analogue signals are simultaneously input to port 5 (see D.C. characteristics).

All ports are bidirectional with the exception of port 5 which is an input port.

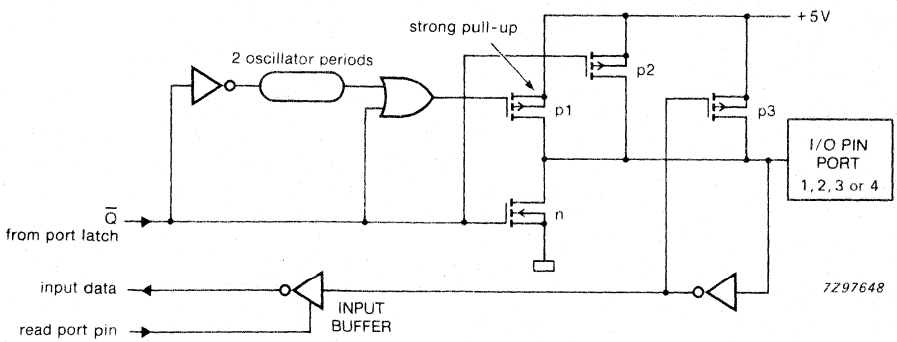


Fig. 6 I/O buffers in the PCB83C552 (Ports 2, 3, 4 and P1.0 to P1.5).

FUNCTIONAL DESCRIPTION (continued)

In addition to the standard 8-bit ports, the I/O facilities of the PCB83C552 also include a number of special I/O lines:

Pulse width modulated outputs

Two pulse width modulated output channels are provided with the PCB83C552. These channels output pulses of programmable length and interval. The repetition frequency is defined by an 8-bit prescaler PWMP which generates the clock for the counter. Both the prescaler and counter are common to both PWM channels. The 8-bit counter counts modulo 255 i.e. from 0 to 254 inclusive. The value of the 8-bit counter is compared to the contents of two registers: PWM0 and PWM1. Provided the contents of either of these registers is greater than the counter value, the output of $\overline{PWM0}$ or $\overline{PWM1}$ is set LOW. If the contents of these registers are equal to, or less than the counter value, the output will be HIGH. The pulse-width-ratio is therefore defined by the contents of the registers PWM0 and PWM1. The pulse-width-ratio is in the range of 0 to 255/255 and may be programmed in increments of 1/255.

The repetition frequency f_{PWM}, at the $\overline{PWMn}$ outputs is given by:

$$f_{PWM} = \frac{f_{osc}}{2 \times (1 + PWMP) \times 255}$$

This gives a repetition frequency range of 92 Hz to 23,5 kHz (f_{osc} = 12 MHz).

By loading the PWM registers with either 00H or FFH, the PWM outputs can be retained at a constant HIGH or LOW level respectively. When loading FFH to the PWM registers, the 8-bit counter will never actually reach this value.

Both $\overline{PWMn}$ output pins are driven by push-pull drivers, and are not shared with any other function.

Prescaler frequency control register PWMP

	7	6	5	4	3	2	1	0
PWMP (FEH)								
	MSB							LSB

Bit	Function
PWMP.0-7	Prescaler division factor = (PWMP) + 1

Pulse width registers PWM0 and PWM1

	7	6	5	4	3	2	1	0
PWM0 (FCH) PWM1 (FDH)								
	MSB							LSB

Bit	Function
PWM0.0-7 PWM1.0-7	Low/high ratio of $\overline{PWMn}$ signals $= \frac{(PWMn)}{255 - (PWMn)}$

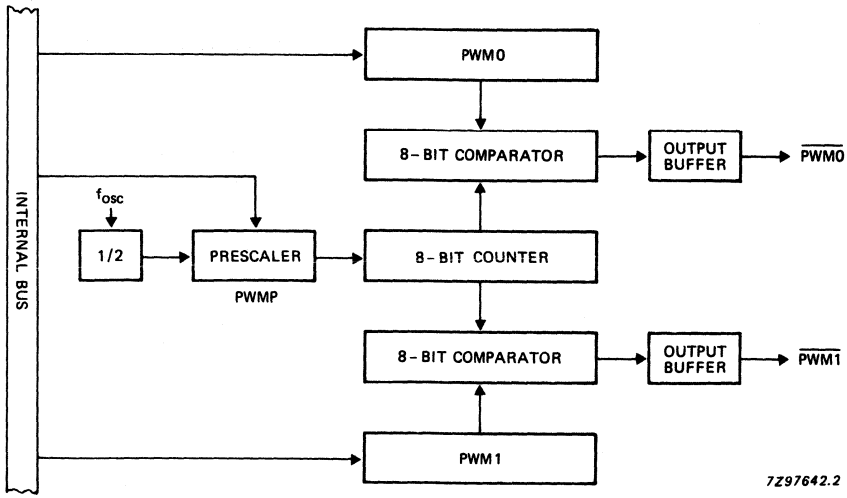


Fig. 7 Functional diagram of pulse width modulated outputs.

DEVELOPMENT DATA

Analogue input pins

The analogue input circuitry consists of an 8-input analogue multiplexer and an ADC with 10-bit resolution. The analogue reference voltage and analogue power supplies are connected via separate input pins. The conversion takes 50 machine cycles i.e. 50 μs at 12 MHz oscillator frequency.

The ADC is controlled using the ADCON control register. Input channels are selected by the analogue multiplexer, care of ADCON register bits 0-2.

ADC control register ADCON

	7	6	5	4	3	2	1	0
ADCON (C5H)	ADC.1	ADC.0	ADEX	ADCI	ADCS	AADR2	AADR1	AADR0

Bit	Symbol	Function
ADCON.7	ADC.1	Bit 1 of ADC converted value
ADCON.6	ADC.0	Bit 0 of ADC converted value
ADCON.5	ADEX	Enable external start of conversion by STADC
		0 = Conversion cannot be started externally by STADC
		1 = Conversion can be started externally by STADC
ADCON.4	ADCI	ADC interrupt flag: this flag is set when an ADC conversion result is ready to be read. An interrupt is invoked if this is enabled. The flag must be cleared by software. It cannot be set by software.

FUNCTIONAL DESCRIPTION (continued)

ADCON.3 ADCS — ADC start and status: setting this bit starts an ADC conversion. It may be set by software or by the external signal STADC. The ADC logic ensures that this signal is HIGH while the ADC is busy. On completion of the conversion, ADCS is reset at the same time the interrupt flag ADCI is set. ADCS can not be reset by software.

ADCI	ADCS	OPERATION
0	0	ADC not busy, a conversion can be started
0	1	ADC busy, start of a new conversion is blocked
1	0	Conversion completed, start of a new conversion is blocked
1	1	Not possible

ADCON.2 ADDR2
ADCON.1 AADR1
ADCON.0 AADR0

Analogue input select: this binary coded address selects one of the eight analogue port bits of P5 to be input to the converter. It can only be changed when ADCI and ADCS are both LOW. AADR2 is the most significant bit (100 selects the ADC4 analogue input channel).

The completion of the 10-bit ADC conversion is flagged by ADCI in the ADCON register and the result is stored in special function register ADCH (upper 8 bits) and the 2 LSBs in register ADCON.

An ADC conversion in progress is unaffected by an external or software ADC start. The result of a completed conversion remains unaffected provided ADCI = logic 1. While ADCS = logic 1 or ADCI = logic 1, a new ADC START will be blocked and consequently lost. An ADC conversion already in progress is aborted when the Idle or Power-down mode is entered. The result of a completed conversion (ADCI = logic 1) remains unaffected when entering the Idle mode.

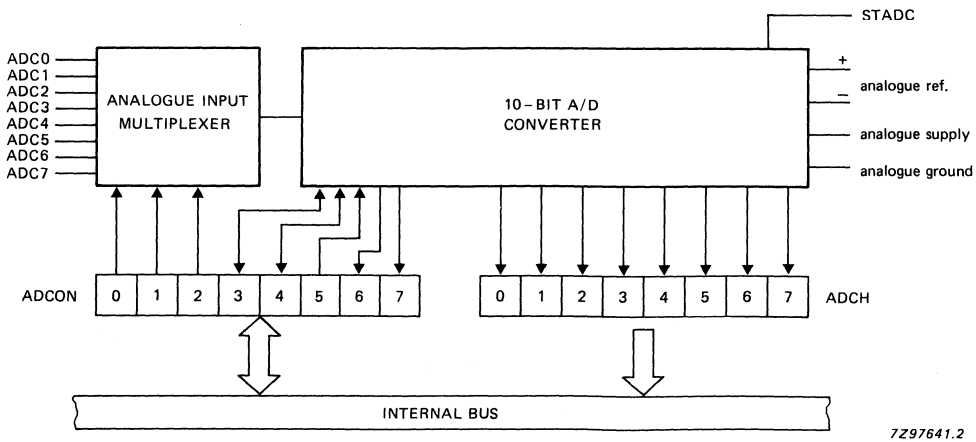


Fig. 8 Functional diagram of analogue input.

Timer/event counters

The PCB83C552 contains three 16-bit timer/event counters: Timer 0, Timer 1 and Timer T2 and one 8-bit timer, T3. Timer 0 and Timer 1 may be programmed to carry out the following functions:

- Measure time intervals and pulse durations
- Count events
- Generate interrupt requests

Timer 0 and Timer 1 can be programmed independently to operate in three modes:

- Mode 0: 8-bit timer or 8-bit counter each with divide by 32 prescaler
- Mode 1: 16-bit time-interval or event counter
- Mode 2: 8-bit time-interval or event counter with automatic reload upon overflow

Timer 0 can be programmed to operate in an additional mode as follows:

- Mode 3: one 8-bit time-interval or event counter and one 8-bit time-interval counter

When Timer 0 is in Mode 3, Timer 1 can be programmed to operate in Modes 0, 1 or 2 but cannot set an interrupt request flag or generate an interrupt. However the overflow from Timer 1 can be used to pulse the serial port transmission-rate generator.

The frequency handling range of these counters with a 12 MHz crystal is as follows:

- In the timer function, the timer is incremented at a frequency of 1 MHz – a division by 12 of the oscillator frequency
- 0 Hz to an upper limit of 0,5 MHz when programmed for external inputs

Both internal and external inputs can be gated to the counter by a second external source for directly measuring pulse durations.

The counters are started and stopped under software control. Each one sets its interrupt request flag when it overflows from all logic 1s to all logic 0s (or automatic reload value), with the exception of mode 3 as previously described.

Timer T2

Timer T2 is a 16 bit timer/counter which has, coupled to it, capture and compare facilities. The operational diagram is shown in Fig. 9.

The 16 bit timer/counter is clocked via a prescaler with a programmable division factor of 1, 2, 4 or 8. The input of the prescaler is clocked with 1/12 of the oscillator frequency, or with positive edges on the T2 input, or it is switched to the off position. This prescaler is cleared if its division factor or its input source is changed, or if the timer/counter is reset. T2 is readable 'on the fly', but posseses no extra read latches; this means that software precautions have to be taken against misinterpretation in overflow from least to most significant byte during read. T2 is not loadable and is reset by the RST signal or at the positive edge of the input signal RT2, if enabled. In the Idle mode the timer/counter and prescaler are reset and halted.

T2 is connected to four 16-bit capture registers: CT0, CT1, CT2 and CT3. These registers are loaded with the contents of T2 and an interrupt is requested upon receipt of the input signals CT0I, CT1I, CT2I or CT3I. These input signals are shared with port 1. Using the capture register CTCON, these inputs may capture on a positive edge, a negative edge or on either a positive or negative edge.

FUNCTIONAL DESCRIPTION (continued)

The contents of the compare registers CM0, CM1 and CM2 are continually compared with the counter value of Timer T2. When a match is found an interrupt may be invoked. Using the match signal of CM0, the controller sets bits 0-5 of port 4, if the corresponding bits of the set enable register STE are logic 1.

Considering a match with CM1, if the corresponding bits of the reset/toggle enable register RTE are logic 1, then the controller will use the match signal to reset bits 0-5 of port 4. Bits 6 and 7 of port 4 may be 'toggled' by the signal that indicates a match between Timer T2 and CM2 if the corresponding bits of RTE are logic 1. CM0, CM1 and CM2 are reset by the RST signal.

Port 4 can be read and written by software without affecting the toggle, set and reset signals. At byte overflow of the least significant byte, or at a 16-bit overflow of the timer/counter, an interrupt sharing the same interrupt vector is requested. Either or both of these overflows can be programmed to request an interrupt.

All interupt flags must be reset by software.

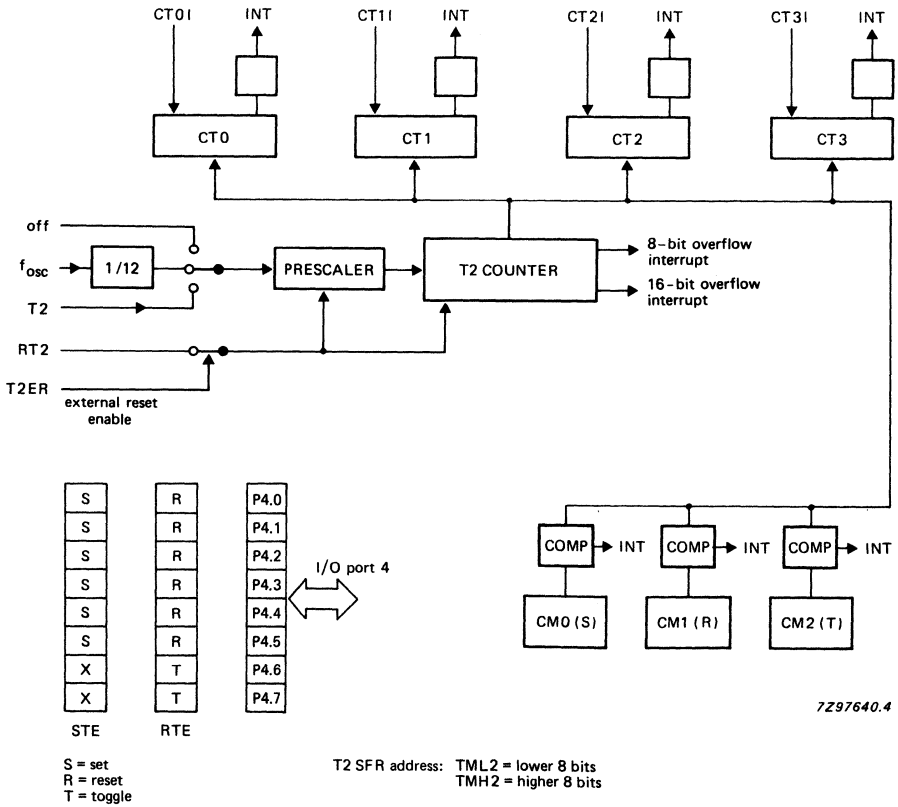


Fig. 9 Block diagram of Timer T2 configuration.

Counter control register TM2CON

	7	6	5	4	3	2	1	0
TM2CON (EAH)	T2IS1	T2IS0	T2ER	T2B0	T2P1	T2P0	T2MS1	T2MS0
	MSB							LSB

Bit	Symbol	Function
TM2CON.7	T2IS1	Timer 2 16 bit overflow interrupt select
TM2CON.6	T2IS0	Timer 2 byte overflow interrupt select
TM2CON.5	T2ER	Timer 2 external reset enable
TM2CON.4	T2B0	Timer 2 byte overflow interrupt flag
TM2CON.3	T2P1	Timer 2 prescaler select
TM2CON.2	T2P0	
TM2CON.1	T2MS1	Timer 2 mode select
TM2CON.0	T2MS0	

T2P1	T2P0	T2 clock
0	0	clock source
0	1	clock source/2
1	0	clock source/4
1	1	clock source/8

T2MS1	T2MS0	Mode Selected
0	0	Timer T2 is halted
0	1	T2 clock source = $f_{osc}/12$
1	0	Test mode; do not use
1	1	T2 clock source = pin T2

Capture control register CTCON

	7	6	5	4	3	2	1	0
CTCON (EBH)	CTN3	CTP3	CTN2	CTP2	CTN1	CTP1	CTN0	CTP0
	MSB							LSB

Bit	Symbol	Capture/Interrupt on:
CTCON.7	CTN3	CT3I negative edge
CTCON.6	CTP3	CT3I positive edge
CTCON.5	CTN2	CT2I negative edge
CTCON.4	CTP2	CT2I positive edge
CTCON.3	CTN1	CT1I negative edge
CTCON.2	CTP1	CT1I positive edge
CTCON.1	CTN0	CT0I negative edge
CTCON.0	CTP0	CT0I positive edge

DEVELOPMENT DATA

FUNCTIONAL DESCRIPTION (continued)

Timer interrupt flag register TM21R

	7	6	5	4	3	2	1	0
TM2IR (C8H)	T20V	CMI2	CMI1	CMI0	CTI3	CTI2	CTI1	CTI0
	MSB							LSB

Bit	Symbol	Function
TM2IR.7	T20V	T2 16-bit overflow interrupt flag
TM2IR.6	CMI2	CM2 interrupt flag
TM2IR.5	CMI1	CM1 interrupt flag
TM2IR.4	CMI0	CM0 interrupt flag
TM2IR.3	CTI3	CT3 interrupt flag
TM2IR.2	CTI2	CT2 interrupt flag
TM2IR.1	CTI1	CT1 interrupt flag
TM2IR.0	CTI0	CT0 interrupt flag

Interrupt enable register IEN1 is used to enable/disable timer 2 interrupts.
Interrupt priority register IP1 is used to determine the timer interrupt priority.

The set enable register STE

	7	6	5	4	3	2	1	0
STE (EEH)	–	–	SP45	SP44	SP43	SP42	SP41	SP40
	MSB							LSB

Bit	Symbol	Function
STE.7	–	not used
STE.6	–	not used
STE.5	SP45	if "1" then P4.5 is set on a match between CM0 and T2
STE.4	SP44	if "1" then P4.4 is set on a match between CM0 and T2
STE.3	SP43	if "1" then P4.3 is set on a match between CM0 and T2
STE.2	SP42	if "1" then P4.2 is set on a match between CM0 and T2
STE.1	SP41	if "1" then P4.1 is set on a match between CM0 and T2
STE.0	SP40	if "1" then P4.0 is set on a match between CM0 and T2

If STE.n is "0" then P4.n is not affected by a match between CM0 and T2

The reset/toggle enable register RTE

	7	6	5	4	3	2	1	0
RTE (EFH)	TP47	TP46	RP45	RP44	RP43	RP42	RP41	RP40
	MSB							LSB

Bit	Symbol	Function
RTE.7	TP47	if "1" then P4.7 toggles on a match between CM2 and T2
RTE.6	TP46	if "1" then P4.6 toggles on a match between CM2 and T2
RTE.5	RP45	if "1" then P4.5 is reset on a match between CM1 and T2
RTE.4	RP44	if "1" then P4.4 is reset on a match between CM1 and T2
RTE.3	RP43	if "1" then P4.3 is reset on a match between CM1 and T2
RTE.2	RP42	if "1" then P4.2 is reset on a match between CM1 and T2
RTE.1	RP41	if "1" then P4.1 is reset on a match between CM1 and T2
RTE.0	RP40	if "1" then P4.0 is reset on a match between CM1 and T2

If RTE.n is "0" then P4.n is not affected by a match between CM1 and T2 or CM2 and T2

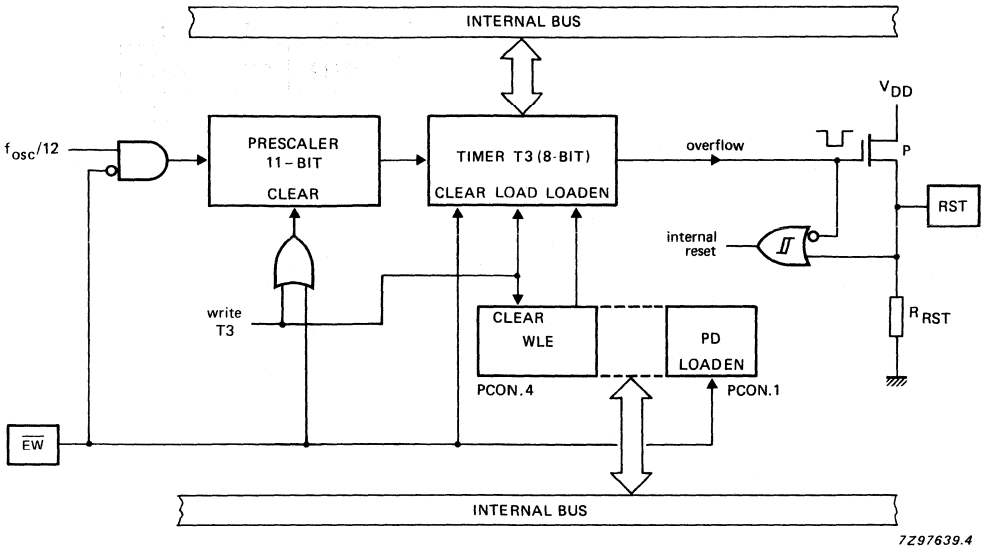


Fig. 10 Functional diagram of T3 watchdog timer.

T3 The watchdog timer (see Fig. 10)

In addition to Timer T2 and the standard timers, a watchdog timer consisting of an 11-bit prescaler and an 8-bit timer are also incorporated.

The timer is incremented every 2 ms, derived from the oscillator frequency of 12 MHz by the following:

$$f_{timer} = \frac{f_{osc}}{12 \times 2048}$$

When a timer overflow occurs, the microcontroller is reset and a reset output pulse is generated at pin RST. To prevent a system reset the timer must be reloaded in time by the application software. If the processor suffers a hardware/software malfunction, the software will fail to reload the timer. This failure will produce a reset upon overflow thus preventing the processor running out of control.

The watchdog timer can only be reloaded if the condition flag WLE = PCON.4 has been previously set by software.

At the moment the counter is loaded the condition flag is automatically cleared.

The time interval between the timer's reloading and occurance of a reset, is dependent upon the reloaded value. This may range from 2 ms to 0,5 s at an oscillator frequency of 12 MHz.

In the Idle state the watchdog timer and reset circuitry remain active.

The watchdog timer is controlled by the watchdog enable pin ($\overline{EW}$). A logic 0 enables the watchdog. timer and disables the Power-down mode. A logic 1 disables and resets the watchdog timer and enables the Power-down mode.

DEVELOPMENT DATA

FUNCTIONAL DESCRIPTION (continued)

Serial I/O (see Fig. 11)

The PCB83C552 is equipped with two independent serial ports. SIO0 is the full duplex UART port and is identical to the serial port of the PCB80C51 (see "SINGLE-CHIP 8-BIT MICROCONTROLLERS" User Manual).

Serial port SIO1 supports the I^2C-bus, the function of which is controlled by the S1CON register. S1STA is the status register whose contents may also be used as a vector to various service routines. S1DAT is the data shift register and S1ADR the slave address register. The least significant bit of S1ADR enables/disables general call address recognition.

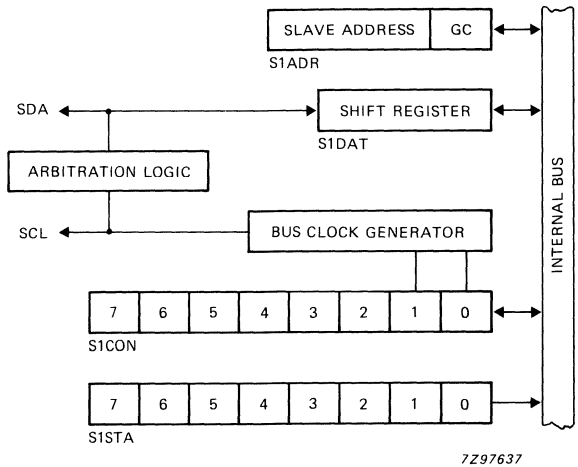


Fig. 11 Block diagram of I^2C serial I/O.

The I^2C serial I/O has complete autonomy in byte handling and operates in 4 modes:

1. Master transmitter
2. Master receiver
3. Slave transmitter
4. Slave receiver

Slave address recognition is performed by on-chip hardware.

The I^2C-bus consists of two lines: a data line (SDA) and a clock line (SCL). These lines also function as the I/O port lines on P1.7 and P1.6. The system is unique because data transport, clock generation, address recognition and bus control arbitration are all controlled by hardware.

Serial control register S1CON

	7	6	5	4	3	2	1	0
S1CON (D8H)	X	ENS1	STA	STO	SI	AA	CR1	CR0

Bits CR1 and CR0 determine the clock frequency that is generated in the master mode of operation. Table 1 displays the clock rate when using a 12 MHz crystal.

Table 1 Clock rate when using a 12 MHz crystal

CR1/CR0	bit frequency	f_{osc} divided by
0 0	12,5 kHz	960
0 1	100 kHz	120
1 0	200 kHz	60 ($f_{osc} < 6$ MHz meeting I^2C)
1 1	62,5 - 0,5 kHz	96 x (256 – reload value Timer 1) (reload value range: 0-254 in mode 2)

AA

Assert acknowledge bit. When this bit is set, an acknowledge is returned after any one of the following conditions:

- Own slave address is received
- General call address is received (S1ADR.0 = logic 1)
- A data byte is received, while the device is programmed to be a master receiver
- A data byte is received, while the device is a selected slave receiver

When this bit is reset, no acknowledge is returned. Consequently, no interrupt is requested when the own address or general call address is received.

SI

SIO1 interrupt flag. This flag is set, and an interrupt request is generated, after any of the following events occur:

- A START condition is generated in MST mode
- The own slave address has been received during AA = logic 1
- The general call address has been received while S1ADR.0 and AA = logic 1
- A data byte has been received or transmitted in MST mode (even if arbitration is lost)
- A data byte has been received or transmitted as selected slave
- A STOP or START condition is received as selected slave receiver or transmitter

STO

STOP flag. When in master mode, and this bit is set a STOP condition is generated. A STOP condition detected on the I^2C-bus clears this bit. This bit may also be set in slave mode in order to recover from an error condition. Then no STOP condition is generated to the I^2C-bus, but the hardware releases the SDA and SCL lines and switches to the not selected slave receiver mode. The STOP flag is cleared by the hardware.

STA

START flag. When this bit is set in slave mode, the hardware checks the I^2C-bus and generates a START condition if the bus is free or after the bus becomes free. If the device operates in master mode it will generate a repeated START condition.

FUNCTIONAL DESCRIPTION (continued)

ENS1

0 = Serial I/O Disabled and reset. P1.6 and P1.7 I/O port function with open drain

1 = Serial I/O Enabled. Output ports P1.6 and P1.7 must be set to logic 1

Serial status register S1STA (S1STA is a read-only register)

	7	6	5	4	3	2	1	0
S1STA (D9H)	SC4	SC3	SC2	SC1	SC0	0	0	0

S1STA.3 - S1STA.7 hold a status code. S1STA.0 - S1STA.2 are held LOW. The contents of the status register may be used as a vector to a service routine. This optimizes the response time of the software and consequently that of the I^2C-bus.

Abbreviations used:

SLA	:	7-bit slave address
R	:	Read bit
W	:	Write bit
ACK	:	Acknowledgement (acknowledge bit = logic 0)
$\overline{\text{ACK}}$	:	Not acknowledgement (acknowledge bit = logic 1)
DATA	:	8-bit data byte to or from I^2C-bus
MST	:	Master
SLV	:	Slave
TRX	:	Transmitter
REC	:	Receiver

The following is a list of the status codes:

MST/TRX mode

S1STA value

08H	– A START condition has been transmitted
10H	– A repeated START condition has been transmitted
18H	– SLA and W have been transmitted, ACK has been received
20H	– SLA and W have been transmitted, $\overline{\text{ACK}}$ received
28H	– DATA of S1DAT has been transmitted, ACK received
30H	– DATA of S1DAT has been transmitted, $\overline{\text{ACK}}$ received
38H	– Arbitration lost in SLA, R/W or DATA

MST/REC mode

S1STA value

38H	– Arbitration lost while returning $\overline{\text{ACK}}$
40H	– SLA and R have been transmitted, ACK received
48H	– SLA and R have been transmitted, $\overline{\text{ACK}}$ received
50H	– DATA has been received, ACK returned
58H	– DATA has been received, $\overline{\text{ACK}}$ returned

SLV/REC mode

S1STA value

60H – Own SLA and W have been received, ACK returned
68H – Arbitration lost in SLA, R/W as MST. Own SLA and W have been received, ACK returned
70H – General CALL has been received, ACK returned
78H – Arbitration lost in SLA, R/W as MST. General call has been received
80H – Previously addressed with own SLA. DATA byte received, ACK returned
88H – Previously addressed with own SLA. DATA byte received, $\overline{\text{ACK}}$ returned
90H – Previously addressed with general call. DATA byte has been received, ACK has been returned
98H – Previously addressed with general call. DATA byte has been received, $\overline{\text{ACK}}$ has been returned
A0H – A STOP condition or repeated START condition has been received while still addressed as SLV/REC or SLV/TRX.

SLV/TRX mode

S1STA value

A8H – Own SLA and R have been received, ACK returned
B0H – Arbitration lost in SLA, R/W as MST. Own SLA and R have been received, ACK returned
B8H – DATA byte has been transmitted, ACK received
C0H – DATA byte has been transmitted, $\overline{\text{ACK}}$ received
C8H – Last DATA byte has been transmitted (AA = logic 0), ACK received

Miscellaneous

S1STA value

00H – Bus error during MST mode or selected SLV mode, due to an erroneous START or STOP condition

DEVELOPMENT DATA

The data shift register S1DAT

	7	6	5	4	3	2	1	0
S1DAT (DAH)								

This register contains the serial data to be transmitted or data which has just been received. Bit 7 is transmitted or received first; i.e. data is shifted from right to left.

Address register S1ADR

	slave address							GC
S1ADR (DBH)	7	6	5	4	3	2	1	0

S1ADR.0, GC : 0 = general call address is not recognized
1 = general call address is recognized

S1ADR.7-1 : own slave address

This 8-bit register may be loaded with the 7-bit slave address to which the controller will respond when programmed as a slave receiver/transmitter. The LSB (GC) is used to determine whether the general call address is recognized.

FUNCTIONAL DESCRIPTION (continued)

Idle and Power-down operation (see Fig. 12)

Idle mode operation permits the interrupt, serial ports and timer blocks to continue to function while the CPU is halted. The following functions are also switched off when the processor enters the Idle mode.

Timer T2	(stopped and reset)
PWM0, PWM1	(reset, output = HIGH)
ADC	(aborted if in progress)

The following functions remain active during Idle mode. These functions may generate an interrupt or reset and thus end the Idle mode.

Timer 0, Timer 1
Timer T3
SIO0, SIO1
External interrupt

The Power-down operation freezes the oscillator. The Power-down mode can only be activated by setting the PD bit in the PCON register. The PD bit can only be set if the EWN input is HIGH.

Idle mode

The instruction that sets PCON.0 is the last instruction executed in the normal operating mode before Idle mode is activated. Once in the Idle mode, the CPU status is preserved in its entirety: the Stack Pointer, Program Counter, Program Status Word, Accumulator, RAM and all other registers maintain their data during Idle mode. The status of the external pins during Idle mode is shown in Table 2.

There are two ways to terminate the Idle mode:

Activation of any enabled interrupt will cause PCON.0 to be cleared by hardware terminating Idle mode. The interrupt is serviced, and following return from interrupt instruction RETI, the next instruction to be executed will be the one which follows the instruction that wrote a logic 1 to PCON.0.

The flag bits GF0 and GF1 may be used to determine whether the interrupt was received during normal execution or during the Idle mode. For example, the instruction that writes to PCON.0 can also set or clear one or both flag bits. When Idle mode is terminated by an interrupt, the service routine can examine the status of the flag bits.

The second way of terminating the Idle mode is with an external hardware reset, or an internal reset caused by an overflow of Timer T3. Since the oscillator is still running, the hardware reset is required to be active for two machine cycles (24 oscillator periods) to complete the reset operation.

Power-down mode

The instruction that sets PCON.1 is the last executed prior to going into the Power-down mode. Once in Power-down mode, the oscillator is stopped. Only the contents of the on-chip RAM are preserved. The Special Function Registers are not saved. A hardware reset is the only way of exiting the Power-down mode.

In the Power-down mode, V_{DD} may be reduced to minimize circuit power consumption. The voltage must not be reduced until the Power-down mode is entered, but must be restored before the hardware reset is applied which will free the oscillator. Reset should not be released until the oscillator has restarted and stabilized.

The status of the external pins during Power-down mode is shown in Table 2. If the Power-down mode is activated while in external program memory, the port data that is held in the Special Function Register P2 is restored to Port 2. If the data is a logic 1, the port pin is held HIGH during the Power-down mode by the strong pull-up transistor p1 (see Fig. 6).

Table 2 Status of external pins during Idle and Power-down modes

mode	memory	ALE	$\overline{PSEN}$	Port 0	Port 1	Port 2	Port 3	Port 4	$\overline{PWM0}$/$\overline{PWM1}$
Idle (1)	internal	1	1	port data	port data	port data	port data	port data	HIGH
Idle (1)	external	1	1	floating	port data	address	port data	port data	HIGH
Power-down	internal	0	0	port data	port data	port data	port data	port data	HIGH
Power-down	external	0	0	floating	port data	port data	port data	port data	HIGH

Power control register (PCON)

These special modes are activated by software via the Special Function Register PCON. Its hardware address is 87H. PCON is not bit addressable.

	7	6	5	4	3	2	1	0
PCON (87H)	SMOD	–	–	WLE	GF1	GF0	PD	IDL

Bit	Symbol	Function
PCON.7	SMOD	Double Baud rate bit. When set to logic 1 the baud rate is doubled when the serial port SIO0 is being used in modes 1, 2 or 3
PCON.6	–	(reserved)
PCON.5	–	(reserved)
PCON.4	WLE	Watchdog load enable. This flag must be set by software prior to loading T3 (watchdog timer). It is cleared when T3 is loaded
PCON.3	GF1	General-purpose flag bit
PCON.2	GF0	General-purpose flag bit
PCON.1	PD	Power-down bit. Setting this bit activates Power-down mode. It can only be set if input $\overline{EW}$ is high.
PCON.0	IDL	Idle mode bit. Setting this bit activates the Idle mode

If logic 1s are written to PD and IDL at the same time, PD takes precedence. The reset value of PCON is (0XX00000).

DEVELOPMENT DATA

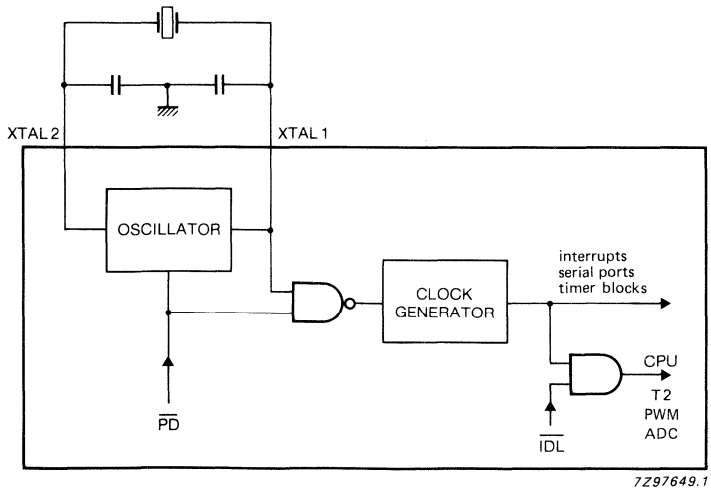


Fig. 12 Internal Idle and Power-down clock configuration.

FUNCTIONAL DESCRIPTION (continued)

Interrupt system (see Fig. 13)

External events and the real-time-driven on-chip peripherals require service by the CPU asynchronous to the execution of any particular section of code. To tie the asynchronous activities of these functions to normal program execution a multiple-source, two-priority-level, nested interrupt system is provided. Interrupt response latency is from 3 μs to 8 μs when using a 12 MHz crystal. The PCB83C552 acknowledges interrupt requests from fifteen sources as follows:

- $\overline{\text{INT0}}$ and $\overline{\text{INT1}}$: externally via pins 26 and 27 respectively
- Timer 0 and Timer 1: from the two internal counters
- Timer T2 (8 separate interrupts): 4 capture interrupts, 3 compare interrupts and an overflow interrupt
- ADC end-of-conversion interrupt
- I^2C serial I/O port interrupt
- UART serial I/O port interrupt

Each interrupt vectors to a separate location in program memory for its service program. Each source can be individually enabled or disabled by a corresponding bit in the IEN0 or IEN1 register, moreover each interrupt may be programmed to a high or low priority level using a corresponding bit in the IP0 or IP1 register. Also all enabled sources can be globally disabled or enabled. Both external interrupts can be programmed to be level-activated or transition-activated; an active LOW level allows "wire-ORing" of several interrupt sources to one input pin.

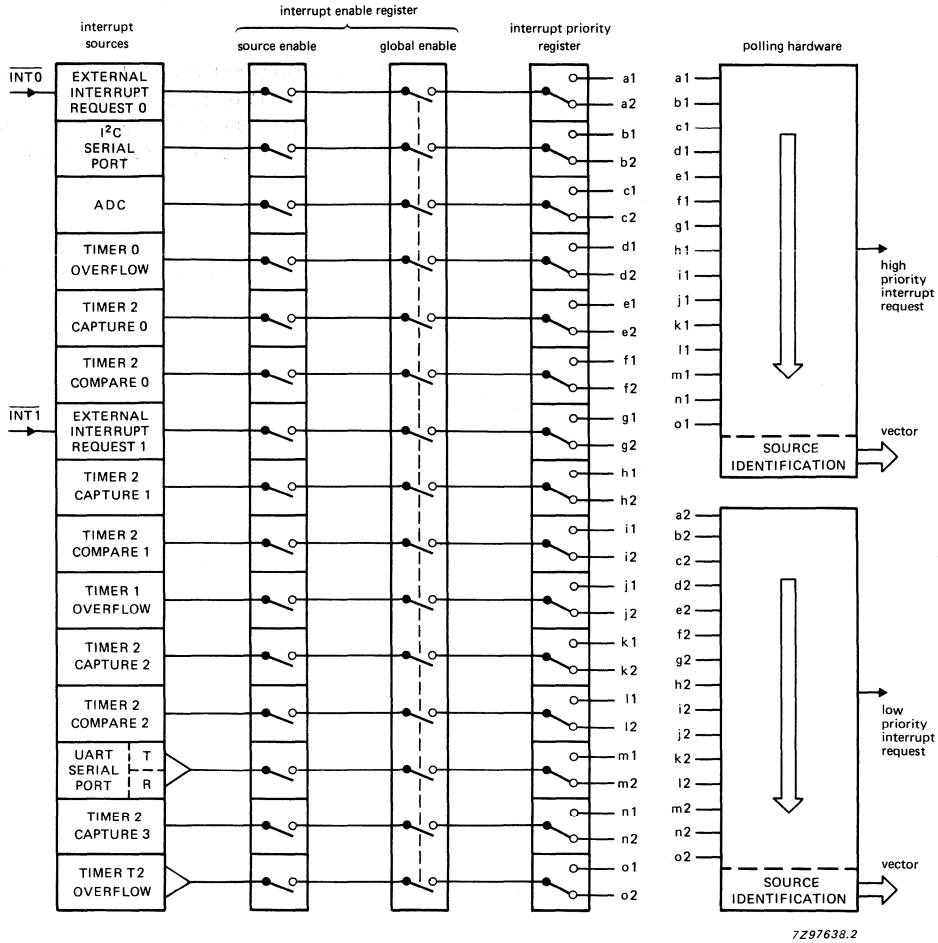


Fig. 13 Interrupt system.

FUNCTIONAL DESCRIPTION (continued)

Interrupt enable registers

	7	6	5	4	3	2	1	0
IEN0 (A8H)	EA	EAD	ES1	ES0	ET1	EX1	ET0	EX0

Bit	Symbol	Function
IEN0.7	EA	General enable/disable control 0 = No interrupt is enabled 1 = Any individually enabled interrupt will be accepted
IEN0.6	EAD	Enable ADC interrupt
IEN0.5	ES1	Enable SIO1 (I^2C) interrupt
IEN0.4	ES0	Enable SIO0 (UART) interrupt
IEN0.3	ET1	Enable Timer 1 interrupt
IEN0.2	EX1	Enable External 1 interrupt
IEN0.1	ET0	Enable Timer 0 interrupt
IEN0.0	EX0	Enable External 0 interrupt

	7	6	5	4	3	2	1	0
IEN1 (E8H)	ET2	ECM2	ECM1	ECM0	ECT3	ECT2	ECT1	ECT0

Bit	Symbol	Function
IEN1.7	ET2	Enable T2 overflow interrupt(s)
IEN1.6	ECM2	Enable T2 comparator 2 interrupt
IEN1.5	ECM1	Enable T2 comparator 1 interrupt
IEN1.4	ECM0	Enable T2 comparator 0 interrupt
IEN1.3	ECT3	Enable T2 capture register 3 interrupt
IEN1.2	ECT2	Enable T2 capture register 2 interrupt
IEN1.1	ECT1	Enable T2 capture register 1 interrupt
IEN1.0	ECT0	Enable T2 capture register 0 interrupt

where "0" = interrupt disabled
and "1" = interrupt enabled

Interrupt priority registers

	7	6	5	4	3	2	1	0
IP0 (B8H)	–	PAD	PS1	PS0	PT1	PX1	PT0	PX0

Bit	Symbol	Function
IP0.7	–	Unused
IP0.6	PAD	ADC interrupt priority level
IP0.5	PS1	SIO1 (I^2C) interrupt priority level
IP0.4	PS0	SIO0 (UART) interrupt priority level
IP0.3	PT1	Timer 1 interrupt priority level
IP0.2	PX1	External interrupt 1 priority level
IP0.1	PT0	Timer 0 interrupt priority level
IP0.0	PX0	External interrupt 0 priority level

	7	6	5	4	3	2	1	0
IP1 (F8H)	PT2	PCM2	PCM1	PCM0	PCT3	PCT2	PCT1	PCT0

DEVELOPMENT DATA

Bit	Symbol	Function
IP1.7	PT2	T2 overflow interrupt(s) priority level
IP1.6	PCM2	T2 comparator 2 priority interrupt level
IP1.5	PCM1	T2 comparator 1 priority interrupt level
IP1.4	PCM0	T2 comparator 0 priority interrupt level
IP1.3	PCT3	T2 capture register 3 priority interrupt level
IP1.2	PCT2	T2 capture register 2 priority interrupt level
IP1.1	PCT1	T2 capture register 1 priority interrupt level
IP1.0	PCT0	T2 capture register 0 priority interrupt level

Interrupt priority levels are as follows: "0" – low priority
"1" – high priority

FUNCTIONAL DESCRIPTION (continued)

Table 3 shows the interrupt vectors. The vector indicates the ROM location where the appropriate interrupt service routine starts.

Table 3 Interrupt vectors

Source		Vector
External 0	X0	0003H
Timer 0 overflow	T0	000BH
External 1	X1	0013H
Timer 1 overflow	T1	001BH
Serial I/O 0 (UART)	S0	0023H
Serial I/O 1 (I^2C)	S1	002BH
T2 capture 0	CT0	0033H
T2 capture 1	CT1	003BH
T2 capture 2	CT2	0043H
T2 capture 3	CT3	004BH
ADC completion	ADC	0053H
T2 compare 0	CM0	005BH
T2 compare 1	CM1	0063H
T2 compare 2	CM2	006BH
T2 overflow	T2	0073H

Interrupt priority

Each interrupt source can be either high priority or low priority. If both priorities are requested simultaneously, the processor will branch to the high priority vector. If there are simultaneous requests from sources of the same priority, then interrupts will be serviced in the following order:

X0, S1, ADC, T0, CT0, CM0, X1, CT1, CM1, T1, CT2, CM2, S0, CT3, T2

A low priority interrupt routine can only be interrupted by a high priority interrupt. A high priority interrupt routine can not be interrupted.

Oscillator circuitry

The oscillator circuitry of the PCB83C552 is a single-stage inverting amplifier in a Pierce oscillator configuration. The circuitry between XTAL 1 and XTAL 2 is basically an inverter biased to the transfer point. Either a crystal or ceramic resonator can be used as the feedback element to complete the oscillator circuitry. Both are operated in parallel resonance. XTAL 1 (pin 35) is the high gain amplifier input, and XTAL 2 (pin 34) is the output (see Fig. 14). To drive the PCB83C552 externally, XTAL 1 is driven from an external source and XTAL 2 left open-circuit (see Fig. 15).

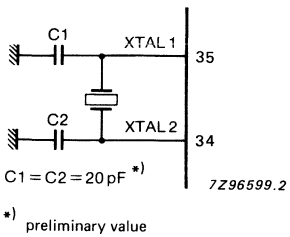


Fig. 14 PCB83C552 oscillator circuit.

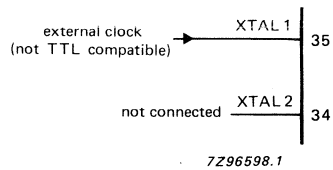


Fig. 15 Driving the PCB83C552 from an external source.

DEVELOPMENT DATA

Reset circuitry (see Fig. 16)

The reset circuitry for the PCB83C552 is connected to the reset pin RST. A Schmitt trigger is used at the input for noise rejection. The output of the Schmitt trigger is sampled by the reset circuitry every machine cycle.

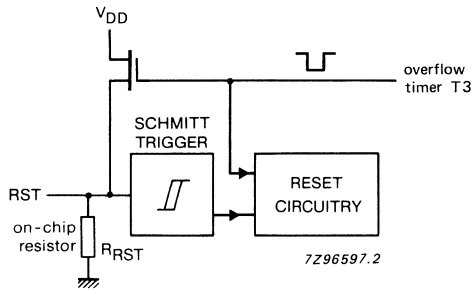


Fig. 16 On-chip reset configuration.

A reset is accomplished by holding the RST pin HIGH for at least two machine cycles (24 oscillator periods). The CPU responds by executing an internal reset. During reset ALE and $\overline{PSEN}$ output a HIGH level. In order to perform a correct reset, this level must not be affected by external elements.

Also with the PCB83C552, the RST line can be pulled HIGH internally by a pull-up transistor activated by the watchdog timer T3. The length of the output pulse from T3 is 3 machine cycles. A pulse of such short duration is necessary in order to recover from a processor or system fault as fast as possible.

FUNCTIONAL DESCRIPTION (continued)

N.B. It can be seen that the short reset pulse from Timer T3 cannot discharge the power-on reset capacitor (see Fig. 17). Consequently, when the watchdog timer is also used to reset external devices this capacitor arrangement should not be connected to the RST pin, and an extra circuit should be used to perform the power-on reset operation. It should be remembered that a Timer T3 overflow, if enabled, will force a reset condition to the PCB83C552 by an internal connection, whether the output RST is tied LOW or not.

The internal reset is executed during the second cycle in which RST is HIGH and is repeated every cycle until RST goes LOW. It leaves the internal registers as follows:

Register	Content
ACC	0000 0000
ADCON	xx00 0000
ADCH	xxxx xxxx
B	0000 0000
CML0 - CML2	0000 0000
CMH0 - CMH2	0000 0000
CTCON	0000 0000
CTL0 - CTL3	xxxx xxxx
CTH0 - CTH3	xxxx xxxx
DPL	0000 0000
DPH	0000 0000
IEN0	0000 0000
IEN1	0000 0000
IP0	x000 0000
IP1	0000 0000
PCH	0000 0000
PCL	0000 0000
PCON	0xx0 0000
PSW	0000 0000
PWM0	0000 0000
PWM1	0000 0000
PWMP	0000 0000
P0 - P4	1111 1111
P5	xxxx xxxx
RTE	0000 0000
S0BUF	xxxx xxxx
S0CON	0000 0000
S1ADR	0000 0000
S1CON	x000 0000
S1DAT	0000 0000
S1STA	1111 1000
SP	0000 0111
STE	xx00 0000
TCON	0000 0000
TH0, TH1	0000 0000
TMH2	0000 0000
TL0, TL1	0000 0000
TML2	0000 0000
TMOD	0000 0000
TM2CON	0000 0000
TM2IR	0111 0000
T3	0000 0000

The internal RAM is not affected by reset. When V_{DD} is turned on, the RAM content is indeterminate.

Power-on reset (see Fig. 17)

When V_{DD} is turned on, and provided its rise-time does not exceed 10 ms, an automatic reset can be obtained by connecting the RST pin to V_{DD} via a 2,2 μF capacitor. When the power is switched on, the voltage on the RST pin is equal to V_{DD} minus the capacitor voltage, and decreases from V_{DD} as the capacitor charges through the internal resistor (R_{RST}) to ground. The larger the capacitor, the more slowly V_{RST} decreases. V_{RST} must remain above the lower threshold of the Schmitt trigger long enough to effect a complete reset. The time required is the oscillator start-up time, plus 2 machine cycles.

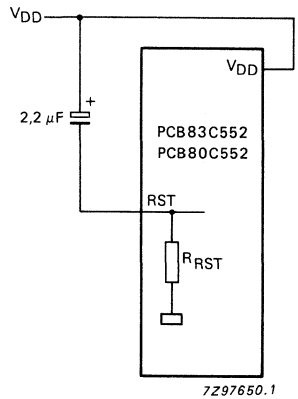


Fig. 17 Power-on reset.

INSTRUCTION SET

Table 4 Instruction set description

mnemonic		description	bytes/ cycles		opcode (hex.)
Arithmetic operations					
ADD	A,Rr	Add register to A	1	1	2*
ADD	A,direct	Add direct byte to A	2	1	25
ADD	A,@Ri	Add indirect RAM to A	1	1	26, 27
ADD	A,#data	Add immediate data to A	2	1	24
ADDC	A,Rr	Add register to A with carry flag	1	1	3*
ADDC	A,direct	Add direct byte to A with carry flag	2	1	35
ADDC	A,@Ri	Add indirect RAM to A with carry flag	1	1	36, 37
ADDC	A,#data	Add immediate data to A with carry flag	2	1	34
SUBB	A,Rr	Subtract register from A with borrow	1	1	9*
SUBB	A,direct	Subtract direct byte from A with borrow	2	1	95
SUBB	A,@Ri	Subtract indirect RAM from A with borrow	1	1	96, 97
SUBB	A,#data	Subtract immediate data from A with borrow	2	1	94
INC	A	Increment A	1	1	04
INC	Rr	Increment register	1	1	0*
INC	direct	Increment direct byte	2	1	05
INC	@Ri	Increment indirect RAM	1	1	06, 07
DEC	A	Decrement A	1	1	14
DEC	Rr	Decrement register	1	1	1*
DEC	direct	Decrement direct byte	2	1	15
DEC	@Ri	Decrement indirect RAM	1	1	16, 17
INC	DPTR	Increment data pointer	1	2	A3
MUL	AB	Multuply A & B	1	4	A4
DIV	AB	Divide A by B	1	4	84
DA	A	Decimal adjust A	1	1	D4

mnemonic		description	bytes/ cycles		opcode (hex.)
Logic operations					
ANL	A,Rr	AND register to A	1	1	5*
ANL	A,direct	AND direct byte to A	2	1	55
ANL	A,@Ri	AND indirect RAM to A	1	1	56, 57
ANL	A,#data	AND immediate data to A	2	1	54
ANL	direct,A	AND A to direct byte	2	1	52
ANL	direct,#data	AND immediate data to direct byte	3	2	53
ORL	A,Rr	OR register to A	1	1	4*
ORL	A,direct	OR direct byte to A	2	1	45
ORL	A,@Ri	OR indirect RAM to A	1	1	46, 47
ORL	A,#data	OR immediate data to A	2	1	44
ORL	direct, A	OR A to direct byte	2	1	42
ORL	direct,#data	OR immediate data to direct byte	3	2	43
XRL	A,Rr	Exclusive-OR register to A	1	1	6*
XRL	A,direct	Exclusive-OR direct byte to A	2	1	65
XRL	A,@Ri	Exclusive-OR indirect RAM to A	1	1	66, 67
XRL	A,#data	Exclusive-OR immediate data to A	2	1	64
XRL	direct,A	Exclusive-OR A to direct byte	2	1	62
XRL	direct,#data	Exclusive-OR immediate data to direct byte	3	2	63
CLR	A	Clear A	1	1	E4
CPL	A	Complement A	1	1	F4
RL	A	Rotate A left	1	1	23
RLC	A	Rotate A left through the carry flag	1	1	33
RR	A	Rotate A right	1	1	03
RRC	A	Rotate A right through the carry flag	1	1	13
SWAP	A	Swap nibbles within A	1	1	C4

INSTRUCTION SET (continued)

mnemonic		description	bytes/ cycles		opcode (hex.)
Data transfer					
MOV	A,Rr	Move register to A	1	1	E*
MOV	A,direct**	Move direct byte to A	2	1	E5
MOV	A,@Ri	Move indirect RAM to A	1	1	E6, E7
MOV	A,#data	Move immediate data to A	2	1	74
MOV	Rr,A	Move A to register	1	1	F*
MOV	Rr,direct	Move direct byte to register	2	2	A*
MOV	Rr,#data	Move immediate data to register	2	1	7*
MOV	direct,A	Move A to direct byte	2	1	F5
MOV	direct,Rr	Move register to direct byte	2	2	8*
MOV	direct,direct	Move direct byte to direct byte	3	2	85
MOV	direct,@Ri	Move indirect RAM to direct byte	2	2	86, 87
MOV	direct,#data	Move immediate data to direct byte	3	2	75
MOV	@Ri,A	Move A to indirect RAM	1	1	F6, F7
MOV	@Ri,direct	Move direct byte to indirect RAM	2	2	A6, A7
MOV	@Ri,#data	Move immediate data to indirect RAM	2	1	76, 77
MOV	DPTR,#data16	Load data pointer with a 16-bit constant	3	2	90
MOVC	A,@A+DPTR	Move code byte relative to DPTR to A	1	2	93
MOVC	A,@A+PC	Move code byte relative to PC to A	1	2	83
MOVX	A,@Ri	Move external RAM (8-bit address) to A	1	2	E2, E3
MOVX	A,@DPTR	Move external RAM (16-bit address) to A	1	2	E0
MOVX	@Ri,A	Move A to external RAM (8-bit address)	1	2	F2, F3
MOVX	@DPTR,A	Move A to external RAM (16-bit address)	1	2	F0
PUSH	direct	Push direct byte onto stack	2	2	C0
POP	direct	Pop direct byte from stack	2	2	D0
XCH	A,Rr	Exchange register with A	1	1	C*
XCH	A,direct	Exchange direct byte with A	2	1	C5
XCH	A,@Ri	Exchange indirect RAM with A	1	1	C6, C7
XCHD	A,@Ri	Exchange LOW-order nibble indirect RAM with A	1	1	D6, D7

** MOV A,ACC is not permitted.

mnemonic		description	bytes/ cycles		opcode (hex.)
Boolean variable manipulation					
CLR	C	Clear carry flag	1	1	C3
CLR	bit	Clear direct bit	2	1	C2
SETB	C	Set carry flag	1	1	D3
SETB	bit	Set direct bit	2	1	D2
CPL	C	Complement carry flag	1	1	B3
CPL	bit	Complement direct bit	2	1	B2
ANL	C,bit	AND direct bit to carry flag	2	2	82
ANL	C,/bit	AND complement of direct bit to carry flag	2	2	B0
ORL	C,bit	OR direct bit to carry flag	2	2	72
ORL	C,/bit	OR complement of direct bit to carry flag	2	2	A0
MOV	C,bit	Move direct bit to carry flag	2	1	A2
MOV	bit,C	Move carry flag to direct bit	2	2	92
Program and machine control					
ACALL	addr11	Absolute subroutine call	2	2	●1addr
LCALL	addr16	Long subroutine call	3	2	12
RET		Return from subroutine	1	2	22
RETI		Return from interrupt	1	2	32
AJMP	addr11	Absolute jump	2	2	▲1addr
LJMP	addr16	Long jump	3	2	02
SJMP	rel	Short jump (relative address)	2	2	80
JMP	@A+DPTR	Jump indirect relative to the DPTR	1	2	73
JZ	rel	Jump if A is zero	2	2	60
JNZ	rel	Jump if A is not zero	2	2	70
JC	rel	Jump if carry flag is set	2	2	40
JNC	rel	Jump if carry flag is not set	2	2	50
JB	bit,rel	Jump if direct bit is set	3	2	20
JNB	bit,rel	Jump if direct bit is not set	3	2	30
JBC	bit,rel	Jump if direct bit is set and clear bit	3	2	10
CJNE	A,direct,rel	Compare direct to A and jump if not equal	3	2	B5
CJNE	A,#data,rel	Compare immediate to A and jump if not equal	3	2	B4
CJNE	Rr,#data,rel	Compare immediate to reg. and jump if not equal	3	2	B*
CJNE	@Ri,#data,rel	Compare immediate to ind. and jump if not equal	3	2	B6, B7
DJNZ	Rr,rel	Decrement register and jump if not zero	2	2	D*
DJNZ	direct,rel	Decrement direct and jump if not zero	3	2	D5
NOP		No operation	1	1	00

Notes to Table 4

Data addressing modes

Rr	Working register R0-R7.
direct	128 internal RAM locations and any special function register (SFR).
@Ri	Indirect internal RAM location addressed by register R0 or R1 of the actual register bank.
#data	8-bit constant included in instruction.
#data16	16-bit constant included as bytes 2 and 3 of instruction.
bit	direct addressed bit in internal RAM or SFR.
addr16	16-bit destination address. Used by LCALL and LJMP. The branch will be anywhere within the 64 K-byte program memory address space.
addr11	11-bit destination address. Used by ACALL and AJMP. The branch will be within the same 2 K-byte page of program memory as the first byte of the following instruction.
rel	Signed (two's complement) 8-bit offset byte. Used by SJMP and all conditional jumps. Range is −128 to + 127 bytes relative to first byte of the following instruction.

Hexadecimal opcode cross-reference to Table 5

* : 8, 9, A, B, C, D, E, F.
● : 11, 31, 51, 71, 91, B1, D1, F1.
▲ : 01, 21, 41, 61, 81, A1, C1, E1.

DEVELOPMENT DATA

Table 5 Instruction map

first hexadecimal character of opcode ↓ | second hexadecimal character of opcode →

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	NOP	AJMP addr11	LJMP addr16	RR A	INC A	INC dir	INC @Ri 0	1	INC Rr 0	1	2	3	4	5	6	7
1	JBC bit,rel	ACALL addr11	LCALL addr16	RRC A	DEC A	DEC dir	DEC @Ri 0	1	DEC Rr 0	1	2	3	4	5	6	7
2	JB bit,rel	AJMP addr11	RET	RL A	ADD A,#data	ADD A,dir	ADD A,@Ri 0	1	ADD A,Rr 0	1	2	3	4	5	6	7
3	JNB bit,rel	ACALL addr11	RETI	RLC A	ADDC A,#data	ADDC A,dir	ADDC A,@Ri 0	1	ADDC A,Rr 0	1	2	3	4	5	6	7
4	JC rel	AJMP addr11	ORL dir,A	ORL dir,#data	ORL A,#data	ORL A,dir	ORL A,@Ri 0	1	ORL A,Rr 0	1	2	3	4	5	6	7
5	JNC rel	ACALL addr11	ANL dir,A	ANL dir,#data	ANL A,#data	ANL A,dir	ANL A,@Ri 0	1	ANL A,Rr 0	1	2	3	4	5	6	7
6	JZ rel	AJMP addr11	XRL dir,A	XRL dir,#data	XRL A,#data	XRL A,dir	XRL A,@Ri 0	1	XRL A,Rr 0	1	2	3	4	5	6	7
7	JNZ rel	ACALL addr11	ORL C,bit	JMP @A+DPTR	MOV A,#data	MOV dir,#data	MOV @Ri,#data 0	1	MOV Rr,#data 0	1	2	3	4	5	6	7
8	SJMP rel	AJMP addr11	ANL C,bit	MOVC A,@A+PC	DIV AB	MOV dir,dir	MOV dir,@Ri 0	1	MOV dir,Rr 0	1	2	3	4	5	6	7
9	MOV DPTR, #data 16	ACALL addr11	MOV bit,C	MOVC A,@A+DPTR	SUBB A,#data	SUBB A,dir	SUBB A,@Ri 0	1	SUBB A,Rr 0	1	2	3	4	5	6	7
A	ORL C,/bit	AJMP addr11	MOV C,bit	INC DPTR	MUL AB		MOV @Ri,dir 0	1	MOV Rr,dir 0	1	2	3	4	5	6	7
B	ANL C,/bit	ACALL addr11	CPL bit	CPL C	CJNE A, #data, rel	CJNE A,dir,rel	CJNE @Ri,#data, rel 0	1	CJNE Rr,#data, rel 0	1	2	3	4	5	6	7
C	PUSH dir	AJMP addr11	CLR bit	CLR C	SWAP A	XCH A,dir	XCH A,@Ri 0	1	XCH A,Rr 0	1	2	3	4	5	6	7
D	POP dir	ACALL addr11	SETB bit	SETB C	DA A	DJNZ dir,rel	XCHD A,@Ri 0	1	DJNZ Rr, rel 0	1	2	3	4	5	6	7
E	MOVX A,@DPTR	AJMP addr11	MOVX A,@Ri 0	1	CLR A	MOV * A,dir	MOV A,@Ri 0	1	MOV A,Rr 0	1	2	3	4	5	6	7
F	MOVX @DPTR,A	ACALL addr11	MOVX @Ri,A 0	1	CPL A	MOV dir,A	MOV @Ri,A 0	1	MOV Rr,A 0	1	2	3	4	5	6	7

* MOV A,ACC is not a valid instruction.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Input voltage on any pin with respect to ground (V_{SS})	V_I	−0,5 to + 6,5	V
Input, output current	$\pm I_I, I_O$	max. 5	mA
Input, output current on any single pin	$\pm I_I, I_O$	max. 10	mA
Total power dissipation	P_{tot}	max. 1	W
Storage temperature range	T_{stg}	−65 to + 150	°C
Operating ambient temperature range	T_{amb}	0 to + 70	°C

D.C. CHARACTERISTICS

V_{DD} = 5 V (± 10%); V_{SS} = 0 V; T_{amb} = 0 to + 70 °C; all voltages with respect to V_{SS} unless otherwise specified.

parameter	symbol	min.	max.	unit	conditions
Supply voltage	V_{DD}	4,5	5,5	V	
Supply current					
operating (note 1)	I_{DD}	–	tbf	mA	f_{CLK} = 12 MHz
Idle mode (note 2)	I_{DD}	–	tbf	mA	f_{CLK} = 12 MHz
Power-down current (note 3)	I_{PD}	–	tbf	µA	V_{DD} = 2 - 6 V
Inputs					
LOW level input voltage (except $\overline{EA}$, P1.6/SCL, P1.7/SDA)	V_{IL}	−0,5	$0,2V_{DD}-0,1$	V	
LOW level input voltage ($\overline{EA}$)	V_{IL1}	−0,5	$0,2V_{DD}-0,3$	V	
LOW level input voltage (note 6) (P1.6/SCL, P1.7/SDA)	V_{IL2}	−0,5	1,5	V	
HIGH level input voltage (except XTAL 1, RST, P1.6/SCL, P1.7/SDA)	V_{IH}	$0,2V_{DD}+0,9$	$V_{DD}+0,5$	V	
HIGH level input voltage (XTAL 1, RST)	V_{IH1}	$0,7V_{DD}$	$V_{DD}+0,5$	V	
HIGH level input voltage (note 6) (P1.6/SCL, P1.7/SDA)	V_{IH2}	3,0	6	V	
Input current logic 0 (Ports 1, 2, 3 and 4; except P1.6/SCL, P1.7/SDA)	$-I_{IL}$	–	50	µA	V_I = 0,45 V
Input current logic 1 to 0 transition (Ports 1, 2, 3 and 4; except P1.6/SCL P1.7/SDA)	$-I_{TL}$	–	650	µA	V_I = 2 V
Input leakage current (Port 0, Port 5, $\overline{EA}$, STADC, $\overline{EW}$)	$\pm I_{LI1}$	–	10	µA	$0,45 V < V_I < V_{DD}$

DEVELOPMENT DATA

parameter	symbol	min.	max.	unit	conditions
Outputs					
Input leakage current (P1.6/SCL, P1.7/SDA	$\pm I_{LI2}$	–	10	μA	$0\ V < V_I < 6\ V$ $0\ V < V_{DD} < 5{,}5\ V$
LOW level output voltage (note 4) (Ports 1, 2, 3 and 4; except P1.6/SCL, P1.7/SDA	V_{OL}	–	0,45	V	I_{OL} = 1,6 mA
LOW level output voltage (note 4) (Port 0, ALE, $\overline{PSEN}$, $\overline{PWM0}$, $\overline{PWM1}$)	V_{OL1}	–	0,45	V	I_{OL} = 3,2 mA
LOW level output voltage (P1.6/SCL, P1.7/SDA	V_{OL2}	–	0,4	V	I_{OL} = 3,0 mA
HIGH level output voltage (Ports 1, 2, 3 and 4; except P1.6/SCL, P1.7/SDA	V_{OH}	2,4	–	V	$-I_{OH}$ = 60 μA; V_{DD} = 5 V ± 10%
		$0{,}75V_{DD}$	–	V	$-I_{OH}$ = 25 μA
		$0{,}9V_{DD}$	–	V	$-I_{OH}$ = 10 μA
HIGH level output voltage (note 5) (Port 0 in external Bus mode, ALE, $\overline{PSEN}$, $\overline{PWM0}$, $\overline{PWM1}$)	V_{OH1}	2,4	–	V	$-I_{OH}$ = 400 μA; V_{DD} = 5 V ± 10%
		$0{,}75V_{DD}$	–	V	$-I_{OH}$ = 150 μA
		$0{,}9V_{DD}$	–	V	$-I_{OH}$ = 40 μA
HIGH level output voltage (RST)	V_{OH2}	2,4	–	V	$-I_{OH}$ = 350 μA
		$0{,}75V_{DD}$	–	V	$-I_{OH}$ = 60 μA
RST pull-down resistor	R_{RST}	50	150	kΩ	
I/O pin capacitance	$C_{I/O}$	–	10	pF	test freq. = 1 MHz T_{amb} = 25 °C

D.C. CHARACTERISTICS (continued)

AV_{DD} = 5,0 V ± 10%; AV_{SS} = 0 V; V_{REF} = 5,0 V; T_{amb} = 0 °C to + 70 °C unless otherwise specified

parameter	symbol	min.	max.	unit	conditions
Analogue inputs					
Analogue supply voltage (note 8)	AV_{DD}	4,5	5,5	V	$AV_{DD} = V_{DD} \pm 0{,}2$ V
Analogue supply current					
operating	AI_{DD}	–	1,0	mA	Port 5 = 1,4 V
Idle mode	AI_{ID}	–	tbf	µA	
Power-down (note 8)	AI_{PD}	–	tbf	µA	AV_{DD} = 2 - 6 V
Analogue input voltage	AV_{IN}	$AV_{SS}-0{,}2$	$AV_{DD}+0{,}2$	V	
Reference voltage	AV_{REF-}	$AV_{SS}-0{,}2$	–	V	
	AV_{REF+}	–	$AV_{DD}+0{,}2$	V	
Resistance between AV_{REF+} and AV_{REF-}	R_{REF}	tbf	tbf	kΩ	
Analogue input capacitance	C_{IA}	tbf	tbf	pF	
Sampling time	t_{ADS}	–	$8t_{CY}$	µs	
Conversion time (including sample time)	t_{ADC}	–	$50t_{CY}$	µs	
Differential non-linearity (note 7)	DL_e	–	± 1	LSB	
Integral non-linearity (note 7)	IL_e	–	± 1	LSB	
Offset error (note 7)	OS_e	–	tbf	mV	
Gain error (note 7)	G_e	–	tbf	%	
Channel to channel matching	M_{ctc}		± 1	LSB	
Crosstalk (note 9)	C_t	–	tbf	dB	0 - 100 kHz

Notes to the d.c. characteristics

1. The operating supply current is measured with all output pins disconnected; XTAL 1 driven with $t_r = t_f$ = 10 ns; $V_{IL} = V_{SS}$ + 0,5 V; $V_{IH} = V_{DD}$ –0,5 V; XTAL 2 not connected; $\overline{EA}$ = RST = Port 0 = P1.6 = P1.7 = $\overline{EW}$ = V_{DD}; STADC = V_{SS}.
2. The Idle mode supply current is measured with all output pins disconnected; XTAL 1 driven with $t_r = t_f$ = 10 ns; $V_{IL} = V_{SS}$ + 0,5 V; $V_{IH} = V_{DD}$ –0,5 V; XTAL 2 not connected; $\overline{EA}$ = Port 0 = P1.6 = P1.7 = $\overline{EW}$ = V_{DD}; RST = STADC = V_{SS}.
3. The power down current is measured with all output pins disconnected; XTAL 2 not connected; $\overline{EA}$ = Port 0 = P1.6 = P1.7 = $\overline{EW}$ = V_{DD}; RST = STADC = V_{SS}.
4. Capacitive loading on Port 0 and Port 2 may cause spurious noise pulses to be superimposed on the LOW level output voltage of ALE, Port 1 and Port 3. The noise is due to external bus capacitance discharging into the Port 0 and Port 2 pins when these pins make a 1-to-0 transition during bus operations. In the most adverse condition (capacitive loading > 100 pF) the noise pulse on ALE line may exceed 0,8 V. In this event it may be required to qualify ALE with a Schmitt trigger, or use an address latch with a Schmitt trigger STROBE input.
5. Capacitive loading on Port 0 and Port 2 may cause the HIGH level output voltage on ALE and $\overline{PSEN}$ to momentarily fall below the 0,9 V_{DD} specification when the address bits are stabilizing.
6. The input threshold voltage of P1.6 and P1.7 (SIO1) meets the I^2C specification, so an input voltage below 1,5 V will be recognized as a logic 0 while an input voltage above 3,0 V will be recognized as a logic 1.
7. Conditions: AV_{REF+} = 5,12 V; AV_{REF-} = 0 V; AV_{DD} = 5,0 V
8. The following condition always applies: $V_{DD}-0{,}2$ V < AV_{DD} < $V_{DD}+0{,}2$ V.
9. This should be considered when both analogue and digital signals are simultaneously input to port 5.

A.C. CHARACTERISTICS

V_{DD} = 5 V ± 10%; V_{SS} = 0 V; T_{amb} = 0 to + 70 °C; C_L = 100 pF (Port 0, ALE and $\overline{PSEN}$; C_L = 80 pF (all other outputs); unless otherwise specified (see waveforms Figs 19, 20 and 21)

parameter	symbol	10 MHz		12 MHz		variable clock		unit
		min.	max.	min.	max.	min.	max.	
Program memory								
ALE pulse duration	t_{LL}	160	–	127	–	$2t_{CK}-40$	–	ns
Address set-up time to ALE	t_{AL}	45	–	28	–	$t_{CK}-55$	–	
Address hold time after ALE	t_{LA}	65	–	48	–	$t_{CK}-35$	–	ns
Time from ALE to valid instruction input	t_{LIV}	–	300	–	233	–	$4t_{CK}-100$	ns
Time from ALE to control pulse $\overline{PSEN}$	t_{LC}	60	–	43	–	$t_{CK}-40$	–	ns
Control pulse duration $\overline{PSEN}$	t_{CC}	255	–	205	–	$3t_{CK}-45$	–	ns
Time from $\overline{PSEN}$ to valid instruction input	t_{CIV}	–	195	–	145	–	$3t_{CK}-105$	ns
Input instruction hold time after $\overline{PSEN}$	t_{CI}	0	–	0	–	0	–	ns
Input instruction float delay after $\overline{PSEN}$	t_{CIF}	–	75	–	59	–	$t_{CK}-25$	ns
Address to valid instruction input	t_{AIV}	–	395	–	312	–	$5t_{CK}-105$	ns
Address float delay after $\overline{PSEN}$	t_{AFC}	–	10	–	10	–	10	ns

DEVELOPMENT DATA

A.C. CHARACTERISTICS (continued)

parameter	symbol	10 MHz		12 MHz		variable clock		unit
		min.	max.	min.	max.	min.	max.	
External data memory								
$\overline{RD}$ pulse duration	t_{RR}	500	–	400	–	$6t_{CK}-100$	–	ns
$\overline{WR}$ pulse duration	t_{WW}	500	–	400	–	$6t_{CK}-100$	–	ns
Address set up time to ALE	t_{AL}	60	–	43	–	$t_{CK}-40$		ns
Address hold time after ALE	t_{LA}	65	–	48	–	$t_{CK}-35$	–	ns
$\overline{RD}$ to valid data input	t_{RD}	–	335	–	250	–	$5t_{CK}-165$	ns
Data hold time after $\overline{RD}$	t_{DR}	0	–	0	–	0	–	ns
Data float delay after $\overline{RD}$	t_{DFR}	–	130	–	97	–	$2t_{CK}-70$	ns
Time from ALE to valid data input	t_{LD}	–	650	–	517	–	$8t_{CK}-150$	ns
Address to valid data input	t_{AD}	–	735	–	585	–	$9t_{CK}-165$	ns
Time from ALE to $\overline{RD}$ or $\overline{WR}$	t_{LW}	250	350	200	300	$3t_{CK}-50$	$3t_{CK}+50$	ns
Time from address to $\overline{RD}$ or $\overline{WR}$	t_{AW}	270	–	203	–	$4t_{CK}-130$	–	ns
Time from $\overline{RD}$ or $\overline{WR}$ HIGH to ALE HIGH	t_{WHLH}	60	140	43	123	$t_{CK}-40$	$t_{CK}+40$	ns
Data valid to $\overline{WR}$ transition	t_{DWX}	40	–	23	–	$t_{CK}-60$	–	ns
Data set-up time before $\overline{WR}$	t_{DW}	550	–	433	–	$7t_{CK}-150$	–	ns
Data hold time after $\overline{WR}$	t_{WD}	50	–	33	–	$t_{CK}-50$	–	ns
Address float delay after $\overline{RD}$	t_{AFR}	–	12	–	12	–	12	ns

Where:

$1/t_{CK}$ = 3,5 to 12 MHz (see Fig. 19 and Table 6).

$t_{CY} = 12\ t_{CK}$ (see Fig. 20 and D.C. Characteristics).

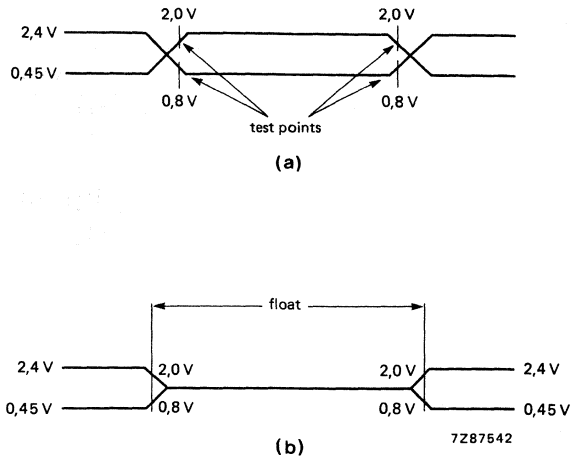


Fig. 18 A.C. testing input, output waveform (a) and float waveform (b).

A.C. testing inputs are driven at 2,4 V for a logic 1 and 0,45 V for a logic 0. Timing measurements are taken at 2,0 V for a logic 1 and 0,8 V for logic 0. The float state is defined as the point at which a Port 0 pin sinks 3,2 mA or sources 400 μA at the voltage test levels.

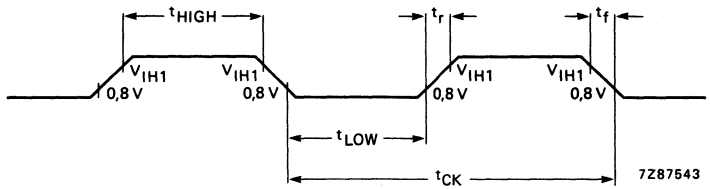


Fig. 19 External clock drive XTAL 1 (see Table 6).

Table 6 External clock drive XTAL 1 (see Fig. 19).

parameter	symbol	variable clock (f = 3,5 to 12 MHz)		unit
		min.	max.	
oscillator clock period	t_{CK}	83,3	286	ns
HIGH time	t_{HIGH}	20	t_{CK}-t_{LOW}	ns
LOW time	t_{LOW}	20	t_{CK}-t_{HIGH}	ns
rise time	t_r	–	20	ns
fall time	t_f	–	20	ns
cycle time	$t_{CY} = 12\ t_{CK}$	1	3,43	μs

A.C. CHARACTERISTICS (continued)

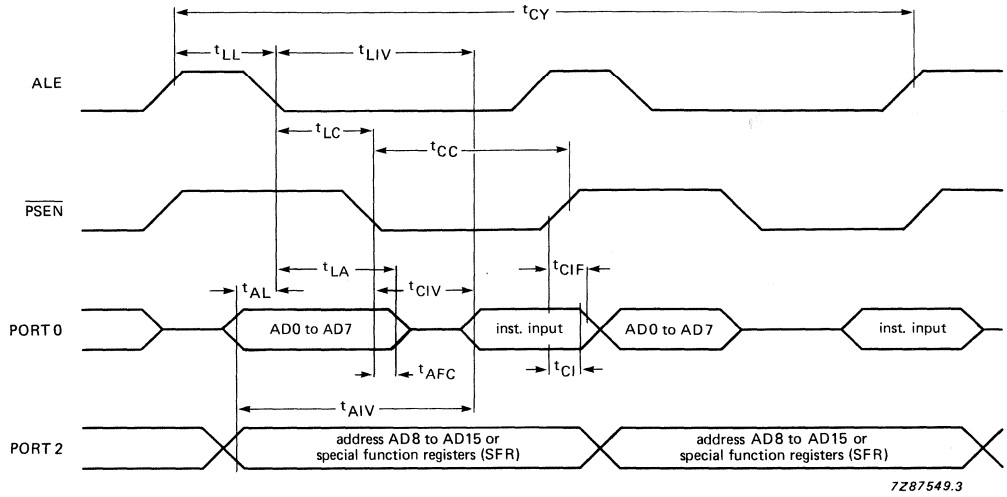


Fig. 20 Read from program memory.

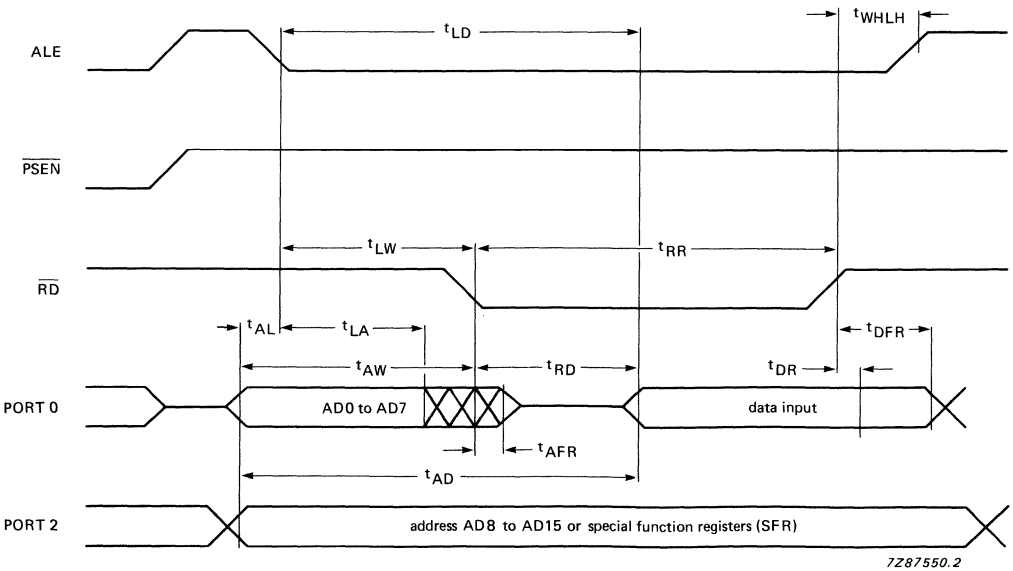


Fig. 21 Read from data memory.

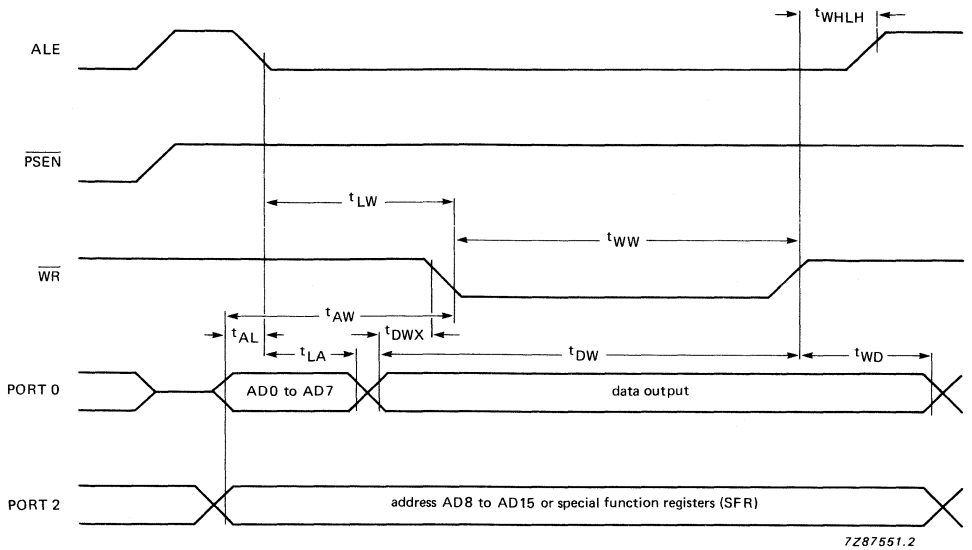


Fig. 22 Write to data memory.

A.C. CHARACTERISTICS (continued)

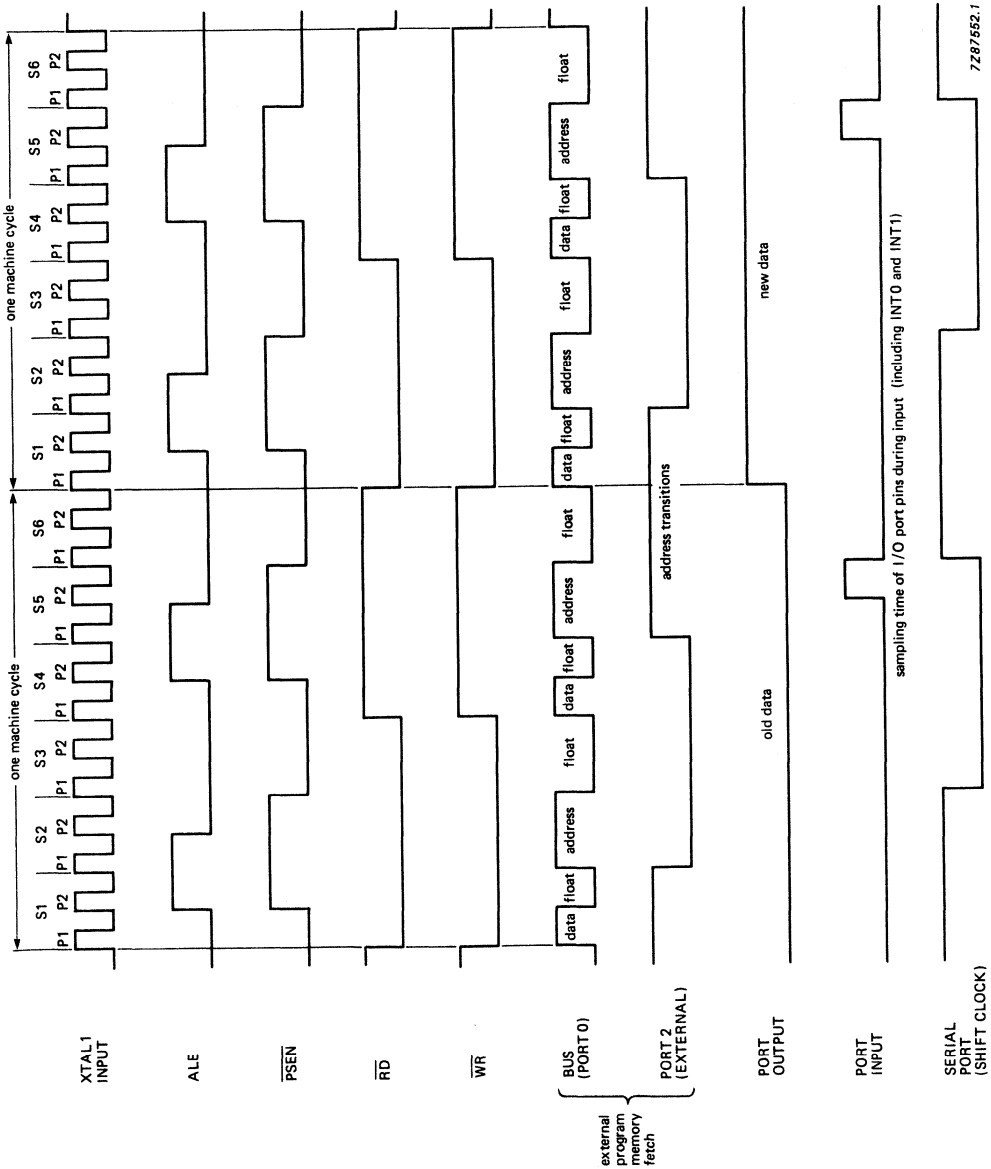


Fig. 23 Instruction cycle timing.

SINGLE-CHIP 8-BIT MICROCONTROLLER

GENERAL DESCRIPTION

The PCB83C652 single-chip 8-bit microcontroller is manufactured in an advanced CMOS process and is a derivative of the PCB80C51 microcontroller family. The PCB83C652 has the same instruction set as the PCB80C51. Two versions of the derivative exist although the generic term "PCB83C652" is used to refer to both family members:

- PCB83C652: 8 K bytes mask-programmable ROM, 256 bytes RAM
- PCB80C652: ROM-less version of the PCB83C652

This device provides architectural enhancements that make it applicable in a variety of applications in general control systems.

The PCB83C652 contains a non-volatile 8 K x 8 read-only program memory, a volatile 256 x 8 read/write data memory, four 8-bit I/O ports, two 16-bit timer/event counters (identical to the timers of the 80C51), a multi-source, two-priority-level, nested interrupt structure, an I^2C interface, UART and on-chip oscillator and timing circuits. For systems that require extra capability, the PCB83C652 can be expanded using standard TTL compatible memories and logic.

The device also functions as an arithmetic processor having facilities for both binary and BCD arithmetic plus bit-handling capabilities. The instruction set consists of over 100 instructions: 49 one-byte, 45 two-byte and 17 three-byte. With a 12 MHz crystal, 58% of the instructions are executed in 1 μs and 40% in 2 μs. Multiply and divide instructions require 4 μs.

Features

- 80C51 central processing unit
- 8 K x 8 ROM, expandable externally to 64 K bytes
- 256 x 8 RAM, expandable externally to 64 K bytes
- Two standard 16-bit timer/counters
- Four 8-bit I/O ports
- I^2C-bus serial I/O port with byte orientated master and slave functions
- Full-duplex UART facilities

- **A version for extended temperature range, extended frequency range (1,2 MHz - 12 MHz) is in preparation**

PACKAGE OUTLINES

PCB83C652P; PCB80C652P: 40-lead DIL; plastic (SOT-129).
PCB83C652WP; PCB80C652WP: 44-lead plastic leaded-chip-carrier (PLCC); (SOT-187).

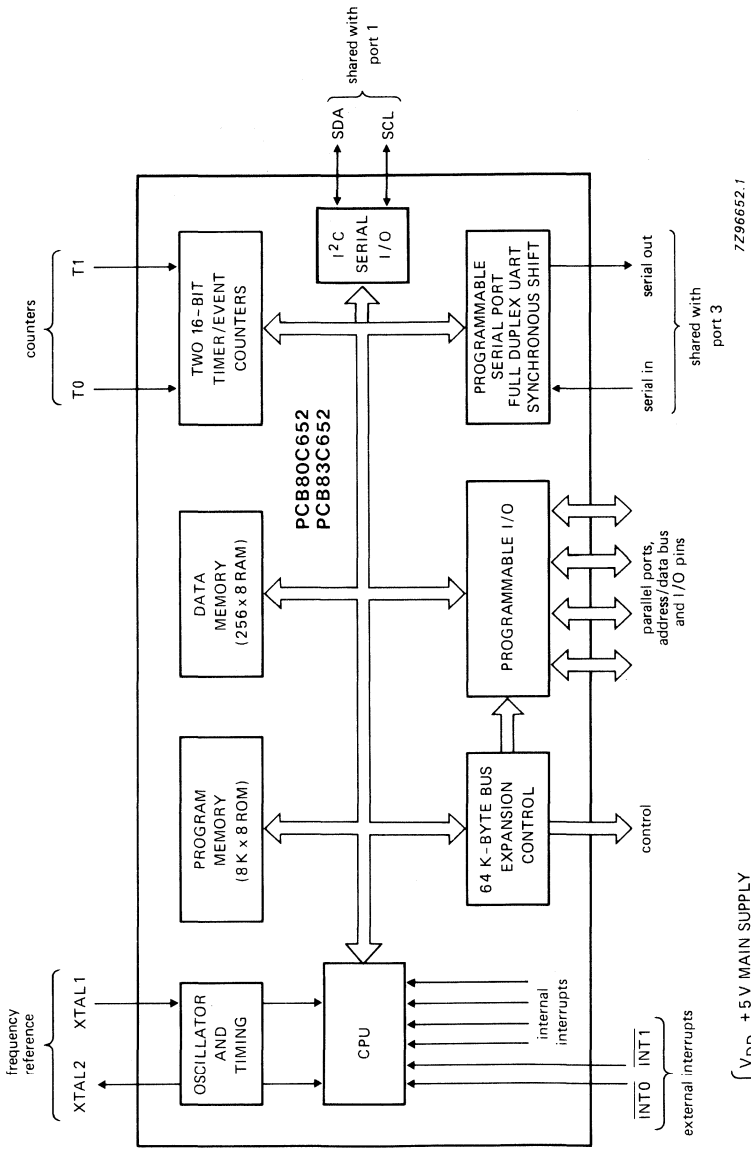


Fig. 1 Block diagram.

DEVELOPMENT DATA

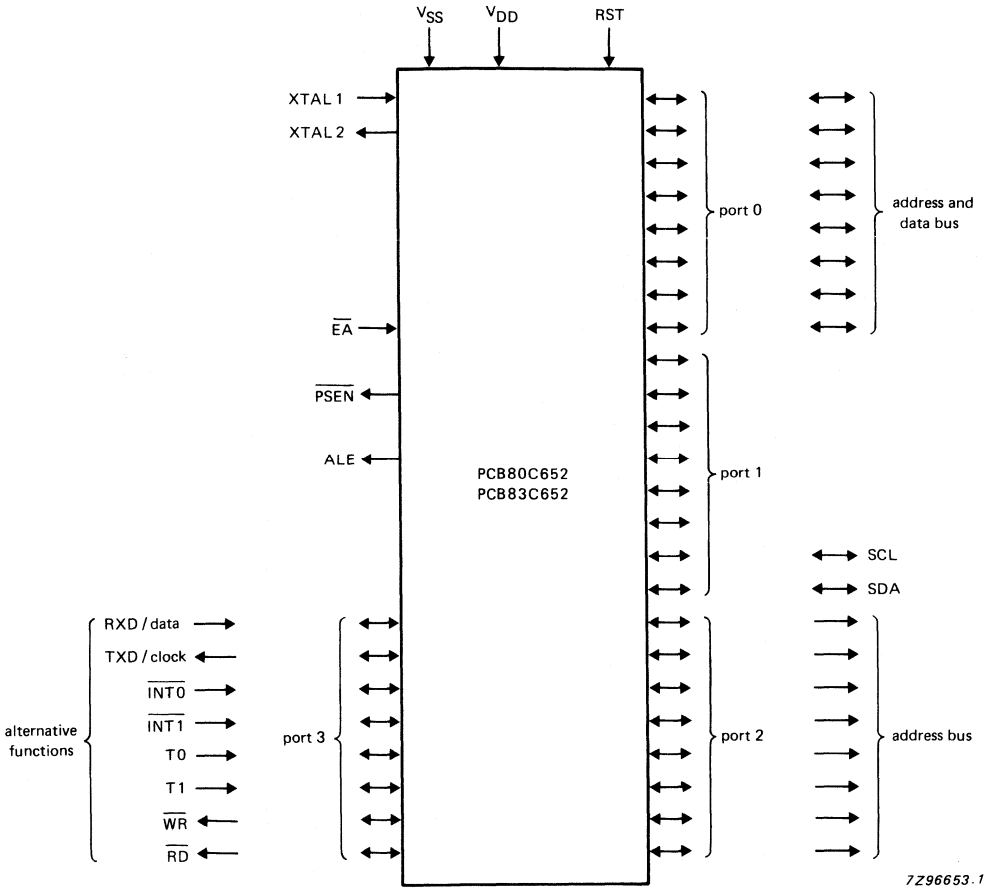


Fig. 2 Functional diagram.

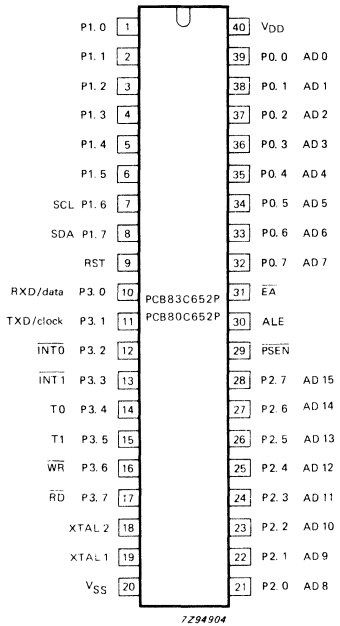


Fig. 3a Pinning diagram for PCB83C652P; PCB80C652P.

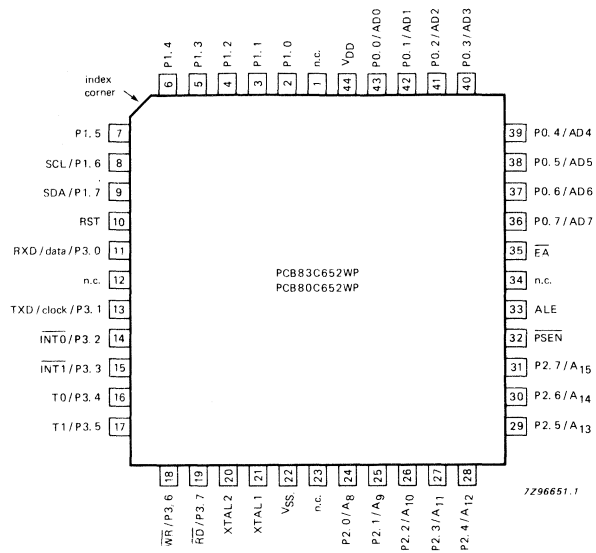


Fig. 3b Pinning diagram for PCB83C652WP; PCB80C652WP.

PINNING (PCB83C652P, PCB80C652P)

1-8	P1.0-P1.7	**Port 1:** 8-bit quasi-bidirectional I/O port. Port 1 can sink/source one TTL (= 4 LSTTL) input. It can drive CMOS inputs without external pull-ups, except P1.6 and P1.7 which have open drain outputs. Port pin — Alternative function P1.6 — SCL: I^2C-bus serial port clock line P1.7 — SDA: I^2C-bus serial port data line
9	RST	**RESET:** a high level on this pin for two machine cycles while the oscillator is running resets the device. An internal pull-down resistor permits Power-On reset using only a capacitor connected to V_{DD}.

10-17	P3.0-P3.7	**Port 3:** 8-bit quasi-bidirectional I/O port with internal pull-ups. It also serves the following alternative functions:

Port pin	Alternative function
P3.0	RXD/data: serial port receiver data input (asynchronous) or data input/output (synchronous)
P3.1	TXD/clock: serial port transmitter data output (asynchronous) or clock output (synchronous)
P3.2	$\overline{\text{INT0}}$: external interrupt 0 or gate control input for timer/event counter 0
P3.3	$\overline{\text{INT1}}$: external interrupt 1 or gate control input for timer/event counter 1
P3.4	T0: external input for timer/event counter 0
P3.5	T1: external input for timer/event counter 1
P3.6	$\overline{\text{WR}}$: external data memory write strobe
P3.7	$\overline{\text{RD}}$: external data memory read strobe

The generation or use of a Port 3 pin as an alternative function is carried out automatically by the PCB83C652 provided the associated Special Function Register bit is set high. Port 3 can sink/source one TTL (= 4 LSTTL) input. It can drive CMOS inputs without external pull-ups.

18	XTAL 2	**Crystal input 2:** output of the inverting amplifier that forms the oscillator. Left open-circuit when an external oscillator clock is used (see Figs 10 and 11).
19	XTAL 1	**Crystal input 1:** input to the inverting amplifier that forms the oscillator, and input to the internal clock generator. Receives the external oscillator clock signal when an external oscillator is used (see Figs 10 and 11).
20	V_{SS}	**Ground:** circuit ground potential.
21-28	P2.0-P2.7	**Port 2:** 8-bit quasi-bidirectional I/O port with internal pull-ups. During access to external memories (RAM/ROM) that use 16-bit addresses (MOVX @DPTR) Port 2 emits the high order address byte. When external RAM is accessed with an 8-bit address (MOVX @Ri) Port 2 emits the contents of the P2 special function register. Port 2 can sink/source one TTL (= 4 LSTTL) input. It can drive CMOS inputs without external pull-ups.
29	$\overline{\text{PSEN}}$	**Program Store Enable output:** read strobe to the external program memory via port 0 and 2. It is activated twice each machine cycle during fetches from external program memory. When executing out of external program memory two activations of $\overline{\text{PSEN}}$ are skipped during each access to external data memory. $\overline{\text{PSEN}}$ is not activated (remains HIGH) during no fetches from external program memory. $\overline{\text{PSEN}}$ can sink/source 8 LSTTL inputs. It can drive CMOS inputs without an external pull-up.
30	ALE	**Address Latch Enable output:** latches the low byte of the address during accesses to external memory in normal operation. It is activated every six oscillator periods except during an external data memory access. ALE can sink/source 8 LSTTL inputs. It can drive CMOS inputs without an external pull-up.

PINNING (continued)

31	$\overline{EA}$	**External Access input:** When $\overline{EA}$ is held at a TTL high level the CPU executes out of the internal program ROM provided the program counter is less than 8192. When $\overline{EA}$ is held at a TTL low level, the CPU executes out of external program memory via port 0 and port 2. $\overline{EA}$ is not allowed to float.
32-39	P0.7-P0.0	**Port 0:** 8-bit open drain bidirectional I/O port. It is also the multiplexed low-order address and data bus during accesses to external memory (during these accesses it activates internal pull-ups). Port 0 can sink/source eight LSTTL inputs.
40	V_{DD}	**Power supply:** + 5 V power supply pin during normal operation, Idle mode and Power-down mode.

To avoid a 'latch-up' effect at power-on, the voltage on any pin at any time must not be higher or lower than V_{DD} + 0,5 V or V_{SS} − 0,5 V respectively.

FUNCTIONAL DESCRIPTION

General

The PCB83C652 is a stand-alone high performance microcontroller designed for use in real-time applications such as instrumentation and industrial control.

The device provides, in addition to the 80C51 standard functions, a serial I^2C-bus interface. As well as the parallel bus, functions may also be expanded using the I^2C-bus utilizing the complete line of the I^2C clips family.

The PCB83C652 is a control-oriented CPU with on-chip program and data memory. It can be extended with external program memory up to 64 K bytes. It can also access up to 64 K bytes of external data memory. For systems requiring extra capability, the PCB83C652 can be expanded using standard memories and peripherals.

The PCB83C652 has two software selectable modes of reduced activity for further power reduction — Idle and Power-down. The Idle mode freezes the CPU while allowing the RAM, timers, serial ports and interrupt system to continue functioning. The Power-down mode saves the RAM contents but freezes the oscillator causing all other chip functions to be inoperative.

Memory organization

The central processing unit (CPU) manipulates operands in three memory spaces; these are the 64 K-byte external data memory, 256-byte internal data memory and the 64 K-byte internal and external program memory. The internal data memory address space is sub-divided into the 256-byte internal data RAM and 128-byte Special Function Register (SFR) address spaces, as shown in Fig. 4. Figure 5 shows the Special Function Register memory map. Internal RAM locations 0-127 are directly and indirectly addressable. Internal RAM locations 128-255 are only indirectly addressable. The special function register locations 128-255 are only directly addressable.

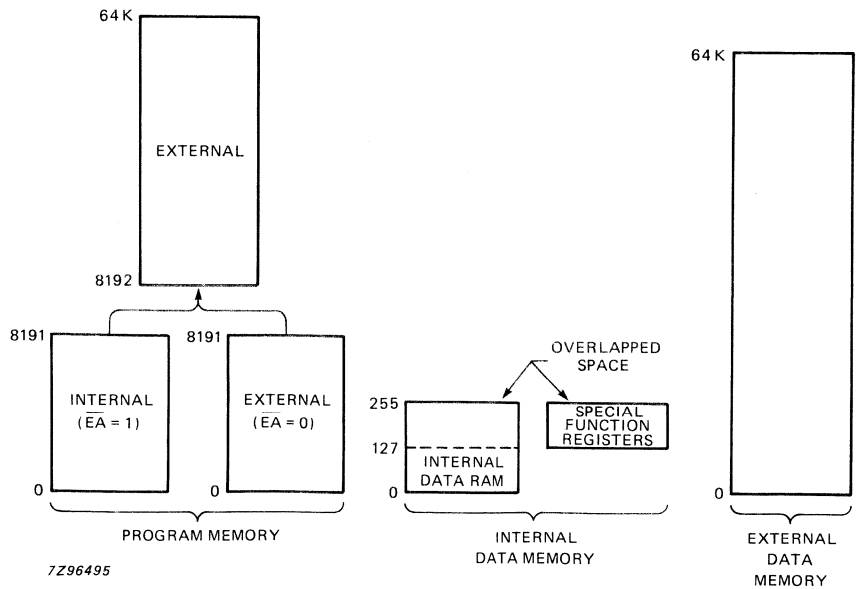
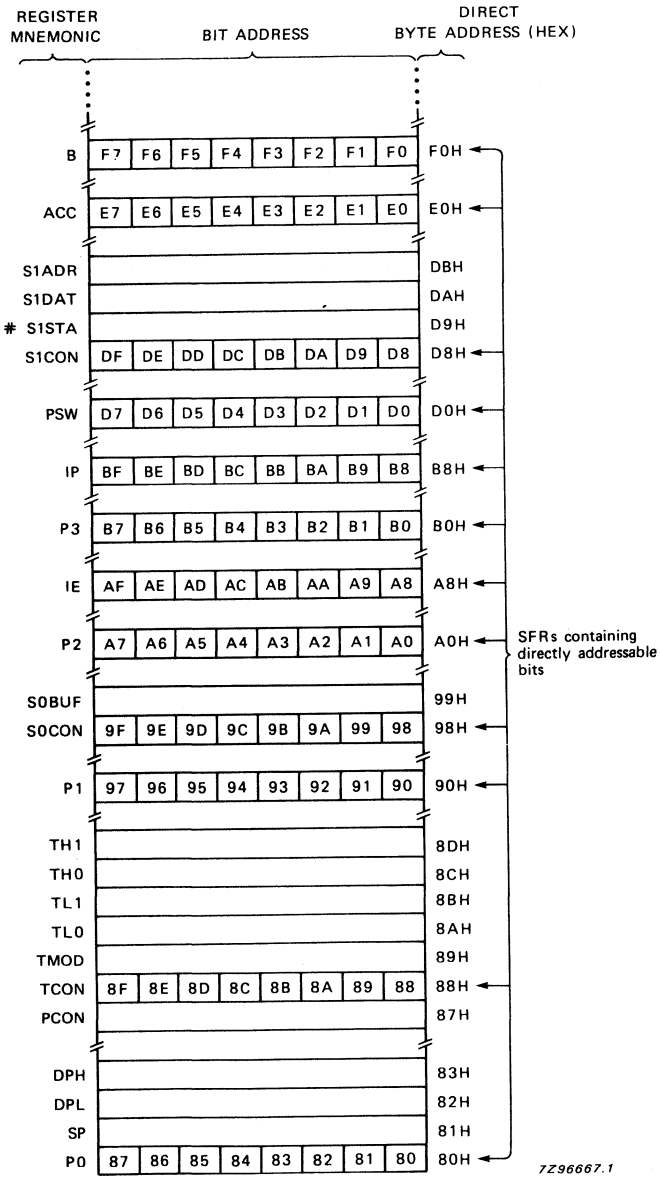


Fig. 4 Memory map.



S1STA is a read-only register.

Fig. 5 Special function registers memory map.

FUNCTIONAL DESCRIPTION (continued)

The internal data RAM contains four register banks (each with eight registers), 128 addressable bits, a scratchpad area and the stack. The stack depth is limited by the available internal data RAM and its location is determined by the 8-bit stack pointer. All registers except the program counter and the four 8-register banks reside in the special function register address space. These memory mapped registers include arithmetic registers, pointers, I/O ports, interrupt system registers, timers and serial port registers. There are 128 addressable bit locations in the SFR address space.

The PCB83C652 contains 256 bytes of internal data RAM and 25 special function registers. It provides a non-paged program memory address space to accommodate relocatable code. Conditional branches are performed relative to the program counter. The register-indirect jump permits branching relative to a 16-bit base register with an offset provided by an 8-bit index register. 16-bit jumps and calls permit branching to any location in the contiguous 64 K program memory address space.

Addressing

The PCB83C652 has five methods for addressing source operands:

- Register
- Direct
- Register-Indirect
- Immediate
- Base-Register plus Index-Register-Indirect

The first three methods can be used for addressing destination operands. Most instructions have a "destination/source" field that specifies the data type, addressing methods and operands involved. For operations other than MOVs, the destination operand is also a source operand.

Access to memory addressing is as follows:

- Registers in one of the four 8-register banks through Register, Direct, or Register-Indirect.
- 256 bytes of internal data RAM through Direct or Register-Indirect. Bytes 0-127 may be addressed directly/indirectly. Bytes 128-255 share their address locations with the SFR registers and so may only be addressed indirectly as data RAM.
- Special function registers through Direct at address locations 128-255.
- External data memory through Register-Indirect.
- Program memory look-up tables through Base-Register plus Index-Register-Indirect.

The PCB83C652 is classified as an 8-bit device since the internal ROM, RAM, Special Function Registers (SFR), Arithmetic Logic Unit (ALU) and external data bus are each 8-bits wide. It performs operations on bit, nibble, byte and double-byte data types.

Facilities are available for byte transfer, logic and integer arithmetic operations. Data transfer, logic and conditional branch operations can be performed directly on Boolean variables to provide excellent bit handling.

Instruction set

The PCB83C652 uses the powerful instruction set of the PCB80C51. Additional special function registers are incorporated to control the on-chip peripherals. The instruction set consists of 49 single-byte, 45 two-byte and 17 three-byte instructions. When using a 12 MHz oscillator, 64 instructions execute in 1 μs and 45 instructions execute in 2 μs. Multiply and divide instructions execute in 4 μs.

FUNCTIONAL DESCRIPTION (continued)

I/O facilities

The PCB83C652 has four 8-bit ports. Ports 0-3 are the same as in the 80C51, with the exception of the additional functions of port 1. Port lines P1.7 and P1.6 may be selected as the SDA and SCL lines of serial port SIO1 (I^2C). Because the I^2C bus may be active while the device is disconnected from V_{DD}, these pins are provided with open drain drivers.

N.B. Therefore pins P1.7 and P1.6 do not have pull-up devices when used as ports.

Ports 0, 1, 2 and 3 perform the following alternative functions:

- Port 0: provides the multiplexed low-order address and data bus used for expanding the PCB83C652 with standard memories and peripherals.
- Port 1: Port 1 is partly used for the I^2C bus functions;
  - SCL and SDA for the I^2C interface, P1.6 and P1.7 respectively.

Bits whose alternate function is not used may be used as normal bidirectional I/O pins.

- Port 2: provides the high-order address bus when expanding the PCB83C652 with external program memory and/or external data memory.
- Port 3: pins can be configured individually to provide:
  - external interrupt request inputs
  - counter inputs
  - serial port receiver input and transmitter output
  - control signals to READ and WRITE external data memory

The generation or use of a Port 3 pin as an alternative function is carried out automatically by the PCB83C652 provided the associated Special Function Register bit is set high.

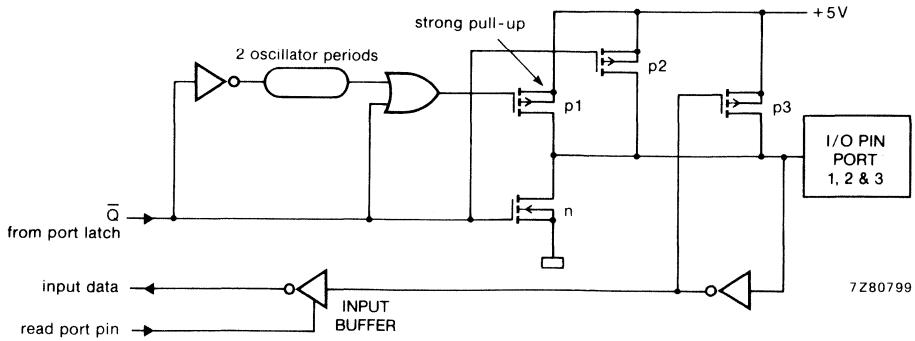


Fig. 6 I/O buffers in the PCB83C652 (Ports 2, 3, and P1.0 to P1.5).

Timer/event counters

The PCB83C652 contains two 16-bit timer/event counters: Timer 0 and Timer 1. Timer 0 and Timer 1 may be programmed to carry out the following functions:

- Measure time intervals and pulse durations
- Count events
- Generate interrupt requests.

Timer 0 and Timer 1 can be programmed independently to operate in three modes:

- Mode 0: 8-bit timer or 8-bit counter each with divide by 32 prescaler
- Mode 1: 16-bit time-interval or event counter
- Mode 2: 8-bit time-interval or event counter with automatic reload upon overflow.

Timer 0 can be programmed to operate in an additional mode as follows:

- Mode 3: one 8-bit time-interval or event counter and one 8-bit time-interval counter.

When Timer 0 is in Mode 3, Timer 1 can be programmed to operate in Modes 0, 1 or 2 but cannot set an interrupt request flag or generate an interrupt. However the overflow from Timer 1 can be used to pulse the serial port transmission-rate generator.

The frequency handling range of these counters with a 12 MHz crystal is as follows:

- In the timer function, the timer is incremented at a frequency of 1 MHz – a division by 12 of the oscillator frequency
- 0 Hz to an upper limit of 0,5 MHz when programmed for external inputs.

Both internal and external inputs can be gated to the counter by a second external source for directly measuring pulse durations.

The counters are started and stopped under software control. Each one sets its interrupt request flag when it overflows from all logic 1s to all logic 0s (or automatic reload value), with the exception of mode 3 as previously described.

Serial I/O (see Fig. 7)

The PCB83C652 is equipped with two independent serial ports. SIO0 is the full duplex UART port and is identical to the serial port of the PCB80C51.

Serial port SIO1 supports the I^2C-bus, the function of which is controlled by the S1CON register. S1STA is the status register whose contents may also be used as a vector to various service routines. S1DAT is the data shift register and S1ADR the slave address register. The least significant bit of S1ADR enables/disables general call address recognition.

FUNCTIONAL DESCRIPTION (continued)

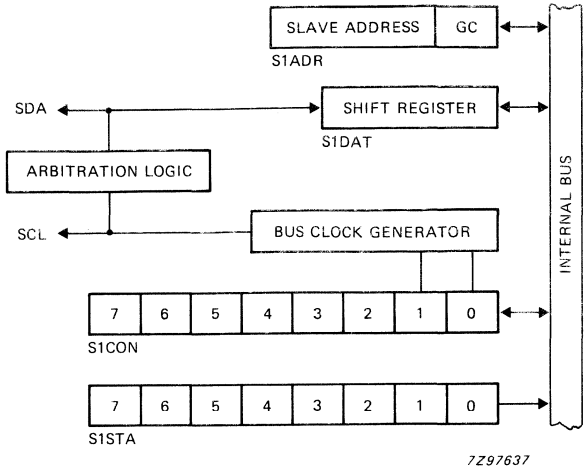


Fig. 7 Block diagram of I^2C serial I/O.

The I^2C serial I/O has complete autonomy in byte handling and operates in 4 modes:

1. Master transmitter
2. Master receiver
3. Slave transmitter
4. Slave receiver

Slave address recognition is performed by on-chip hardware.

The I^2C-bus consists of two lines: a data line (SDA) and a clock line (SCL). These lines also function as the I/O port lines on P1.7 and P1.6. The system is unique because data transport, clock generation, address recognition and bus control arbitration are all controlled by hardware.

Serial control register S1CON

	7	6	5	4	3	2	1	0
S1CON(D8H)	X	ENS1	STA	STO	SI	AA	CR1	CR0

Bits CR1 and CR0 determine the clock frequency that is generated in the master mode of operation. Table 1 displays the clock rate when using a 12 MHz crystal.

Table 1 Clock rate when using a 12 MHz crystal

CR1 / CR0		bit frequency	f_{osc} divided by
0	0	12,5 kHz	960
0	1	100 kHz	120
1	0	200 kHz	60 ($f_{osc} < 6$ MHz meeting I^2C)
1	1	62,5–0,5 kHz	96 x (256–reload value Timer 1) (reload value range: 0-254 in mode 2)

AA

Assert acknowledge bit. When this bit is set, an acknowledge is returned after any one of the following conditions:

- Own slave address is received
- General call address is received (S1ADR.0 = logic 1)
- A data byte is received, while the device is programmed to be a master receiver
- A data byte is received, while the device is a selected slave receiver.

When this bit is reset, no acknowledge is returned. Consequently, no interrupt is requested when the own address or general call address is received.

SI

SIO1 interrupt flag. This flag is set, and an interrupt request is generated, after any of the following events occur:

- A START condition is generated in MST mode
- The own slave address has been received during AA = logic 1
- The general call address has been received while S1ADR.0 and AA = logic 1
- A data byte has been received or transmitted in MST mode (even if arbitration is lost)
- A data byte has been received or transmitted as selected slave
- A STOP or START condition is received as selected slave receiver or transmitter.

STO

STOP flag. When in master mode,and this bit is set a STOP condition is generated. A STOP condition detected on the I^2C-bus clears this bit. This bit may also be set in slave mode in order to recover from an error condition. Then no STOP condition is generated to the I^2C-bus, but the hardware releases the SDA and SCL lines and switches to the not selected slave receiver mode. The STOP flag is cleared by the hardware.

STA

START flag. When this bit is set, the hardware checks the I^2C-bus and generates a START condition if the bus is free. If the device is already programmed as either master/transmitter or master/receiver, it will generate a repeated START condition.

ENS1

0 = Serial I/O Disabled and reset.Output ports P1.6 and P1.7 function with open drain

1 = Serial I/O Enabled. Output ports P1.6 and P1.7 must be set to logic 1.

FUNCTIONAL DESCRIPTION (continued)

Serial status register S1STA (S1STA is a read-only register)

	7	6	5	4	3	2	1	0
S1STA(D9H)	SC4	SC3	SC2	SC1	SC0	0	0	0

S1STA.3 - S1STA.7 hold a status code. S1STA.0 - S1STA.2 are held LOW. The contents of the status register may be used as a vector to a service routine. This optimizes the response time of the software and consequently that of the I^2C-bus.

Abbreviations used:

SLA : 7-bit slave address
R : Read bit
W : Write bit
ACK : Acknowledgement (acknowledge bit = logic 0)
$\overline{ACK}$: Not acknowledgement (acknowledge bit = logic 1)
DATA : 8-bit data byte to or from I^2C bus
MST : Master
SLV : Slave
TRX : Transmitter
REC : Receiver

The following is a list of the status codes:

MST/TRX mode

S1STA value

08H - A START condition has been transmitted
10H - A repeated START condition has been transmitted
18H - SLA and W have been transmitted, ACK has been received
20H - SLA and W have been transmitted, $\overline{ACK}$ received
28H - DATA of S1DAT has been transmitted, ACK received
30H - DATA of S1DAT has been transmitted, $\overline{ACK}$ received
38H - Arbitration lost in SLA, R/W or DATA

MST/REC mode

S1STA value

38H - Arbitration lost while returning $\overline{ACK}$
40H - SLA and R have been transmitted, ACK received
48H - SLA and R have been transmitted, $\overline{ACK}$ received
50H - DATA has been received, ACK returned
58H - DATA has been received, $\overline{ACK}$ returned

SLV/REC mode

S1STA value

- 60H - Own SLA and W have been received, ACK returned
- 68H - Arbitration lost in SLA, R/W as MST. Own SLA and W have been received, ACK returned
- 70H - General CALL has been received, ACK returned
- 78H - Arbitration lost in SLA, R/W as MST. General call has been received
- 80H - Previously addressed with own SLA. DATA byte received, $\overline{\text{ACK}}$ returned
- 88H - Previously addressed with own SLA. DATA byte received, $\overline{\text{ACK}}$ returned
- 90H - Previously addressed with general call. DATA byte has been received, ACK has been returned
- 98H - Previously addressed with general call. DATA byte has been received, $\overline{\text{ACK}}$ has been returned
- A0H - A STOP condition or repeated START condition has been received while still addressed as SLV/REC or SLV/TRX.

SLV/TRX mode

S1STA value

- A8H - Own SLA and R have been received, ACK returned
- B0H - Arbitration lost in SLA, R/W as MST. Own SLA and R have been received, ACK returned
- B8H - DATA byte has been transmitted, $\overline{\text{ACK}}$ received
- C0H - DATA byte has been transmitted, $\overline{\text{ACK}}$ received
- C8H - Last DATA byte has been transmitted (AA = logic 0), ACK received.

Miscellaneous

S1STA value

- 00H - Bus error during MST mode or selected SLV mode, due to an erroneous START or STOP condition

The data shift register S1DAT

S1DAT(DAH)	7	6	5	4	3	2	1	0

This register contains the serial data to be transmitted or data which has just been received. Bit 7 is transmitted or received first; i.e. data is shifted from right to left.

Address register S1ADR

	slave address							GC
S1ADR (DBH)	7	6	5	4	3	2	1	0

S1ADR.0, GC : 0 = general call address is not recognized
1 = general call address is recognized

S1ADR.7-1 : own slave address

This 8-bit register may be loaded with the 7-bit slave address to which the controller will respond when programmed as a slave receiver/transmitter. The LSB (GC) is used to determine whether the general call address is recognized.

FUNCTIONAL DESCRIPTION (continued)

Idle and Power-down operation (see Fig. 8)

Idle mode operation permits the interrupt, serial ports and timer blocks to continue to function while the CPU is halted.

The following functions remain active during Idle mode. These functions may generate an interrupt or reset and thus end the Idle mode:

Timer 0, Timer 1
SIO0, SIO1
External interrupt

The Power-down operation freezes the oscillator. The Power-down mode can only be activated by setting the PD bit in the PCON register.

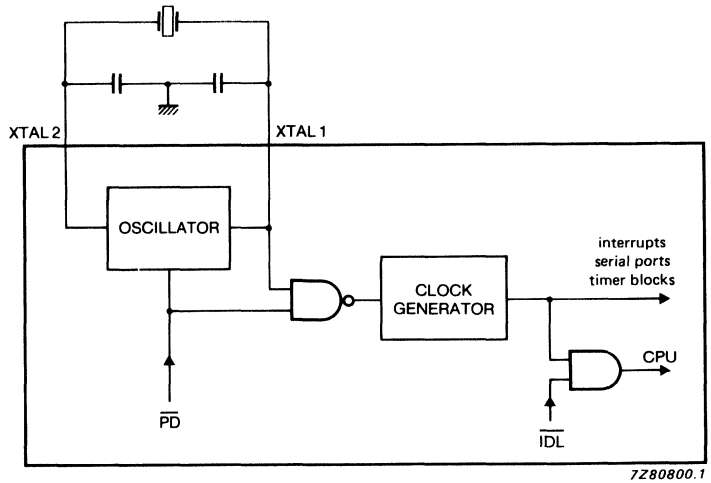


Fig. 8 Internal Idle and Power-down clock configuration.

Power control register

These special modes are activated by software via the Special Function Register PCON. Its hardware address is 87H. PCON is not bit addressable.

	7	6	5	4	3	2	1	0
PCON(87H)	SMOD	–	–	–	GF1	GF0	PD	IDL

Bit	Symbol	Function
PCON.7	SMOD	Double Baud rate bit. When set to logic 1 the baud rate is doubled when the serial port SIO0 is being used in modes 1, 2 or 3
PCON.6	–	(reserved)
PCON.5	–	(reserved)
PCON.4	–	(reserved)
PCON.3	GF1	General-purpose flag bit
PCON.2	GF0	General-purpose flag bit
PCON.1	PD	Power-down bit. Setting this bit activates Power-down mode
PCON.0	IDL	Idle mode bit. Setting this bit activates the Idle mode.

If logic 1s are written to PD and IDL at the same time, PD takes precedence. The reset value of PCON is 0XXX0000.

Idle mode

The instruction that sets PCON.0 is the last instruction executed in the normal operating mode before Idle mode is activated. Once in the Idle mode, the CPU status is preserved in its entirety: the Stack Pointer, Program Counter, Program Status Word, Accumulator, RAM and all other registers maintain their data during Idle mode. The status of the external pins during Idle mode is shown in Table 2.

There are two ways to terminate the Idle mode:

Activation of any enabled interrupt will cause PCON.0 to be cleared by hardware terminating Idle mode. The interrupt is serviced, and following return from interrupt instruction RETI, the next instruction to be executed will be the one which follows the instruction that wrote a logic 1 to PCON.0.

The flag bits GF0 and GF1 may be used to determine whether the interrupt was received during normal execution or during the Idle mode. For example, the instruction that writes to PCON.0 can also set or clear one or both flag bits. When Idle mode is terminated by an interrupt, the service routine can examine the status of the flags bits.

The second way of terminating the Idle mode is with an external hardware reset. Since the oscillator is still running, the hardware reset is required to be active for two machine cycles (24 oscillator periods) to complete the reset operation.

Power-down mode

The instruction that sets PCON.1 is the last executed prior to going into the Power-down mode. Once in Power-down mode, the oscillator is stopped. Only the contents of the on-chip RAM are preserved. The Special Function Registers are not saved. A hardware reset is the only way of exiting the Power-down mode.

In the Power-down mode, V_{DD} may be reduced to minimize circuit power consumption. The voltage must not be reduced until the Power-down mode is entered, but must be restored before the hardware reset is applied which will free the oscillator. Reset should not be released until the oscillator has restarted and stabilized.

The status of the external pins during Power-down mode is shown in Table 2. If the Power-down mode is activated while in external program memory, the port data that is held in the Special Function Register P2 is restored to port 2. If the data is a logic 1, the port pin is held HIGH during the Power-down mode by the strong pull-up transistor p1 (see Fig. 6).

FUNCTIONAL DESCRIPTION (continued)

Table 2 Status of the external pins during Idle and Power-down modes.

mode	memory	ALE	$\overline{PSEN}$	Port 0	Port 1	Port 2	Port 3
Idle	internal	1	1	port data	port data	port data	port data
Idle	external	1	1	floating	port data	address	port data
Power-down	internal	0	0	port data	port data	port data	port data
Power-down	external	0	0	floating	port data	port data	port data

Note: Ports 1.7 and 1.6 if selected, function as SDA and SCL respectively in the Idle mode.

Interrupt system (see Fig. 9)

External events and the real-time-driven on-chip peripherals require service by the CPU asynchronous to the execution of any particular section of code. To tie the asynchronous activities of these functions to normal program execution a multiple-source, two-priority-level, nested interrupt system is provided. Interrupt response latency is from 3 μs to 8 μs when using a 12 MHz crystal. The PCB83C652 acknowledges interrupt requests from six sources as follows:

- $\overline{INT0}$ and $\overline{INT1}$: two external interrupts
- Timer 0 and Timer 1: two internal counters
- I^2C serial I/O interrupt
- UART serial I/O port interrupt

Each interrupt vectors to a separate location in program memory for its service program. Each source can be individually enabled or disabled by a corresponding bit in the IE register, moreover each interrupt may be programmed to a high or low priority level using a corresponding bit in the IP register. Also all enabled sources can be globally disabled or enabled. Both external interrupts can be programmed to be level-activated or transition-activated; an active LOW level allows "wire-ORing" of several interrupt sources to the input pin.

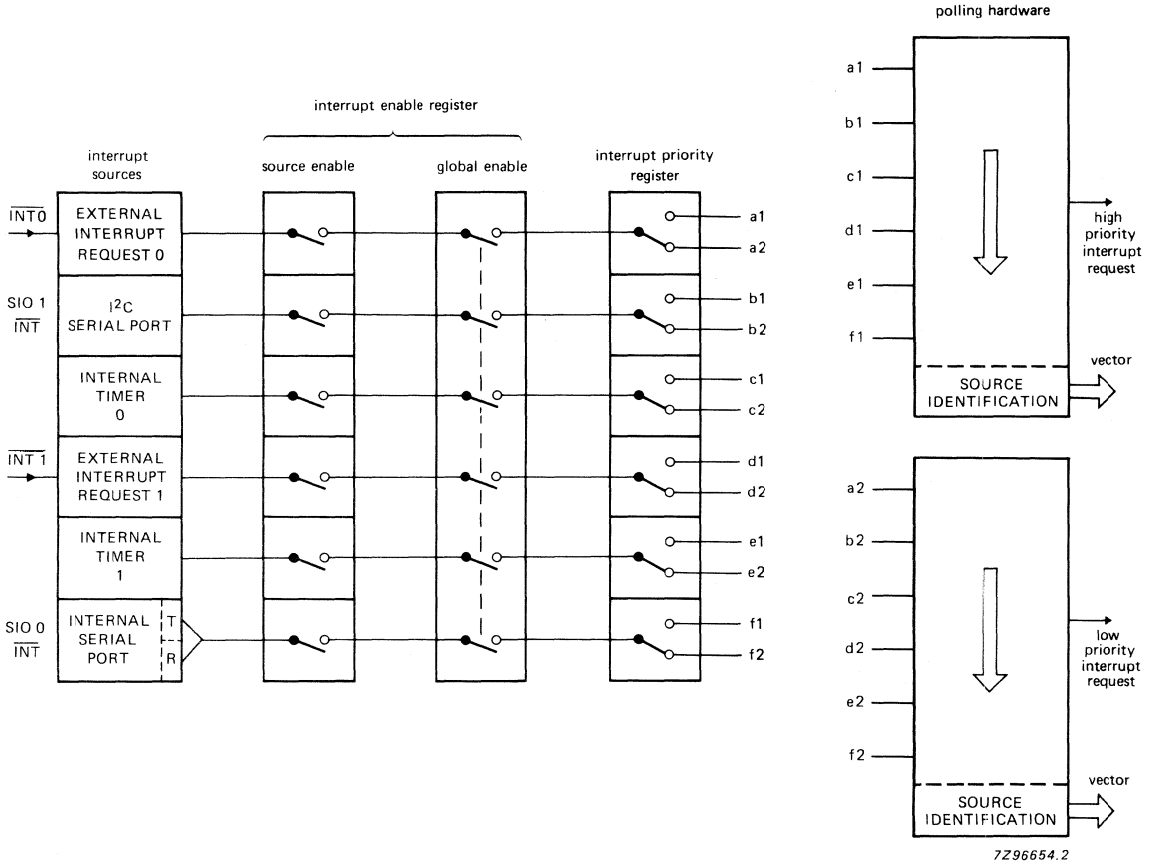


Fig. 9 Interrupt system.

FUNCTIONAL DESCRIPTION (continued)

Interrupt enable register

	7	6	5	4	3	2	1	0
IE(A8H)	EA	–	ES1	ES0	ET1	EX1	ET0	EX0

Bit	Symbol	Function
IE.7	EA	General enable/disable control 0 = No interrupt is enabled 1 = Any individually enabled interrupt will be accepted
IE.6	–	Unused
IE.5	ES1	Enable SIO1 (I^2C) interrupt
IE.4	ES0	Enable SIO0 (UART) interrupt
IE.3	ET1	Enable Timer 1 interrupt
IE.2	EX1	Enable External 1 interrupt
IE.1	ET0	Enable Timer 0 interrupt
IE.0	EX0	Enable External 0 interrupt
		where "0" = interrupt disabled and "1" = interrupt enabled

Interrupt priority register

	7	6	5	4	3	2	1	0
IP(B8H)	–	–	PS1	PS0	PT1	PX1	PT0	PX0

Bit	Symbol	Function
IP.7	–	Unused
IP.6	–	Unused
IP.5	PS1	SIO1 (I^2C) interrupt priority level
IP.4	PS0	SIO0 (UART) interrupt priority level
IP.3	PT1	Timer 1 interrupt priority level
IP.2	PX1	External interrupt 1 priority level
IP.1	PT0	Timer 0 interrupt priority level
IP.0	PX0	External interrupt 0 priority level

Interrupt priority levels are as follows: "0" – low priority
"1" – high priority

Table 3 shows the interrupt vectors. The vector indicates the ROM location where the appropriate interrupt service routine starts.

Table 3 Interrupt vectors

Source		Vector
External 0	X0	0003H
Timer 0 overflow	T0	000BH
External 1	X1	0013H
Timer 1 overflow	T1	001BH
Serial I/O 0 (UART)	S0	0023H
Serial I/O 1 (I^2C)	S1	002BH

Interrupt priority

Each interrupt source can be either high priority or low priority. If both priorities are requested simultaneously, the processor will branch to the high priority vector. If there are simultaneous requests from sources of the same priority, then interrupts will be serviced in the following order:

X0, S1, T0, X1, T1, S0

An low priority interrupt routine can only be interrupted by high priority interrupt. A high priority interrupt routine can not be interrupted.

Oscillator circuitry

The oscillator circuitry of the PCB83C652 is a single-stage inverting amplifier in a Pierce oscillator configuration. The circuitry between XTAL 1 and XTAL 2 is basically an inverter biased to the transfer point. Either a crystal or ceramic resonator can be used as the feedback element to complete the oscillator circuitry. Both are operated in parallel resonance. XTAL 1 is the high gain amplifier input, and XTAL 2 is the output (see Fig. 10). To drive the PCB83C652 externally, XTAL 1 is driven from an external source and XTAL 2 left open-circuit (see Fig. 11).

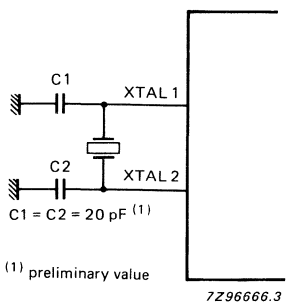


Fig. 10 PCB83C652 oscillator circuit.

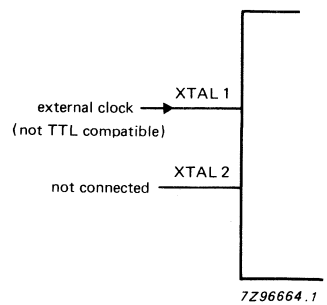


Fig. 11 Driving the PCB83C652 from an external source.

FUNCTIONAL DESCRIPTION (continued)

Reset circuitry (see Fig. 12)

The reset circuitry for the PCB83C652 is connected to the reset pin RST. A Schmitt trigger is used at the input for noise rejection. The output of the Schmitt trigger is sampled by the reset circuitry every machine cycle.

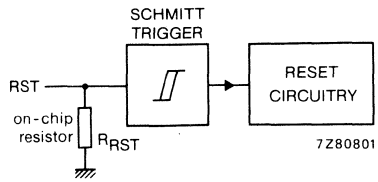


Fig. 12 On chip reset configuration.

A reset is accomplished by holding the RST pin HIGH for at least two machine cycles (24 oscillator periods). The CPU responds by executing an internal reset. During reset ALE and $\overline{PSEN}$ output a HIGH level. In order to perform a correct reset, this level must not be affected by external elements.

The internal reset is executed during the second cycle in which RST is HIGH and is repeated every cycle until RST goes LOW. It leaves the internal registers as follows:

Register	Content
ACC	0000 0000
B	0000 0000
DPL	0000 0000
DPH	0000 0000
IE	0x00 0000
IP	xx00 0000
PCH	0000 0000
PCL	0000 0000
PCON	0xxx 0000
PSW	0000 0000
P0 - P3	1111 1111
S0BUF	xxxx xxxx
S0CON	0000 0000
S1ADR	0000 0000
S1CON	x000 0000
S1DAT	0000 0000
S1STA	1111 1000
SP	0000 0111
TCON	0000 0000
TH0, TH1	0000 0000
TL0, TL1	0000 0000
TMOD	0000 0000

The internal RAM is not affected by reset. When V_{DD} is turned on, the RAM content is indeterminate.

Power-on reset (see Fig. 13)

When V_{DD} is turned on an automatic reset can be obtained by connecting the RST pin to V_{DD} via a 2,2 μF capacitor. When the power is switched on, the voltage on the RST pin is equal to V_{DD} minus the capacitor voltage, and decreases from V_{DD} as the capacitor charges through the internal resistor (R_{RST}) to ground. The larger the capacitor, the more slowly V_{RST} decreases. V_{RST} must remain above the lower threshold of the Schmitt trigger long enough to effect a complete reset. The time required is the oscillator start-up time, plus 2 machine cycles.

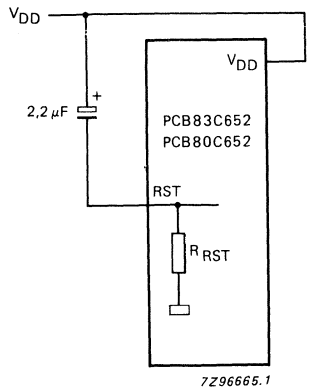


Fig. 13 Power-on reset.

INSTRUCTION SET

Table 4 Instruction set description

mnemonic		description	bytes/ cycles		opcode (hex.)
Arithmetic operations					
ADD	A,Rr	Add register to A	1	1	2*
ADD	A,direct	Add direct byte to A	2	1	25
ADD	A,@Ri	Add indirect RAM to A	1	1	26, 27
ADD	A,#data	Add immediate data to A	2	1	24
ADDC	A,Rr	Add register to A with carry flag	1	1	3*
ADDC	A,direct	Add direct byte to A with carry flag	2	1	35
ADDC	A,@Ri	Add indirect RAM to A with carry flag	1	1	36, 37
ADDC	A,#data	Add immediate data to A with carry flag	2	1	34
SUBB	A,Rr	Subtract register from A with borrow	1	1	9*
SUBB	A,direct	Subtract direct byte from A with borrow	2	1	95
SUBB	A,@Ri	Subtract indirect RAM from A with borrow	1	1	96, 97
SUBB	A,#data	Subtract immediate data from A with borrow	2	1	94
INC	A	Increment A	1	1	04
INC	Rr	Increment register	1	1	0*
INC	direct	Increment direct byte	2	1	05
INC	@Ri	Increment indirect RAM	1	1	06, 07
DEC	A	Decrement A	1	1	14
DEC	Rr	Decrement register	1	1	1*
DEC	direct	Decrement direct byte	2	1	15
DEC	@Ri	Decrement indirect RAM	1	1	16, 17
INC	DPTR	Increment data pointer	1	2	A3
MUL	AB	Multiply A & B	1	4	A4
DIV	AB	Divide A by B	1	4	84
DA	A	Decimal adjust A	1	1	D4

mnemonic		description	bytes/ cycles		opcode (hex.)
Logic operations					
ANL	A,Rr	AND register to A	1	1	5*
ANL	A,direct	AND direct byte to A	2	1	55
ANL	A,@Ri	AND indirect RAM to A	1	1	56, 57
ANL	A,#data	AND immediate data to A	2	1	54
ANL	direct,A	AND A to direct byte	2	1	52
ANL	direct,#data	AND immediate data to direct byte	3	2	53
ORL	A,Rr	OR register to A	1	1	4*
ORL	A,direct	OR direct byte to A	2	1	45
ORL	A,@Ri	OR indirect RAM to A	1	1	46, 47
ORL	A,#data	OR immediate data to A	2	1	44
ORL	direct,A	OR A to direct byte	2	1	42
ORL	direct,#data	OR immediate data to direct byte	3	2	43
XRL	A,Rr	Exclusive-OR register to A	1	1	6*
XRL	A,direct	Exclusive-OR direct byte to A	2	1	65
XRL	A,@Ri	Exclusive-OR indirect RAM to A	1	1	66, 67
XRL	A,#data	Exclusive-OR immediate data to A	2	1	64
XRL	direct,A	Exclusive-OR A to direct byte	2	1	62
XRL	direct,#data	Exclusive-OR immediate data to direct byte	3	2	63
CLR	A	Clear A	1	1	E4
CPL	A	Complement A	1	1	F4
RL	A	Rotate A left	1	1	23
RLC	A	Rotate A left through the carry flag	1	1	33
RR	A	Rotate A right	1	1	03
RRC	A	Rotate A right through the carry flag	1	1	13
SWAP	A	Swap nibbles within A	1	1	C4

DEVELOPMENT DATA

INSTRUCTION SET (continued)

mnemonic		description	bytes/ cycles		opcode (hex.)
Data transfer					
MOV	A,Rr	Move register to A	1	1	E*
MOV	A,direct (**)	Move direct byte to A	2	1	E5
MOV	A,@Ri	Move indirect RAM to A	1	1	E6, E7
MOV	A,#data	Move immediate data to A	2	1	74
MOV	Rr,A	Move A to register	1	1	F*
MOV	Rr,direct	Move direct byte to register	2	2	A*
MOV	Rr,#data	Move immediate data to register	2	1	7*
MOV	direct,A	Move A to direct byte	2	1	F5
MOV	direct,Rr	Move register to direct byte	2	2	8*
MOV	direct,direct	Move direct byte to direct byte	3	2	85
MOV	direct,@Ri	Move indirect RAM to direct byte	2	2	86, 87
MOV	direct,#data	Move immediate data to direct byte	3	2	75
MOV	@Ri,A	Move A to indirect RAM	1	1	F6, F7
MOV	@Ri,direct	Move direct byte to indirect RAM	2	2	A6, A7
MOV	@Ri,#data	Move immediate data to indirect RAM	2	1	76, 77
MOV	DPTR,#data 16	Load data pointer with a 16-bit constant	3	2	90
MOVC	A,@A+DPTR	Move code byte relative to DPTR to A	1	2	93
MOVC	A,@A+PC	Move code byte relative to PC to A	1	2	83
MOVX	A,@Ri	Move external RAM (8-bit address) to A	1	2	E2, E3
MOVX	A,@DPTR	Move external RAM (16-bit address) to A	1	2	E0
MOVX	@Ri,A	Move A to external RAM (8-bit address)	1	2	F2, F3
MOVX	@DPTR,A	Move A to external RAM (16-bit address)	1	2	F0
PUSH	direct	Push direct byte onto stack	2	2	C0
POP	direct	Pop direct byte from stack	2	2	D0
XCH	A,Rr	Exchange register with A	1	1	C*
XCH	A,direct	Exchange direct byte with A	2	1	C5
XCH	A,@Ri	Exchange indirect RAM with A	1	1	C6, C7
XCHD	A,@Ri	Exchange LOW-order nibble indirect RAM with A	1	1	D6, D7

** MOV A,ACC is not permitted.

mnemonic		description	bytes/ cycles		opcode (hex.)
Boolean variable manipulation					
CLR	C	Clear carry flag	1	1	C3
CLR	bit	Clear direct bit	2	1	C2
SETB	C	Set carry flag	1	1	D3
SETB	bit	Set direct bit	2	1	D2
CPL	C	Complement carry flag	1	1	B3
CPL	bit	Complement direct bit	2	1	B2
ANL	C,bit	AND direct bit to carry flag	2	2	82
ANL	C,/bit	AND complement of direct bit to carry flag	2	2	B0
ORL	C,bit	OR direct bit to carry flag	2	2	72
ORL	C,/bit	OR complement of direct bit to carry flag	2	2	A0
MOV	C,bit	Move direct bit to carry flag	2	1	A2
MOV	bit,C	Move carry flag to direct bit	2	2	92
Program and machine control					
ACALL	addr11	Absolute subroutine call	2	2	●1addr
LCALL	addr16	Long subroutine call	3	2	12
RET		Return from subroutine	1	2	22
RETI		Return from interrupt	1	2	32
AJMP	addr11	Absolute jump	2	2	▲1addr
LJMP	addr16	Long jump	3	2	02
SJMP	rel	Short jump (relative address)	2	2	80
JMP	@A+DPTR	Jump indirect relative to the DPTR	1	2	73
JZ	rel	Jump if A is zero	2	2	60
JNZ	rel	Jump if A is not zero	2	2	70
JC	rel	Jump if carry flag is set	2	2	40
JNC	rel	Jump if carry flag is not set	2	2	50
JB	bit,rel	Jump if direct bit is set	3	2	20
JNB	bit,rel	Jump if direct bit is not set	3	2	30
JBC	bit,rel	Jump if direct bit is set and clear bit	3	2	10
CJNE	A,direct,rel	Compare direct to A and jump if not equal	3	2	B5
CJNE	A,#data,rel	Compare immediate to A and jump if not equal	3	2	B4
CJNE	Rr,#data,rel	Compare immed. to reg. and jump if not equal	3	2	B*
CJNE	@Ri,#data,rel	Compare immed. to ind. and jump if not equal	3	2	B6, B7
DJNZ	Rr,rel	Decrement register and jump if not zero	2	2	D*
DJNZ	direct,rel	Decrement direct and jump if not zero	3	2	D5
NOP		No operation	1	1	00

Notes to Table 4

Data addressing modes

Rr	Working register R0-R7.
direct	128 internal RAM locations and any special function register (SFR).
@Ri	Indirect internal RAM location addressed by register R0 or R1 of the actual register bank.
#data	8-bit constant included in instruction.
#data16	16-bit constant included as bytes 2 and 3 of instruction.
bit	direct addressed bit in internal RAM or SFR.
addr16	16-bit destination address. Used by LCALL and LJMP. The branch will be anywhere within the 64 K-byte program memory address space.
addr11	11-bit destination address. Used by ACALL and AJMP. The branch will be within the same 2 K-byte page of program memory as the first byte of the following instruction.
rel	Signed (two's complement) 8-bit offset byte. Used by SJMP and all conditional jumps. Range is −128 to + 127 bytes relative to first byte of the following instruction.

Hexadecimal opcode cross-reference to Table 5

* : 8, 9, A, B, C, D, E, F.
● : 11, 31, 51, 71, 91, B1, D1, F1.
▲ : 01, 21, 41, 61, 81, A1, C1, E1.

Table 5 Instruction map

first hexadecimal chacter of opcode ↓ — second hexadecimal character of opcode →

	0	1	2	3	4	5	6 | 7	8 | 9 | A | B | C | D | E | F
0	NOP	AJMP addr11	LJMP addr16	RR A	INC A	INC dir	INC @Ri 0 | 1	INC Rr 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7
1	JBC bit,rel	ACALL addr11	LCALL addr16	RRC A	DEC A	DEC dir	DEC @Ri 0 | 1	DEC Rr 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7
2	JB bit,rel	AJMP addr11	RET	RL A	ADD A,#data	ADD A,dir	ADD A,@Ri 0 | 1	ADD A,Rr 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7
3	JNB bit,rel	ACALL addr11	RETI	RLC A	ADDC A,#data	ADDC A,dir	ADDC A,@Ri 0 | 1	ADDC A,Rr 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7
4	JC rel	AJMP addr11	ORL dir,A	ORL dir,#data	ORL A,#data	ORL A,dir	ORL A,@Ri 0 | 1	ORL A,Rr 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7
5	JNC rel	ACALL addr11	ANL dir,A	ANL dir,#data	ANL A,#data	ANL A,dir	ANL A,@Ri 0 | 1	ANL A,Rr 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7
6	JZ rel	AJMP addr11	XRL dir,A	XRL dir,#data	XRL A,#data	XRL A,dir	XRL A,@Ri 0 | 1	XRL A,Rr 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7
7	JNZ rel	ACALL addr11	ORL C,bit	JMP @A+DPTR	MOV A,#data	MOV dir,#data	MOV @Ri,#data 0 | 1	MOV Rr,#data 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7
8	SJMP rel	AJMP addr11	ANL C,bit	MOVC A,@A+PC	DIV AB	MOV dir,dir	MOV dir,@Ri 0 | 1	MOV dir,Rr 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7
9	MOV DPTR, #data	ACALL addr11	MOV bit,C	MOVC A,@A+DPTR	SUBB A,#data	SUBB A,dir	SUBB A,@Ri 0 | 1	SUBB A,Rr 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7
A	ORL C,/bit	AJMP addr11	MOV C,bit	INC DPTR	MUL AB		MOV @Ri,dir 0 | 1	MOV Rr,dir 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7
B	ANL C,/bit	ACALL addr11	CPL bit	CPL C	CJNE A, #data,rel	CJNE A,dir,rel	CJNE @Ri,#data,rel 0 | 1	CJNE Rr,#data,rel 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7
C	PUSH dir	AJMP addr11	CLR bit	CLR C	SWAP A	XCH A,dir	XCH A,@Ri 0 | 1	XCH A,Rr 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7
D	POP dir	ACALL addr11	SETB bit	SETB C	DA A	DJNZ dir,rel	XCHD A,@Ri 0 | 1	DJNZ Rr,rel 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7
E	MOVX A,@DPTR	AJMP addr11	MOVX A,@Ri 0 | 1		CLR A	MOV * A,dir	MOV A,@Ri 0 | 1	MOV A,Rr 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7
F	MOVX @DPTR,A	ACALL addr11	MOVX @Ri,A 0 | 1		CPL A	MOV dir,A	MOV @Ri,A 0 | 1	MOV Rr,A 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7

* MOV A,ACC is not a valid instruction.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Input voltage on any pin with respect to ground (V_{SS})	V_I	−0,5 to +6,5	V
Input, output current on any single pin	$\pm I_I$, I_O	max. 10	mA
Total power dissipation	P_{tot}	max. 1	W
Storage temperature range	T_{stg}	−65 to +150	°C
Operating ambient temperature range	T_{amb}	0 to +70	°C

DEVELOPMENT DATA

D.C. CHARACTERISTICS

V_{DD} = 5 V (±10%); V_{SS} = 0 V; T_{amb} = 0 to +70 °C; all voltages with respect to V_{SS} unless otherwise specified

parameter	symbol	min.	max.	unit	conditions
Supply voltage	V_{DD}	4,5	5,5	V	
Supply current					
operating (note 1)	I_{DD}	–	tbf	mA	f_{CLK} = 12 MHz
idle mode (note 2)	I_{DD}	–	tbf	mA	f_{CLK} = 12 MHz
Power-down current (note 3)	I_{PD}	–	tbf	µA	V_{DD} = 2 - 6 V
Inputs					
LOW level input voltage (except $\overline{EA}$, P1.6/SCL, P1.7/SDA	V_{IL}	−0,5	$0,2V_{DD}-0,1$	V	
LOW level input voltage ($\overline{EA}$)	V_{IL1}	−0,5	$0,2V_{DD}-0,3$	V	
LOW level input voltage (P1.6/SCL, P1.7/SDA)(note 6)	V_{IL2}	−0,5	1,5	V	
HIGH level input voltage (except XTAL 1, RST, P1.6/SCL, P1.7/SDA)	V_{IH}	$0,2V_{DD}+0,9$	$V_{DD}+0,5$	V	
HIGH level input voltage (XTAL 1, RST)	V_{IH1}	$0,7V_{DD}$	$V_{DD}+0,5$	V	
HIGH level input voltage (P1.6/SCL, P1.7/SDA)(note 6)	V_{IH2}	3,0	6	V	
Input current logic 0 (Ports 1, 2, 3; except P1.6/SCL, P1.7/SDA)	$-I_{IL}$	–	50	µA	V_I = 0,45 V
Input current logic 1 to 0 transition (Ports 1, 2, 3; except P1.6/SCL, P1.7/SDA)	$-I_{TL}$	–	650	µA	V_I = 2 V
Input leakage current (Port 0, $\overline{EA}$)	$\pm I_{LI1}$	–	10	µA	$0,45\,V < V_I < V_{DD}$
Input leakage current (P1.6/SCL, P1.7/SDA)	$\pm I_{LI2}$	–	10	µA	$0\,V < V_I < 6\,V$ $0\,V < V_{DD} < 5,5\,V$

D.C. CHARACTERISTICS (continued)

parameter	symbol	min.	max.	unit	conditions
Outputs					
LOW level output voltage (note 4) (Ports 1, 2, 3; except P1.6/SCL, P1.7/SDA)	V_{OL}	–	0,45	V	I_{OL} = 1,6 mA
LOW level output voltage (note 4) (Port 0, ALE, $\overline{PSEN}$)	V_{OL1}	–	0,45	V	I_{OL} = 3,2 mA
LOW level output voltage (P1.6/SCL, P1.7/SDA)	V_{OL2}	–	0,4	V	I_{OL} = 3,0 mA
HIGH level output voltage (Ports 1, 2, 3)	V_{OH}	2,4	–	V	$-I_{OH}$ = 60 μA; V_{DD} = 5 V ± 10%
		$0{,}75V_{DD}$	–	V	$-I_{OH}$ = 25 μA
		$0{,}9V_{DD}$	–	V	$-I_{OH}$ = 10 μA
HIGH level output voltage (note 5) (Port 0 in external Bus mode, ALE, $\overline{PSEN}$)	V_{OH1}	2,4	–	V	$-I_{OH}$ = 400 μA; V_{DD} = 5 V ± 10%
		$0{,}75V_{DD}$	–	V	$-I_{OH}$ = 150 μA
		$0{,}9V_{DD}$	–	V	$-I_{OH}$ = 40 μA
RST pull-down resistor	R_{RST}	50	150	kΩ	
I/O pin capacitance	$C_{I/O}$	–	10	pF	test freq. = 1 MHz; T_{amb} = 25 °C

Notes to the d.c. characteristics

1. The operating supply current is measured with all output pins disconnected; XTAL 1 driven with $t_r = t_f$ = 10 ns; $V_{IL} = V_{SS}$ + 0,5 V; $V_{IH} = V_{DD}$ −0,5 V; XTAL 2 not connected; $\overline{EA}$ = RST = Port 0 = P1.6 = P1.7 = V_{DD}.
2. The idle mode supply current is measured with all output pins disconnected; XTAL 1 driven with $t_r = t_f$ = 10 ns; $V_{IL} = V_{SS}$ + 0,5 V; $V_{IH} = V_{DD}$ −0,5 V; XTAL 2 not connected; $\overline{EA}$ = Port 0 = P1.6 = P1.7 = V_{DD}; RST = V_{SS}.
3. The power-down current is measured with all output pins disconnected; XTAL 2 not connected; $\overline{EA}$ = Port 0 = P1.6 = P1.7 = V_{DD}; RST = V_{SS}.
4. Capacitive loading on Port 0 and Port 2 may cause spurious noise pulses to be superimposed on the LOW level output voltage of ALE, Port 1 and Port 3. The noise is due to external bus capacitance discharging into the Port 0 and Port 2 pins when these pins make a 1-to-0 transition during Bus operations. In the most adverse condition (capacitive loading > 100 pF) the noise pulse on ALE line may exceed 0,8 V. In this event it may be required to qualify ALE with a Schmitt trigger, or use an address latch with a Schmitt trigger STROBE input.
5. Capacitive loading on Port 0 and Port 2 may cause the HIGH level output voltage on ALE and $\overline{PSEN}$ to momentarily fall below the 0,9 V_{DD} specification when the address bits are stabilizing.
6. The input threshold voltage of P1.6 and P1.7 (SIO1) meets the I^2C specification, so an input voltage below 1,5 V will be recognized as a logic 0 while an input voltage above 3,0 V will be recognized as a logic 1.

DEVELOPMENT DATA

A.C. CHARACTERISTICS

V_{DD} = 5 V ± 10%; V_{SS} = 0 V; T_{amb} = 0 to +70 °C; C_L = 100 pF (Port 0, ALE and $\overline{PSEN}$); C_L = 80 pF (all other outputs); unless otherwise specified (see waveforms Figs 16, 17 and 18)

parameter	symbol	10 MHz		12 MHz		variable clock		unit
		min.	max.	min.	max.	min.	max.	
Program memory								
ALE pulse duration	t_{LL}	160	–	127	–	$2t_{CK}-40$	–	ns
Address set-up time to ALE	t_{AL}	45	–	28	–	$t_{CK}-55$	–	ns
Address hold time after ALE	t_{LA}	65	–	48	–	$t_{CK}-35$	–	ns
Time from ALE to valid instruction input	t_{LIV}	–	300	–	233	–	$4t_{CK}-100$	ns
Time from ALE to control pulse $\overline{PSEN}$	t_{LC}	60	–	43	–	$t_{CK}-40$	–	ns
Control pulse duration $\overline{PSEN}$	t_{CC}	255	–	205	–	$3t_{CK}-45$	–	ns
Time from $\overline{PSEN}$ to valid instruction input	t_{CIV}	–	195	–	145	–	$3t_{CK}-105$	ns
Input instruction hold time after $\overline{PSEN}$	t_{CI}	0	–	0	–	0	–	ns
Input instruction float delay after $\overline{PSEN}$	t_{CIF}	–	75	–	59	–	$t_{CK}-25$	ns
Address to valid instruction input	t_{AIV}	–	395	–	312	–	$5t_{CK}-105$	ns
Address float delay after $\overline{PSEN}$	t_{AFC}	–	10	–	10	–	10	ns

A.C. CHARACTERISTICS (continued)

parameter	symbol	10 MHz		12 MHz		variable clock		unit
		min.	max.	min.	max.	min.	max.	
External data memory								
$\overline{RD}$ pulse duration	t_{RR}	500	–	400	–	$6t_{CK}-100$	–	ns
$\overline{WR}$ pulse duration	t_{WW}	500	–	400	–	$6t_{CK}-100$	–	ns
Address set-up time to ALE	t_{AL}	60	–	43	–	$t_{CK}-40$	–	ns
Address hold time after ALE	t_{LA}	65	–	48	–	$t_{CK}-35$	–	ns
$\overline{RD}$ to valid data input	t_{RD}	–	335	–	250	–	$5t_{CK}-165$	ns
Data hold time after $\overline{RD}$	t_{DR}	0	–	0	–	0	–	ns
Data float delay after $\overline{RD}$	t_{DFR}	–	130	–	97	–	$2t_{CK}-70$	ns
Time from ALE to valid data input	t_{LD}	–	650	–	517	–	$8t_{CK}-150$	ns
Address to valid data input	t_{AD}	–	735	–	585	–	$9t_{CK}-165$	ns
Time from ALE to $\overline{RD}$ or $\overline{WR}$	t_{LW}	250	350	200	300	$3t_{CK}-50$	$3t_{CK}+50$	ns
Time from address to $\overline{RD}$ or $\overline{WR}$	t_{AW}	270	–	203	–	$4t_{CK}-130$	–	ns
Time from $\overline{RD}$ or $\overline{WR}$ HIGH to ALE HIGH	t_{WHLH}	60	140	43	123	$t_{CK}-40$	$t_{CK}+40$	ns
Data valid to $\overline{WR}$ transition	t_{DWX}	40	–	23	–	$t_{CK}-60$	–	ns
Data set-up time before $\overline{WR}$	t_{DW}	550	–	433	–	$7t_{CK}-150$	–	ns
Data hold time after $\overline{WR}$	t_{WD}	50	–	33	–	$t_{CK}-50$	–	ns
Address float delay after $\overline{RD}$	t_{AFR}	–	12	–	12	–	12	ns

Where:

$1/t_{CK}$ = 3,5 to 12 MHz (see Fig. 15 and Table 6)

t_{CY} = 12 t_{CK} (see Fig. 16 and D.C. characteristics)

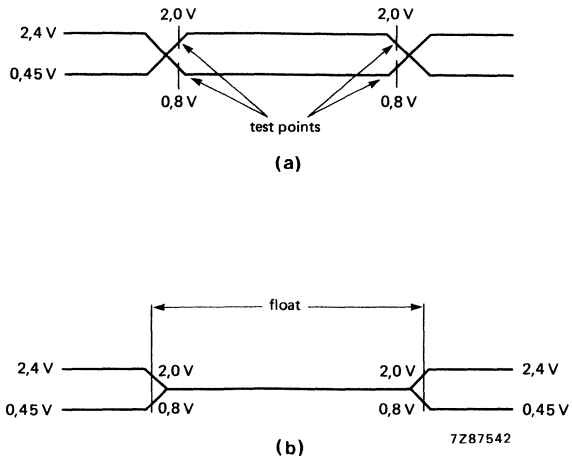


Fig. 14 A.C. testing input, output waveform (a) and float waveform (b).

A.C. testing inputs are driven at 2,4 V for a logic 1 and 0,45 V for a logic 0. Timing measurements are taken at 2,0 V for a logic 1 and 0,8 V for logic 0. The float state is defined as the point at which a Port 0 pin sinks 3,2 mA or sources 400 μA at the voltage test levels.

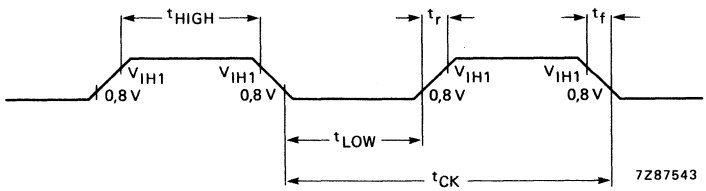


Fig. 15 External clock drive XTAL 1 (see Table 6).

Table 6 External clock drive XTAL 1 (see Fig. 15)

parameter	symbol	variable clock (f = 3,5 to 12 MHz)		unit
		min.	max.	
oscillator clock period	t_{CK}	83,3	286	ns
HIGH time	t_{HIGH}	20	$t_{CK}-t_{LOW}$	ns
LOW time	t_{LOW}	20	$t_{CK}-t_{HIGH}$	ns
rise time	t_r	–	20	ns
fall time	t_f	–	20	ns
cycle time	$t_{CY} = 12\ t_{CK}$	1	3,43	μs

A.C. CHARACTERISTICS (continued)

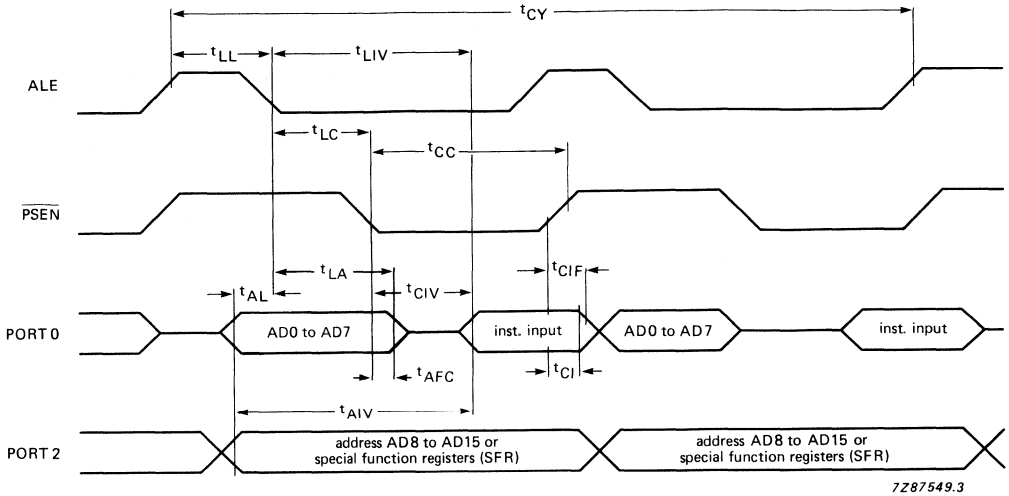


Fig. 16 Read from program memory.

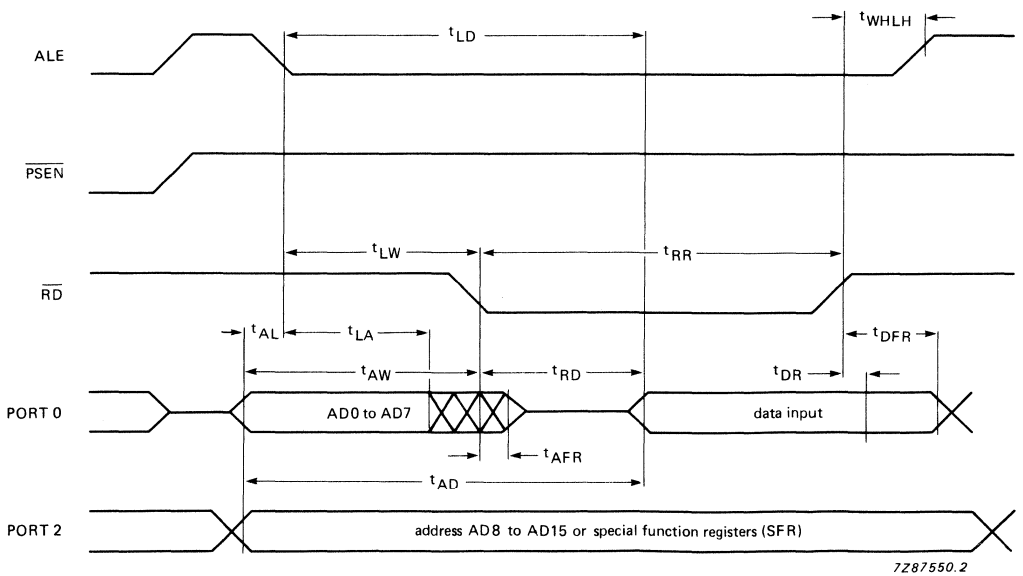


Fig. 17 Read from data memory.

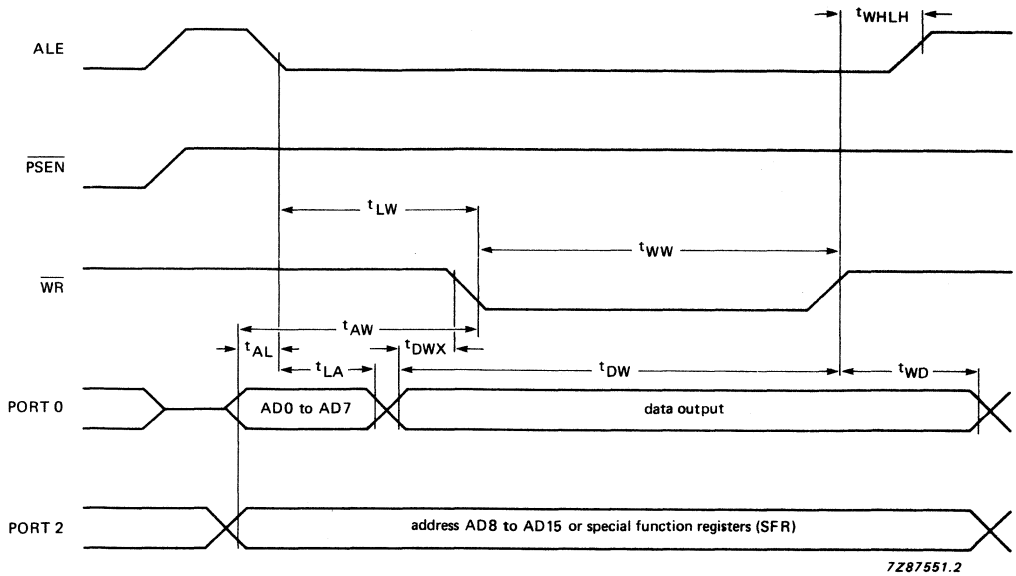


Fig. 18 Write to data memory.

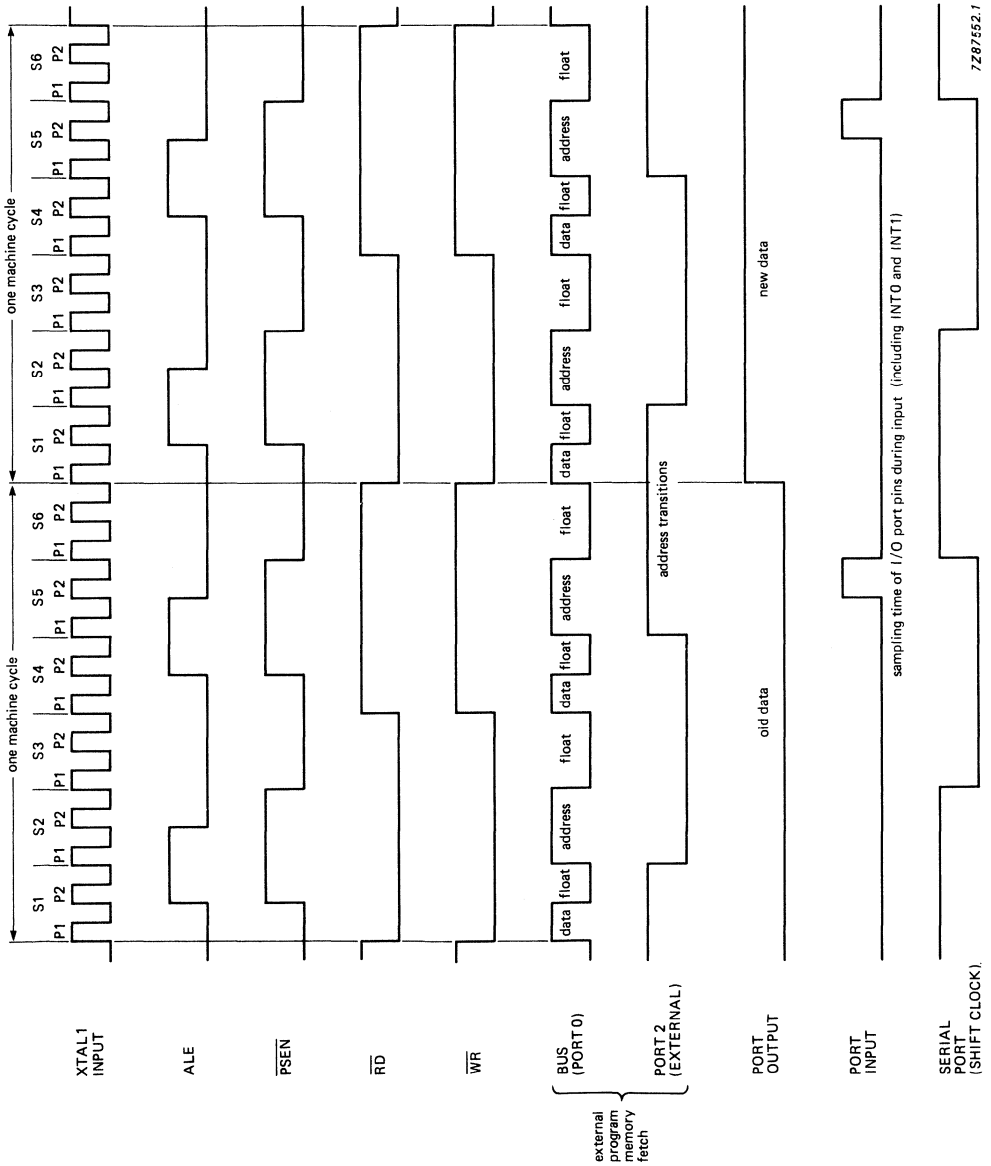


Fig. 19 Instruction cycle timing.

CMOS MICROCONTROLLER FOR TELEPHONE SETS

GENERAL DESCRIPTION

The PCD3315C is a single-chip 8-bit microcontroller fabricated in CMOS and is a member of the PCD3343 family. It has special on-chip features for application in telephone sets.

Features

- 8-bit CPU, ROM, RAM, I/O in a single 28-lead DIL or SO package
- 1536 ROM bytes
- 160 RAM bytes
- 20 quasi-bidirectional I/O port lines
- Two test inputs: one of which is also the external interrupt input (CE/$\overline{T0}$)
- Single-level vectored interrupts: external, timer/event counter
- 8-bit programmable timer/event counter
- Over 80 instructions (based on MAB8048, MAB8400, PCD3343 and PCF8500)
- All instructions 1 or 2 cycles
- Clock frequency 100 kHz to 10 MHz
- Single supply voltage from 1,8 V to 6 V
- Low standby voltage and current
- STOP and IDLE mode
- On-chip oscillator with output drive capability for peripherals
- Configuration of all I/O port lines individually selected by mask: pull-up, open drain or push-pull
- Power-on-reset circuit and low supply voltage detection
- Reset state of all ports individually selected by mask
- Operating temperature range: −25 to + 70 °C

PACKAGE OUTLINES

PCD3315CP: 28-lead DIL; plastic (SOT-117).
PCD3315CT: 28-lead mini-pack; plastic (SO-28; SOT-136A).

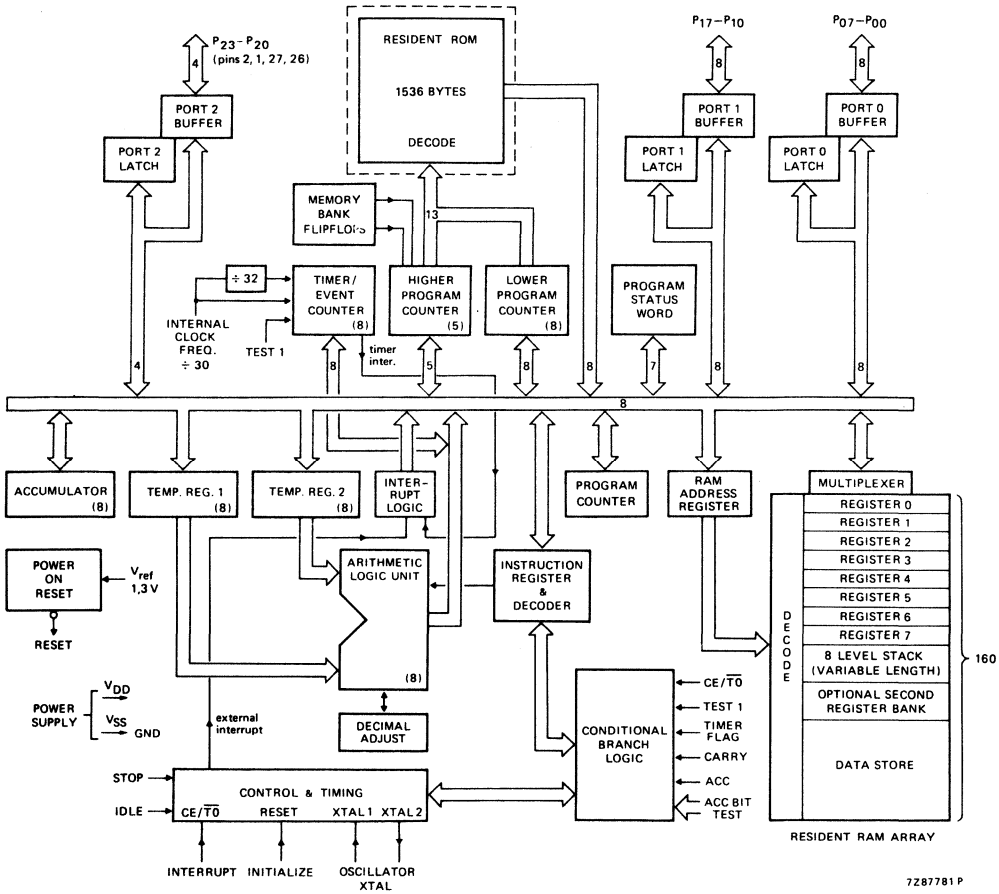
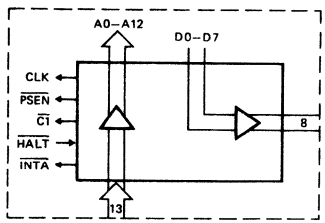
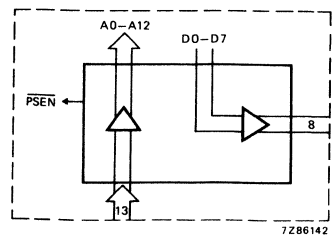


Fig. 1 Block diagram; PCD3315C.



(a)

Fig. 1a Replacement of dotted part in Fig. 1, for the PCD8500F bond-out version.



(b)

Fig. 1b Replacement of dotted part in Fig. 1, for the PCF8500B 'Piggy-back' version.

DEVELOPMENT DATA

PINNING

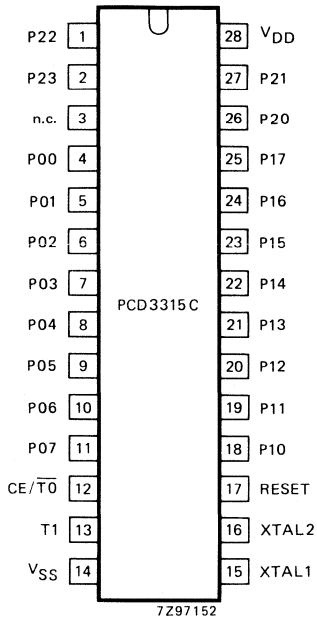


Fig. 2 Pinning diagram: PCD3315C.

PIN DESIGNATION

3	n.c.	not connected
4-11	P00-P07	**Port 0**: 8-bit quasi-bidirectional I/O port.
12	CE/$\overline{T0}$	**Interrupt/Test 0**: external interrupt input (sensitive to positive-going edge edge)/test input pin; when used as a test input directly tested by conditional branch instructions JT0 and JNT0.
13	T1	**Test 1**: test input pin, directly tested by conditional branch instructions JT1 and JNT1. T1 also functions as an input to the 8-bit timer/event counter, using the STRT CNT instruction.
14	V_{SS}	**Ground**: circuit earth potential.
15	XTAL 1	**Crystal input**: connection to timing component (crystal) which determines the frequency of the internal oscillator; also the input for an external clock source.
16	XTAL 2	connection to the other side of the timing component.
17	RESET	**Reset input**: used to initialize the processor (active HIGH), or output of power-on-reset circuit.
18-25	P10-P17	**Port 1**: 8-bit quasi-bidirectional I/O port.
26, 27, 1, 2	P20-P23	**Port 2**: 4-bit quasi-bidirectional I/O port.
28	V_{DD}	**Power supply**: 1,8 V to 6 V.

D.C. CHARACTERISTICS

V_{DD} = 2,5 to 6 V; V_{SS} = 0 V; T_{amb} = −25 to + 70 °C; all voltages with respect to V_{SS}; f = 3,58 MHz with R_S = 50 Ω; unless otherwise specified.

parameter	symbol	min.	typ.	max.	unit
Supply voltage					
operating	V_{DD}	1,8	–	6	V
STOP mode for RAM retention	V_{DD}	1,0	–	6	V
Supply current					
operating					
at V_{DD} = 3 V	I_{DD}	–	350	–	μA
IDLE mode					
at V_{DD} = 3 V	I_{DD}	–	150	–	μA
STOP mode (note 1)					
at V_{DD} = 1,8 V; T_{amb} = 25 °C	I_{DD}	–	1,2	2,5	μA
at V_{DD} = 1,8 V; T_{amb} = 55 °C	I_{DD}	–	–	5	μA
at V_{DD} = 1,8 V; T_{amb} = 70 °C	I_{DD}	–	–	10	μA
RESET I/O					
Switching level	V_{RESET}	–	1,2	–	V
Sink current					
at $V_{DD} > V_{RESET}$	I_{OL}	–	7	–	μA
Inputs					
Input voltage LOW	V_{IL}	0	–	$0{,}3V_{DD}$	V
Input voltage HIGH	V_{IH}	$0{,}7V_{DD}$	–	V_{DD}	V
Input leakage current					
at $V_{SS} < V_I < V_{DD}$	$\pm I_{IL}$	–	–	1	μA
Outputs					
Output voltage LOW					
at $V_I = V_{SS}$ or V_{DD}; $\lvert I_O \rvert < 1$ μA	V_{OL}	–	–	0,05	V
Output sink current LOW					
at V_{DD} = 3 V; V_O = 0,4 V	I_{OL}	0,6	1,5	–	mA
Pull-up output source current HIGH					
at V_{DD} = 3 V; $V_O = 0{,}9V_{DD}$	$-I_{OH}$	10	–	–	μA
at V_{DD} = 3 V; $V_O = V_{SS}$	$-I_{OH}$	–	–	200	μA
Push-pull output source current HIGH					
at V_{DD} = 3 V; $V_O = V_{DD}$−0,4 V	$-I_{OH}$	0,6	1,5	–	mA

Note 1

Crystal connected between XTAL 1 and XTAL 2; pin 2 pulled to V_{DD} via 5,6 kΩ resistor; CE and T1 at V_{SS}.

CMOS MICROCONTROLLER FOR TELEPHONE SETS

GENERAL DESCRIPTION

The PCD3343 is a single-chip 8-bit microcontroller fabricated in CMOS. It has special on-chip features for application in telephone sets.
The device is mask programmable, designed to provide telephone dialling facilities such as redial, repertory dial, emergency call, keyboard scan and control for liquid crystal display, pulse dial and/or DTMF dial via dedicated peripheral.

Features

- 8-bit CPU, ROM, RAM, I/O in a single 28-lead DIL or SO package
- 3 K ROM bytes
- 224 RAM bytes
- 20 quasi-bidirectional I/O port lines
- Two test inputs: one of which is also the external interrupt input (CE/$\overline{T0}$)
- Single-level vectored interrupts: external, timer/event counter, serial I/O
- Serial I/O which can be used in bus systems with more than one master (serial I/O data via an existing port line and clock via a dedicated line)
- 8-bit programmable timer/event counter
- Over 80 instructions (based on MAB8048, MAB8400 and PCF8500)
- All instructions 1 or 2 cycles
- Clock frequency 100 kHz to 10 MHz
- Single supply voltage from 1,8 V to 6 V
- Low standby voltage and current
- STOP and IDLE mode
- On-chip oscillator with output drive capability for peripherals (e.g. PCD3312 DTMF generator)
- Configuration of all I/O port lines individually selected by mask: pull-up, open drain or push-pull
- Power-on-reset circuit and low supply voltage detection
- Reset state of all ports individually selected by mask
- Operating temperature range: −25 to + 70 °C

PACKAGE OUTLINES

PCD3343P : 28-lead DIL; plastic (SOT-117).
PCD3343D: 28-lead DIL; ceramic (CERDIP) (SOT-135A).
PCD3343T : 28-lead mini-pack; plastic (SO-28; SOT-136A).

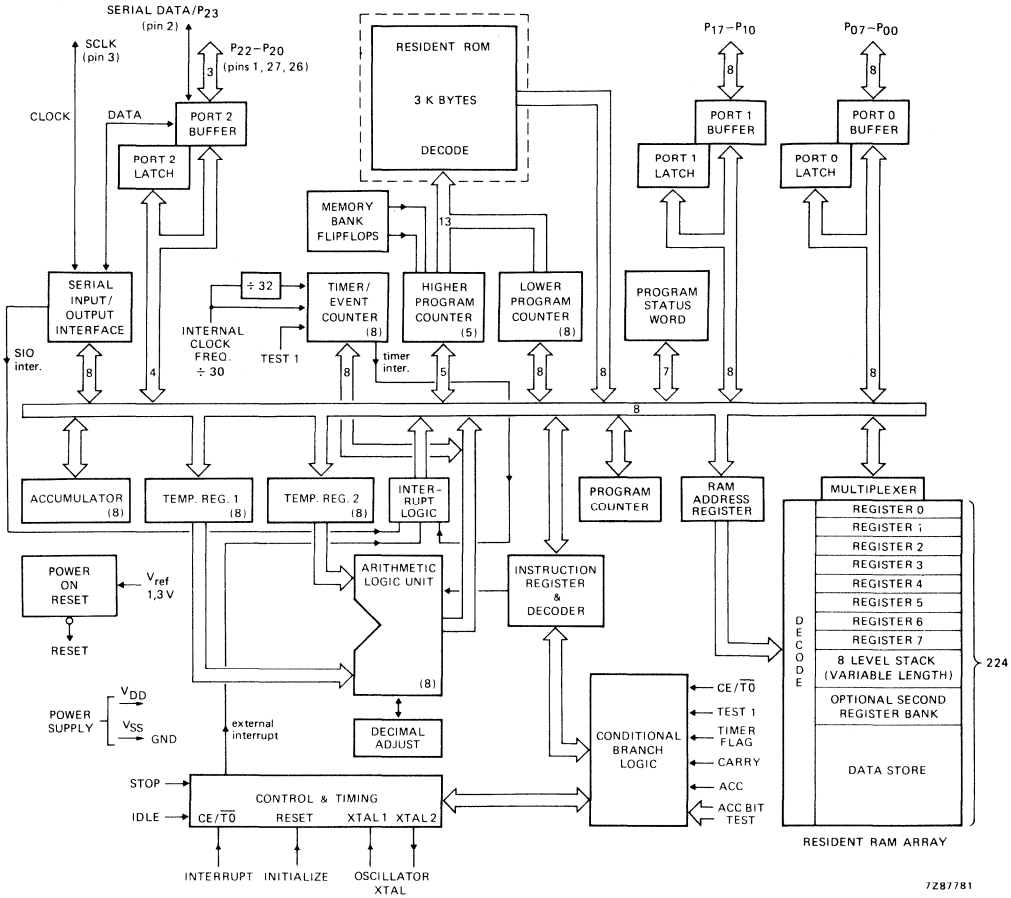
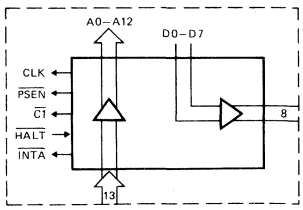
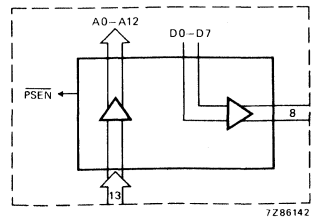


Fig. 1 Block diagram; PCD3343.



(a)

Fig. 1a Replacement of dotted part in Fig. 1, for the PCF8500F bond-out version.

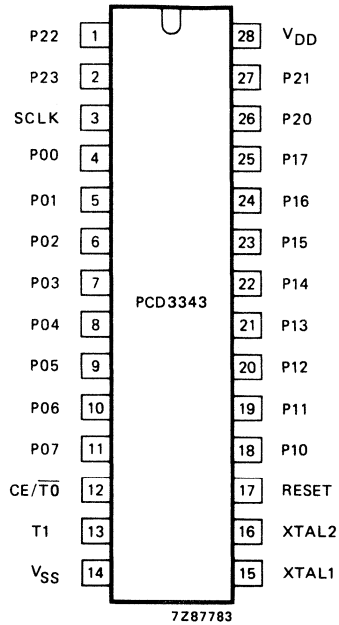


(b)

Fig. 1b Replacement of dotted part in Fig. 1, for the PCF8500B 'Piggy-back' version.

DEVELOPMENT DATA

PINNING



Note CE/$\overline{T0}$ is labelled $\overline{INT}$/T0 on the PCF8500B and has inverted polarity.

Fig. 2 Pinning diagram: PCD3343 and bottom pinning PCF8500B.

PIN DESIGNATION

3	SCLK	**Clock**: bidirectional clock for serial I/O.
4-11	P00-P07	**Port 0**: 8-bit quasi-bidirectional I/O port.
12	CE/$\overline{T0}$	**Interrupt/Test 0**: external interrupt input (sensitive to positive-going edge)/test input pin; when used as a test input directly tested by conditional branch instructions JT0 and JNT0.
13	T1	**Test 1**: test input pin, directly tested by conditional branch instructions JT1 and JNT1. T1 also functions as an input to the 8-bit timer/event counter, using the STRT CNT instruction.
14	V_{SS}	**Ground**: circuit earth potential.
15	XTAL 1	**Crystal input**: connection to timing component (crystal) which determines the frequency of the internal oscillator; also the input for an external clock source.
16	XTAL 2	connection to the other side of the timing component.
17	RESET	**Reset input**: used to initialize the processor (active HIGH), or output of power-on-reset circuit.
18-25	P10-P17	**Port 1**: 8-bit quasi-bidirectional I/O port.
26, 27, 1, 2	P20-P23	**Port 2**: 4-bit quasi-bidirectional I/O port. P23 is the serial data input/output in serial I/O mode.
28	V_{DD}	**Power supply**: 1,8 V to 6 V.

PINNING (continued)

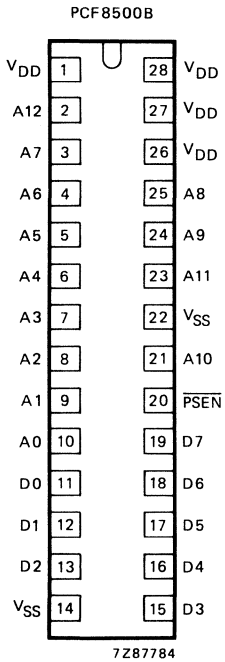


Fig. 3 Pinning diagram: PCF8500B 'Piggy-back' version top pinning; to access a 2732 or 2764 EPROM.

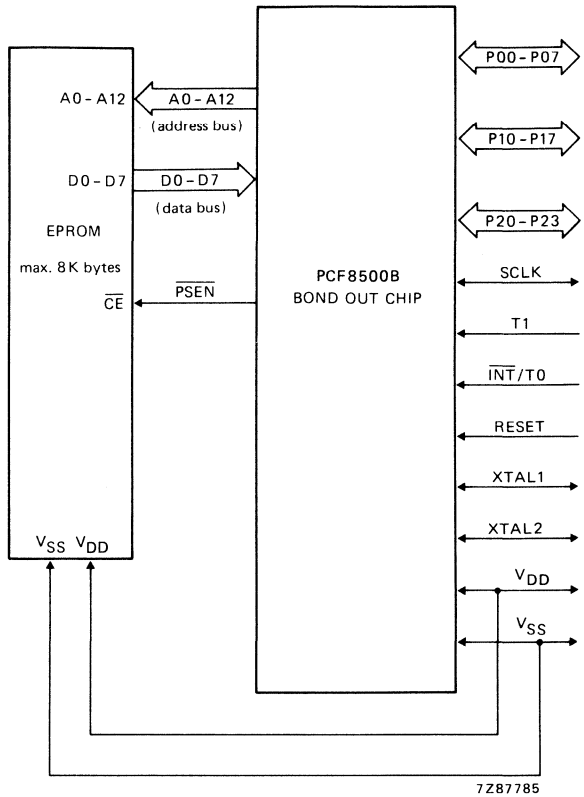


Fig. 3a Connection of EPROM to 'Piggy-back' package PCF8500B.

PIN DESIGNATION

14, 22	V_{SS}	**Ground**
1, 26-28	V_{DD}	**Power supply**
10-3, 25, 24, 21, 23, 2	A0-A12	**Address outputs**
11-13, 15-19	D0-D7	**Data**
20	$\overline{PSEN}$	**Program store enable**

Notes

1. RAM capacity of PCF8500B is 256 bytes.
2. Access time for ROMS/EPROMS to be below 7 x $1/f_{XTAL}$.
3. Pin 12 CE/$\overline{T0}$ is on the PCF8500B, inverted and labelled $\overline{INT}$/T0.

FUNCTIONAL DESCRIPTION

Bond-out version PCF8500F

The PCF8500F is a microcontroller that contains no on-board ROM, but has all address and data lines brought-out to access an external ROM or EPROM. This version has more pins than the PCD3343 with on-board ROM (see Fig. 1a). The RAM has 256 bytes. It can address 8 K bytes of ROM.

'Piggy-back' version PCF8500B

The PCF8500B is a special package that has standard pinning to the bottom which facilitates insertion as a mask-programmed device. An EPROM can be mounted on top in an additional socket. The total package height is greater than the standard DIL package. The RAM has 256 bytes and can also address 8 K bytes of program memory.

Program memory PCD3343

The program memory consists of 3072 bytes (8-bit words), in a read-only memory (ROM). Each location is directly addressable by the program counter. The memory is mask-programmed at the factory. Figure 4 shows the program memory map.

Four program memory locations are of special importance:

- Location 0; contains the first instruction to be executed after the processor is initialized (RESET),
- Location 3; contains the first byte of an external interrupt service subroutine,
- Location 5; contains the first byte of a serial I/O interrupt service subroutine,
- Location 7; contains the first byte of a timer/event counter interrupt service subroutine.

Program memory is arranged in banks of 2 K bytes, which are selected by SEL MB instructions. The program memory is further divided into location 'pages', each of 256 bytes. This latter division applies only for conditional branches. Memory bank boundaries can be crossed only by using the unconditional branch instructions after the appropriate memory bank has been selected. A CALL instruction can transfer control to a subroutine on any 'page'; RET and RETR instructions can transfer control from a subroutine back to the main program.

Data memory PCD3343

Data memory consists of 224 bytes (8-bit words), random-access data memory (RAM). All locations are indirectly addressable using RAM pointer registers; up to 16 designated locations are directly addressable. Memory also includes an 8-level program counter stack addressed by a 3-bit stack pointer. Figure 5 shows the data memory map.

Working registers

Locations 0 to 7 are designated as working registers, directly addressable by the direct register instructions. Ease of addressing, and a minimum requirement of instruction bytes to manipulate their contents, makes these locations suitable for storing frequently addressed intermediate results. This bank of registers can be selected by the SEL RB0 instruction.

Executing the select register bank instruction SEL RB1, designates locations 24 to 31 as working registers, instead of locations 0 to 7, and these are then directly addressable. This second bank of working registers may be used as an extension of the first or reserved for use during interrupt service subroutines saving the first bank for use in the main program. If the second bank is not used, locations 24 to 31 may serve as general purpose RAM.

The first locations of each bank contain the RAM pointer registers R0, R1, R0' and R1', which indirectly address all RAM locations.

All RAM locations make efficient program loop counters when used with the decrement register and test instruction DJNZ.

FUNCTIONAL DESCRIPTION (continued)

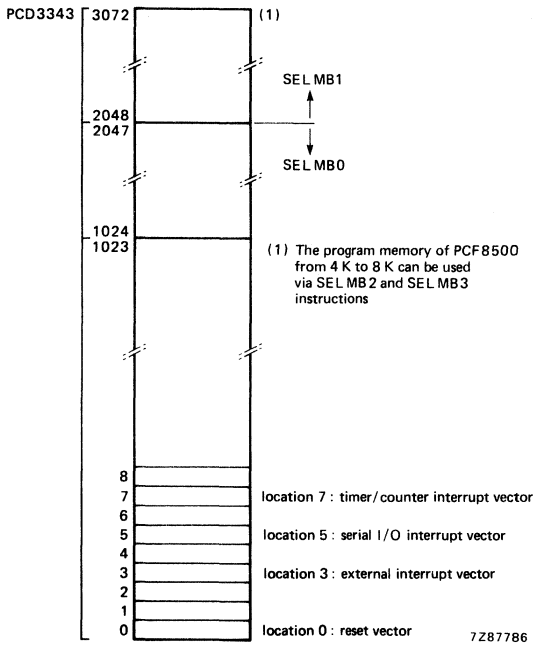


Fig. 4 Program memory map.

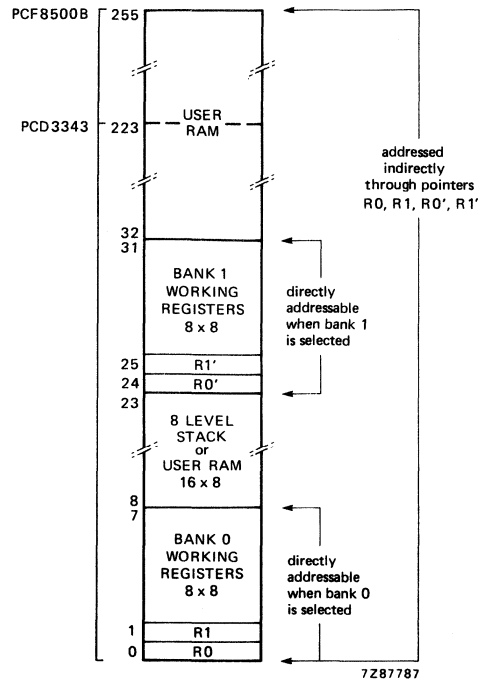


Fig. 5 Data memory map.

Program counter stack

Locations 8 to 23 may be designated as an 8-level program counter stack (2 locations per level), or as general purpose RAM. The program counter stack (Fig. 6) enables the processor to keep track of the return addresses and status generated by interrupts or CALL instructions by storing the contents of the program counter prior to servicing the subroutine. A 3-bit stack pointer determines which of the eight register pairs of the program counter stack will be loaded with next generated return address.

The stack pointer, when initialized to 000 by RESET, points to RAM locations 8 and 9. On the first subroutine CALL or interrupt, the contents of the program counter and bits 4, 6 and 7 of the program status word (PSW) are transferred to locations 8 and 9. The stack pointer increments by one and points to locations 10 and 11 ready for another CALL. Because an address may be up to 13 bits long, two bytes must be used to store each address.

At the end of a subroutine, which is signalled by a return instruction (RET or RETR), the stack pointer decrements by one and the contents of the register pair on top of the stack are transferred to the program counter. The saved PSW bits are transferred to the PSW only by the RETR instruction.

If not all 8 levels of subroutine and interrupt nesting are used, the unused portion of the stack may be used as any other indirectly addressable RAM locations. Possible locations from 32 to 223 may be used for storage of program variables or data.

Nesting of subroutines within subroutines can continue up to 8 times without overflowing the stack. If overflow does occur the deepest address stored (locations 8 and 9) will be overwritten and lost since the stack pointer overflows from 111 to 000. It also underflows from 000 to 111.

The value of the saved contents of the program counter is different for an interrupt CALL compared to a normal CALL to subroutine. With an interrupt CALL, the program counter return address is saved; with a subroutine CALL, the saved program counter value is one less than the program counter return address.

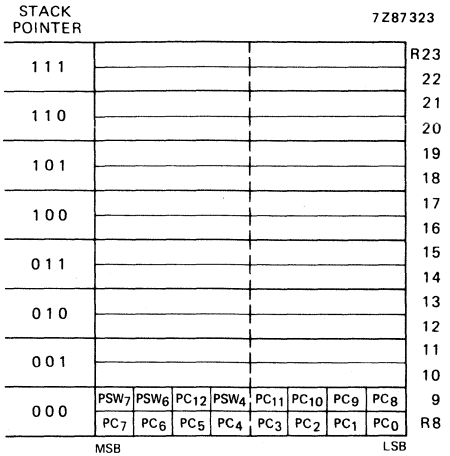


Fig. 6 Program counter stack.

IDLE and STOP modes

IDLE mode

When the microcontroller enters the IDLE mode via the IDLE instruction (H'01') the oscillator, timer/counter and serial I/O are kept running. The microcontroller exits from the IDLE mode by one of three interrupts if they are enabled or by activating a RESET. If the interrupt is not enabled the processor will remain in the IDLE mode. An active signal on the RESET pin restarts the microcontroller and a normal RESET sequence is executed (see Fig. 7).

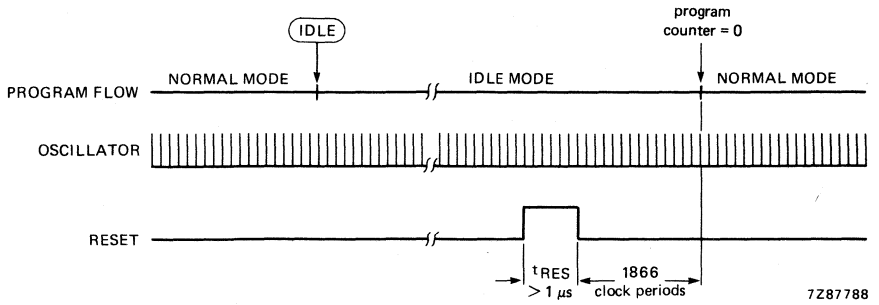


Fig. 7 Exit from IDLE mode via a RESET.

FUNCTIONAL DESCRIPTION (continued)

An active signal coming from an enabled interrupt causes the execution of the normal interrupt routine since normal interrupt scanning is still being carried out. A LOW-to-HIGH transition on the external interrupt pin (CE/$\overline{T0}$) reactivates the microcontroller. A HIGH level applied to CE/$\overline{T0}$ will reactivate the microcontroller only in the STOP mode. Thus, if CE/$\overline{T0}$ was HIGH before the microcontroller entered the IDLE mode, it must go LOW before the microcontroller can be reactivated (see Fig. 8).

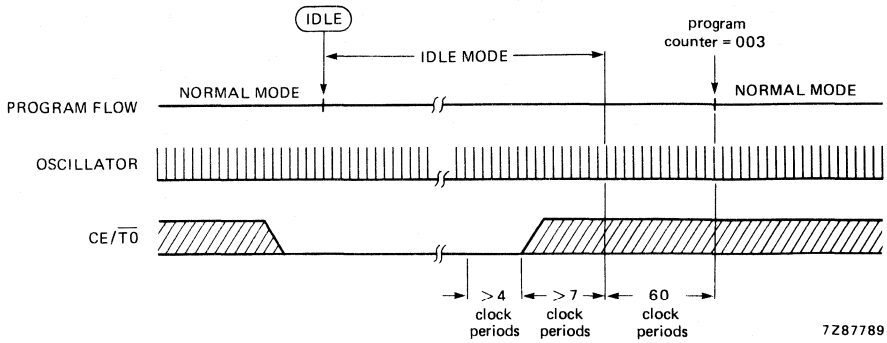


Fig. 8 Exit from IDLE mode via an interrupt.

Wake-up from the IDLE mode is ensured when CE/$\overline{T0}$ is LOW for 4 CP (clock periods) followed by a HIGH for 7 CP. After the initial forced CALL H'003' operation (60 CP) the program continues with the external interrupt service routine.

STOP mode

The microcontroller enters the STOP mode by the STOP instruction (H'22'). The oscillator is switched off. The internal status of the CPU, RAM contents and the state of I/O ports are not affected. The microcontroller can be brought-out of the STOP mode by an active signal at the external interrupt input or by an external RESET signal. When one of these two signals is applied an internal delay of 1866 CP is provided to ensure that all internal clocks are operating correctly before restart (see Fig. 9).

If the microcontroller exits from the STOP mode by activating RESET, a normal RESET sequence is executed.

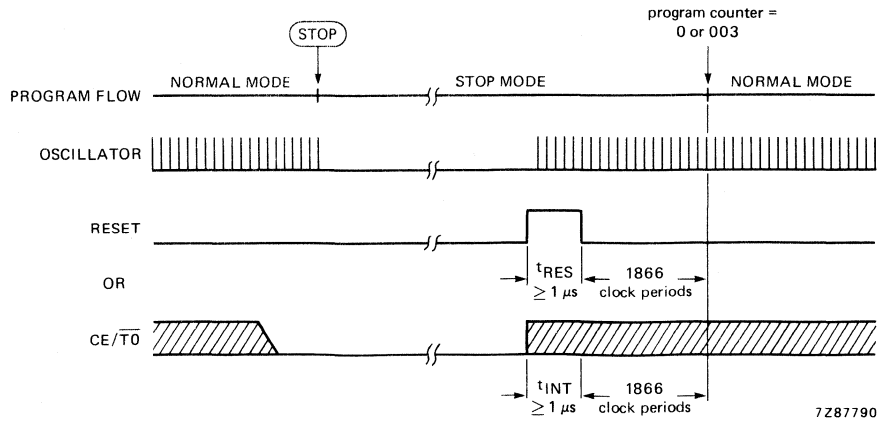


Fig. 9 Entering and exiting the STOP mode.

If the microcontroller exits the STOP mode by pulling the external interrupt input pin HIGH, an interrupt sequence is executed only if the external interrupt is enabled. In this event the microcontroller resumes the normal program sequence after returning from the interrupt routine, as in the normal mode. If the interrupt is not enabled, it continues the normal program sequence, executing the instruction following the STOP instruction.

The microcontroller is restarted by a HIGH level applied at the CE/$\overline{T0}$ pin, and not by a LOW-to-HIGH transition as in a normal interrupt mechanism.

When the CE/$\overline{T0}$ level is active during the STOP instruction then no STOP is executed.

A HIGH level on the external interrupt input of at least 1 μs will cause the microcontroller to exit the STOP mode.

I/O facilities

The PCD3343 family has 23 I/O lines arranged as:

- Port 0 parallel port of 8 lines (P00 to P07)
- Port 1 parallel port of 8 lines (P10 to P17)
- Port 2 parallel port of 4 lines (P20 to P23)
- SCLK serial I/O consisting of a data line shared with a parallel port line (P23) and a separate clock line SCLK
- CE/$\overline{T0}$ external interrupt and test input. When used as a test input can be directly tested by conditional branch instructions JT0 and JNT0
- T1 test input which can alter program sequences when tested by conditional jump instructions JT1 and JNT1. T1 also functions as an input to the 8-bit timer/event counter.

Parallel ports

All parallel ports can be used as outputs or inputs, their structure is quasi-bidirectional.
Output data written to a port is latched and remains unchanged until rewritten.
Input data is not latched and so must be present until read by an input instruction.

Input lines are fully CMOS compatible, output lines can drive one LS-TTL or CMOS load.

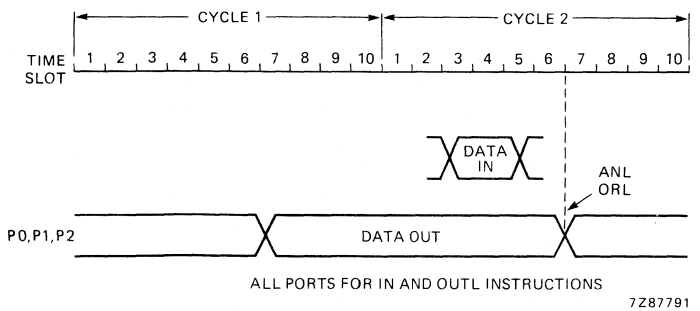


Fig. 10 Timing diagram of all ports on IN and OUTL instructions; for ANL and ORL instructions, the ports change on the time slot 7 of cycle 2.

Fig. 11 shows the quasi-bidirectional I/O interface with push-pull output and switched pull-up current source.
Each line is pulled up to V_{DD} via a constant current source (TR4), which is enabled via TR3 whenever one of the two output latches contains a logic 1. This current provides sufficient source current for a TTL HIGH level, yet can be pulled LOW by an external CMOS device, thus allowing the same pin to be used for both input and output.

FUNCTIONAL DESCRIPTION (continued)

When a logic 1 is written to the line for the first time (MQ = 1, SQ = 0), TR2 is switched on for the duration of the internal write pulse (one oscillator period), to provide a fast transition from logic 0 to logic 1. Subsequent writing of a logic 1 to the port lines will not switch TR2 on. This prevents unnecessary current through external components connected to the port lines of the same port which might be in the input mode and also connected to ground.

When a logic 0 is written to the line, TR3 switches off the current source. Current sinking capability is provided by TR1, which is now switched on. When used as an input, a logic 1 must first be written to the line, otherwise TR1 will remain low impedance.

In telephone applications this switched pull-up source may not be sufficient. Therefore the PCD3343 offers the possibility to select individually 19 of the 20 parallel port pins (not P23), by the following mask options:

Option 1- STANDARD PORT; quasi-bidirectional I/O with switched pull-up current source of 100 μA (typ.) and P-channel booster transistor TR2 (1,5 mA). TR2 is only active during 1 clock cycle (0,28 μs at 3,58 MHz).

Option 2- OPEN DRAIN; quasi-bidirectional I/O with only an N-channel open drain output. Application as an output requires connection of an external pull-up resistor (Fig. 12).

Option 3- PUSH-PULL OUTPUT; drive capability of the output will be 1,5 mA (typ.) at V_{DD} = 3 V in both polarities. To avoid a large current flowing through the output transistors during the input mode, these push-pull pins must only be used as outputs (Fig. 13).

Also, individual mask selection of the RESET state of these port pins can be achieved by appending the following options S and R to options 1, 2 or 3.

Option S-SET; after RESET this pin will be initialized to HIGH.

Option R-RESET; after RESET this pin will be initialized to LOW.

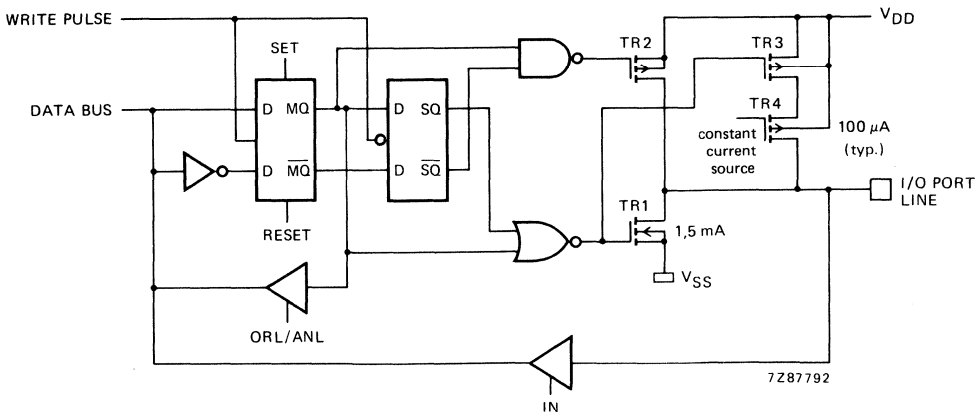


Fig. 11 Standard output with switched pull-up current source.

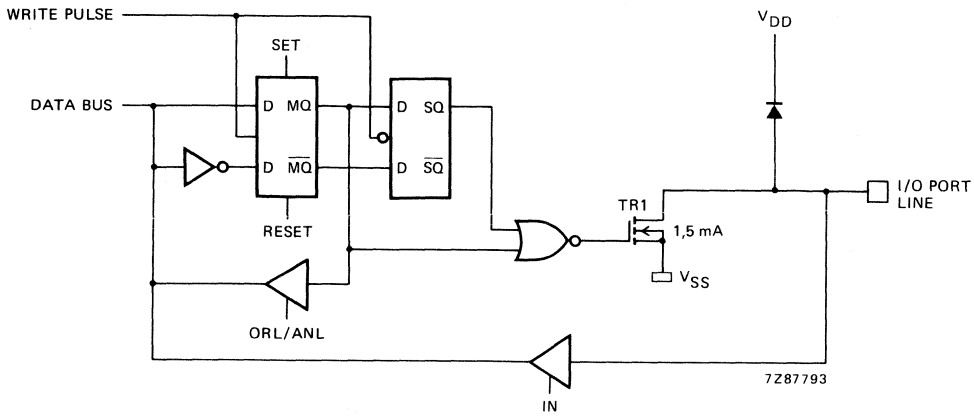


Fig. 12 Open drain output.

DEVELOPMENT DATA

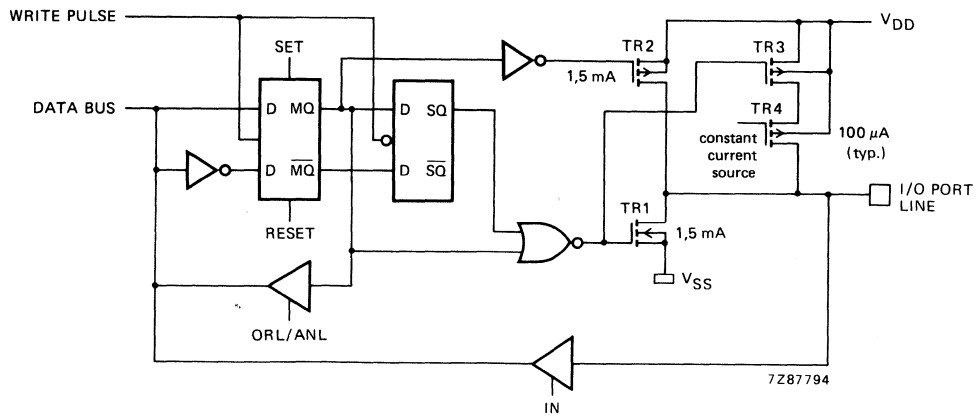


Fig. 13 Push-pull output.

FUNCTIONAL DESCRIPTION (continued)

Serial I/O (SIO)

The PCD3343 has an on-chip serial I/O interface. This SIO interface is a versatile feature in an intelligent telephone set, as shown in application diagram Fig. 32.

In this application the SIO is used to communicate with the different peripherals, such as:

- DTMF generator (PCD3312)
- LCD drivers (PCF8577)
- External RAM (PCD8571)
- Clock calendar (PCB8573)

No extra hardware is required for decoding, addressing and data processing.

Whereas a normal microcontroller must regularly monitor the serial data bus for the presence of data, the serial I/O interface detects, receives and converts the serial data stream into parallel format without interrupting the execution of the current program. An interrupt is sent to the PCD3343 only when a complete byte is received. It then reads the data byte in one instruction. Likewise during transmission the serial I/O interface performs parallel to serial conversion and subsequent serial output of the data. The microcontroller is only interrupted in the execution of its programmed tasks when a complete byte has been transmitted.

The design of the PCD3343 serial I/O system allows any number of devices from PCF8500 family (clips) to be connected via the two-line serial bus. The ability of any devices to communicate, without interrupting the operation of any other devices on the bus, is an outstanding attribute of the system. This is achieved by allocating a specific 7-bit address to each device and providing a system whereby a device reacts only to a message prefixed with its own address or the 'general CALL' address. Address recognition is performed by the interface hardware so that operation of the microcontroller need only be interrupted when a valid address has been received. This saves significant processing time and memory space compared with a conventional microcontroller employing a software serial interface. When the addressing facility is not required, for instance in a system with only two microcontrollers, direct data transfer without addressing can be performed. In multi-master systems, an automatically invoked arbitration procedure prevents two or more devices from continuing simultaneous transmission.

In NORMAL (running) and IDLE mode, the serial I/O logic remains active; its internal system clock will be switched off when there is no activity on the serial bus.

After execution of the STOP instruction, the oscillator of the PCD3343 is switched off. This means that the serial I/O logic will remain in the state it was at the occurance of the STOP instruction. To avoid "bus block" problems and to assure correct start-up of the bus after exit from the STOP mode, the user should disable the serial logic (ESO = 0) prior to the execution of the STOP instruction. This must be carried out only when the PCD3343 has finished a serial data transfer.

Serial I/O interface

Figure 14 shows the serial I/O interface. The clock line of the serial bus has exclusive use of pin 3 (SCLK) while the data line shares pin 2 (serial data) with the I/O line P23 of port 2. When the serial I/O is enabled, P23 is disabled as a parallel port line; (P23 and SCLK only open drain).

The microcontroller and interface communicate via the internal microcontroller bus and the Serial Interrupt Request line. Data and information controlling the operation of the interface are stored in four registers:

- Data shift register (S0)
- Serial I/O interface status word (S1)
- Serial clock control word (S2)
- Address register

Data shift register (S0)

Register S0 converts serial data to parallel format and vice versa. A pending interrupt is generated only after a complete byte has been transmitted, or after a complete data byte, specific address or 'general CALL' address has been received. The most significant bit is transmitted first.

Serial I/O interface status word (S1)

Register S1 provides information concerning the state of the interface and stores information from the microcontroller. Bits 0 to 3 are duplicated: control bits in these positions can only be written by the microcontroller, while interface bits can only be read.

MST and TRX (see Table 1)

These bits determine the operating mode of the serial I/O interface.

Table 1 Operating modes of the serial I/O interface

MST	TRX	operating mode
0	0	slave receiver
1	0	master receiver
0	1	slave transmitter
1	1	master transmitter

BB: Bus Busy.

This is the flag which indicates the status of the bus.

PIN: Pending Interrupt Not

PIN = '0' indicates the presence of a pending interrupt, which will cause a Serial Interrupt Request when the serial interrupt mechanism is enabled.

ESO: Enable Serial output

The ESO flag enables/disables the serial I/O interface: ESO = '1' enables, ESO = '0' disables. ESO can only be written by software.

BC0, BC1 and BC2

Bits BC0, BC1 and BC2 indicate the number of bits received or transmitted in a data stream. These bits can only be written by software.

AL: Arbitration Lost

The arbitration lost flag is set by hardware when the serial I/O interface, as master transmitter, loses a bus arbitration procedure.

AAS: Addressed As Slave

This flag is set by hardware when the interface detects either its own specific address or the 'general CALL' address as the first byte of a transfer and the interface has been programmed to operate in the address recognition mode.

AD0: Address Zero

This flag is set by hardware after detection of the 'general CALL' address when the interface is operating in the address recognition mode.

LRB: Last Received Bit

This contains either the last data bit received or, for a transmitting device in the acknowledgement mode, the acknowledgement signal from the receiving device.

Bits AL, AAS, AD0 and LRB can only be read by software.

FUNCTIONAL DESCRIPTION (continued)

Serial clock control word (S2)

Bits 0 to 4 of the clock control register S2 are used to set the frequency of the serial clock signal. When a 3,58 MHz crystal is used, the frequency of the serial clock can be varied between 92 kHz and 580 Hz (see Table 2). An asymmetrical clock with a HIGH-to-LOW ratio of 3 : 1 can be generated using bit 5. The asymmetrical clock allows a microcontroller more time per clock period for sampling the data line, making the timing of this action less critical. Bit 6 can be used to activate the acknowledge mode of the serial I/O. S2 is a write only register.

Address register

The address register contains the 7-bit address back-up latches and the bit (ALS) used to enable/disable the address recognition mode. The address register can be written using the MOV S0, A and MOV S0, # data instructions, but only when ES0 = '0'.

Serial I/O interrupt logic

An EN SI instruction enables and a DIS SI instruction disables the interrupt logic. When the logic is enabled, a pending interrupt results in a serial I/O interrupt to the processor, causing a CALL to location 5 in the ROM. When disabled, the presence of an interrupt is still indicated by PIN in S1, allowing the interrupt to be serviced. However, vectored interrupt will not occur.

Table 2 SIO clock pulse frequency control when using a 3,58 MHz crystal

hexadecimal S20-S24 code	divisor	f_{SCLK} (kHz) (approximate)
0	not allowed	
1	39	92
2	45	80
3	51	70
4	63	57
5	75	48
6	87	41
7	99	36
8	123	29
9	147	24
A	171	21
B	195	18
C	243	15
D	291	12
E	339	11
F	387	9,2
10	483	7,4
11	579	6,2
12	675	5,3
13	771	4,6
14	963	3,7
15	1155	3,1
16	1347	2,7
17	1539	2,3
18	1923	1,9
19	2307	1,6
1A	2691	1,3
1B	3075	1,2
1C	3843	0,93
1D	4611	0,78
1E	5379	0,67
1F	6147	0,58

DEVELOPMENT DATA

FUNCTIONAL DESCRIPTION (continued)

Table 3 Serial I/O addresses for telephony peripherals

type	address 7	6	5	4	3	2	1	0	description
PCF8570A	1	0	1	0	A2	A1	X	R/$\overline{W}$	2 K RAM
PCF8570	1	0	1	0	A2	A1	A0	R/$\overline{W}$	2 K RAM
PCD8571	1	0	1	0	A2	A1	A0	R/$\overline{W}$	1 K RAM
PCD3311	0	1	0	0	1	0	A0	R/$\overline{W}$	DTMF dialler
PCD3312	0	1	0	0	1	0	A0	R/$\overline{W}$	DTMF dialler
PCE2111	0	0	0	0	0	0	1	0	LCD driver *
PCD8573	1	1	0	1	0	A1	A0	R/$\overline{W}$	clock calendar
PCF8574	0	0	1	1	A2	A1	A0	R/$\overline{W}$	8-bit I/O expander
PCF8576	0	1	1	1	0	0	SA0	R/$\overline{W}$	1 : 4 LCD driver
PCF8577	0	1	1	1	0	1	0	R/$\overline{W}$	1 : 2 LCD driver

* LCD driver requires an additional enable line.

DEVELOPMENT DATA

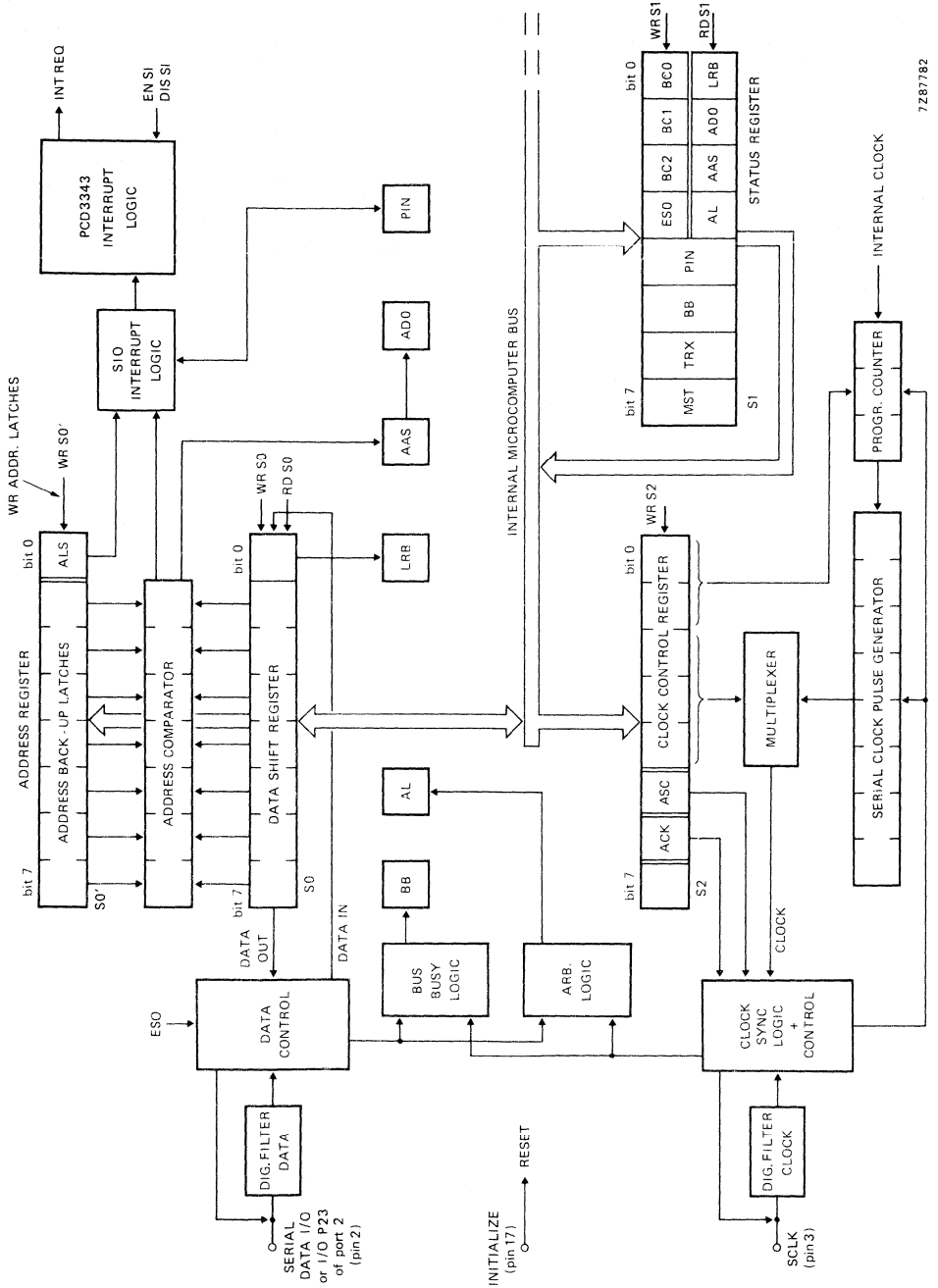


Fig. 14 Serial I/O interface.

FUNCTIONAL DESCRIPTION (continued)

Interrupts (see Fig. 15)

When the external interrupt is enabled, a LOW-to-HIGH transition on the CE/$\overline{T0}$ input initiates an external interrupt subroutine which causes a CALL to program memory location 3 following completion of the current instruction.
The interrupt must remain enabled until the interrupt instruction is completed, otherwise the next instruction of the main program will be executed. Serial I/O interrupt, when enabled, causes a CALL to location 5, and a timer/event counter overflow forces a CALL to location 7 when the timer interrupt is enabled.

When an interrupt subroutine starts, the contents of the program counter and bits 4, 6 and 7 of the PSW have been saved in the program counter stack. Accumulator contents have to be saved by software. Interrupt acknowledgement can be carried out by software via port pins. All interrupt subroutines must reside in memory bank 0.

Since the interrupt system is single level, once an interrupt is detected, all further interrupt requests are latched, but ignored, pending a RETR instruction to re-enable the interrupt input logic. After executing RETR, the program continues in the main part; this is independent of the occurance of a second interrupt during the running of the first routine. If 2 or 3 interrupts occur simultaneously, their priority is:

- (1) external
- (2) serial I/O
- (3) timer/event counter

An external interrupt can be generated by using the timer/counter in the event counter mode. The counter is first preset to (H'FF'), then EN TCNTI instruction is executed. A LOW-to-HIGH transition of the T1 input will then initiate an interrupt subroutine and cause a CALL to location 7.

On execution of a DIS I instruction, the PCD3343 always clears the digital filter/latch and the External Interrupt Flag.

The Timer Flag (TF) is reset only when the JTF or JNTF instruction is executed or after RESET.

The Timer Interrupt Flag is set when timer overflow occurs, only if the timer interrupt is enabled.

The microcontroller will exit the IDLE mode when any one of the following three interrupts is enabled:

- External
- Serial I/O
- Timer/event counter

There is no internal pull-up or pull-down device connected to the external interrupt input (pin 12). If required pin 12 must be externally connected to a resistor ($R \leqslant 100\ k\Omega$). When the external interrupt is not used pin 12 must be connected to V_{SS}.

DEVELOPMENT DATA

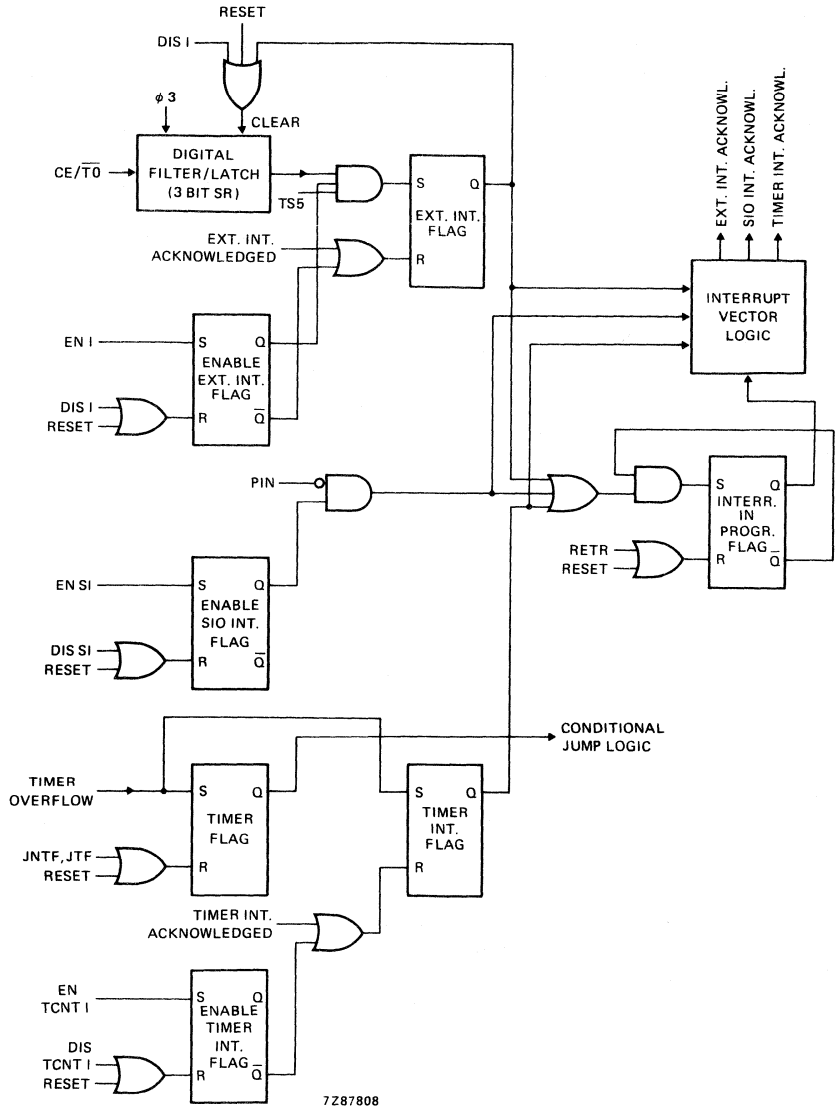


Fig. 15 Interrupt logic.

Notes to figure 15

1. CE/$\overline{T0}$ positive edge is always latched in the digital filter/latch.
2. Correct interrupt timing in ensured when CE/$\overline{T0}$ is LOW for >4 CP followed by a HIGH for >7 CP.
3. When the interrupt in progress flag is set, further interrupts are latched but ignored, until RETR is executed.
4. A DIS I instruction always clears a pending external interrupt.

FUNCTIONAL DESCRIPTION (continued)

Oscillator (see Fig. 16)

The 3,58 MHz oscillator can be inhibited by the STOP instruction under software control. It is also inhibited when a low-voltage condition is present to prevent discharge of a weak back-up battery.

Provided the supply voltage is within the operating range, the oscillator will be restarted after a STOP instruction by a HIGH level at either the CE/$\overline{T0}$ or RESET pin.

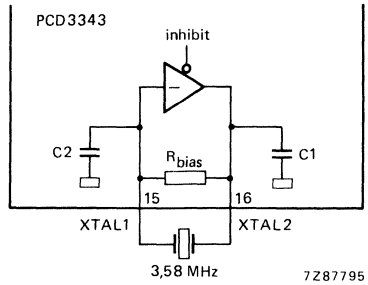


Fig. 16 Oscillator with integrated elements.

The oscillator has the output drive capability for the DTMF generator (PCD3311/3312) via pin 16 (XTAL 2). An external clock can be applied to pin 15 (XTAL 1). A machine cycle consists of 10 time slots, each time slot being 3 oscillator periods.

In telephony applications the 3,58 MHz crystal provides a 8,4 μs machine cycle. The range of the clock frequency is from 100 kHz up to a maximum which is a function of the supply voltage (see Fig. 23).

Timer/event counter (see Fig. 17)

An internal 8-bit up-counter is provided. This can count external events, modulo-32 machine cycles, or machine cycles directly. Table 4 gives the instructions that control the counter and the prescaler, and the functions performed.

When used as a timer, the input to the counter is either the overflow or input of a 5-bit prescaler. When used as an event counter, LOW-to-HIGH transitions on pin 13 (T1) are counted. The maximum rate at which the counter may be incremented is once every machine cycle (182,6 kHz for a 8,4 μs machine cycle). When the counter overflows, the timer flag is set. The flag can be tested and reset using the JTF (jump if timer flag = 1) or JNTF instruction. Overflow also generates an interrupt to the processor via setting of the Timer Interrpt Flag when the timer/event counter interrupt is enabled.

Table 4 Timer/event counter control

function	timer mode modulo-1, modulo-32*	counter mode
CLEAR	MOV T,A (A) = 0 or RESET	MOV T,A (A) = 0 or RESET
PRESET	MOV T,A	MOV T,A
START	STRT T	STRT CNT
STOP	STOP TCNT or RESET	STOP TCNT or RESET
TEST	JTF/JNTF	JTF/JNTF
READ**	MOV A,T	MOV A,T

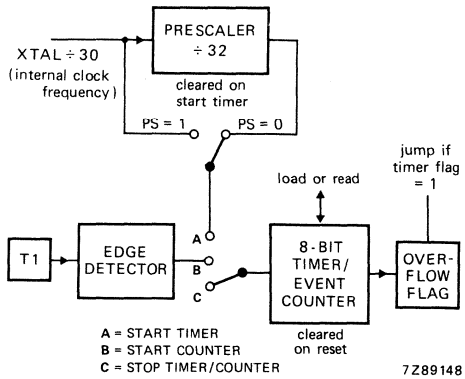


Fig. 17 Timer/event counter.

DEVELOPMENT DATA

Program status word (see Fig. 18)

The program status word (PSW) is an 8-bit word (1 byte) in the CPU which stores information about the current status of the microcontroller.
The PSW bits are:

- Bits 0 to 2 — stack pointer bits (SP_0, SP_1, SP_2)
- Bit 3 — prescaler select (PS);
  0 = modulo-32; 1 = modulo-1 (no prescaling)
- Bit 4 — working register bank select (RBS);
  0 = register bank 0; 1 = register bank 1
- Bit 5 — not used (1)
- Bit 6 — auxiliary carry (AC); half-carry bit generated by an ADD instruction and used by the decimal adjust instruction DA A
- Bit 7 — carry (CY); the carry flag indicates that previous operation has resulted in an overflow of the accumulator.

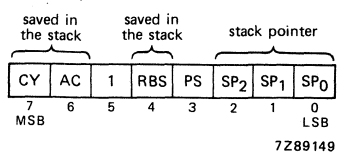


Fig. 18 Program status word.

* With prescaler select, PS = 0, the timer counts modulo-32 machine cycles, with PS = 1 it counts modulo-1 cycles (prescaler not used); prescaler cleared with STRT T, prescaler not readable.

** READ does not disturb the counting process.

FUNCTIONAL DESCRIPTION (continued)

Program status word (continued)

All bits can be read using the MOV A, PSW instruction. Bits 7 and 6 are set and cleared by CPU operation. Bit 4 can be changed by a SEL RB instruction, bit 3 by the MOV PSW, A instruction, and bits 0, 1 and 2 by the CALL, RET or RETR instructions and in the event of an interrupt. Bits 7, 6 and 4 are stored in the program counter stack during subroutine and interrupt calls. These bits are restored in the PSW with a RETR (return and restore) instruction which must be used at the end of an interrupt and can be used at the end of a normal subroutine. The RET instruction has no restore feature and cannot be used at the end of an interrupt.

Program counter (see Fig. 19)

A 13-bit program counter is used to facilitate 8 K bytes of ROM being addressed. The arrangement of the bits is shown in figure 19. During an interrupt subroutine PC_{11} and PC_{12} are forced to logic 0. All 13 bits are saved in the stack during CALL and interrupt routines.

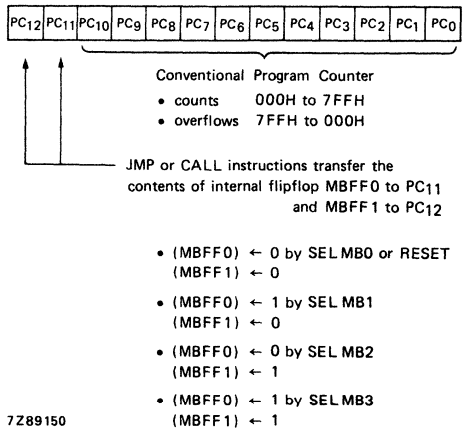


Fig. 19 Program counter.

Central processing unit

The PCD3343 has arithmetic, logical and branching capabilities. The DA A, SWAP A and XCHD instructions simplify BCD arithmetic and the handling of nibbles. The MOVP A,@A instruction permits efficient table look-up from the current ROM page.

Conditional branch logic

The conditional branch logic within the processor enables several conditions, internal and external to the processor, to be tested by the user's program. Table 5 lists the conditional jump instructions used to change the program sequence. The DJNZ instruction decrements a designated register or data memory location and branches if the contents are not zero. This instruction is useful for looping control. The JMPP@A instruction allows multiway branches to destinations determined by the contents of the accumulator.

Table 5 Conditional branches

test	jump condition	jump instruction
accumulator	all bits zero	JZ
	any bit non-zero	JNZ
accumulator bit test	1	JB0 to JB7
carry flag	1	JC
	0	JNC
timer overflow flag	1	JTF
	0	JNTF
test input T0	1	JNT0
	0	JT0*
test input T1	1	JT1
	0	JNT1
register	non-zero	DJNZ

Test input T1 (pin 13)

The T1 input line can be used as:

- A test input for branch instructions JT1 and JNT1
- An external input to the event counter

When used as a test input:

- JT1 instruction tests for logic 1 level
- JNT1 instruction tests for logic 0 level

When used as an input to the event counter, T1 must be LOW for > 4 CP, followed by a HIGH for > 4 CP. The transition can be recognized with a repetition rate of once per 30 oscillator clock periods (1 machine cycle).

There is no internal pull-up or pull-down resistor connected to the T1 input. If required it must be externally connected to a resistor ($R = \leqslant 100\ k\Omega$). When T1 is not used pin 13 must be connected to V_{DD} or V_{SS}.

Reset (pin 17)

A positive-going signal on the RESET input/output:

- Sets the program counter to zero
- Selects location 0 of memory band 0 and register bank 0
- Sets the stack pointer to zero (000); pointing to RAM address 8
- Disables the interrupts (external, timer and serial I/O)
- Stops the timer/event counter, then sets it to zero
- Sets the timer prescaler to modulo-32
- Resets the timer flag
- Sets all ports according to reset states
- Sets the serial I/O to slave receiver mode and disables the serial I/O
- Cancels IDLE and STOP mode

After the voltage is applied to RESET an internal delay of 1866 CP is introduced before the microcontroller commences operation.

* Because of the inverted interrupt input CE/$\overline{T0}$ the conditional jump JT0 is also inverted.

FUNCTIONAL DESCRIPTION (continued)

Power-on-reset and low-voltage detection (see Fig. 20)

In telephony applications, correct operation of the PCD3343 during moments of slowly changing supply voltages and low-voltage conditions is essential. This is achieved by the addition of an internal power-on-reset and low-voltage detection circuit.
To allow an external RESET signal being fed into the PCD3343, the reset pin (pin 17) has been configured as an input/output.

While a reset condition exists in the detection circuit, pin 17 is pulled HIGH by TR1 controlled by the reset circuit.
When the reset condition is not present a pull-down current source (TR2) will be activated. TR2 forces pin 17 LOW thus removing the RESET signal from the microcontroller.

Since the level at pin 17 is recognized by the microcontroller, the reset time constant can be stretched by connecting an external capacitor between V_{DD} and pin 17 (see Fig. 22).

The signal at pin 17 can also be used as an output to reset other devices in the system.

The internal reset circuit monitors the PCD3343 supply voltage. If the voltage drops below the switching level (typ. 1,3 V), a reset (HIGH) is applied to pin 17. This reset is removed (pin 17 goes LOW), after a fixed delay (t_d), when the supply voltage rises above the switching level again. The delay ensures a complete reset even when the supply voltage quickly rises above switching level after initial switch-on.

During a low-voltage condition the oscillator is inhibited to prevent complete discharge of a weak battery. The timing of the power-on-reset and low-voltage detection circuit is shown in figure 21.

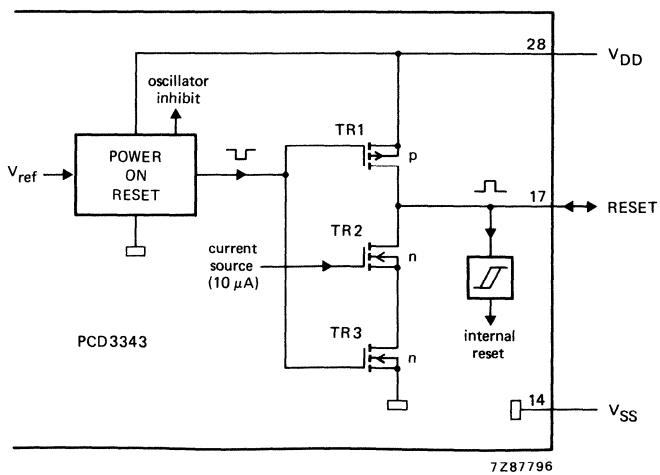
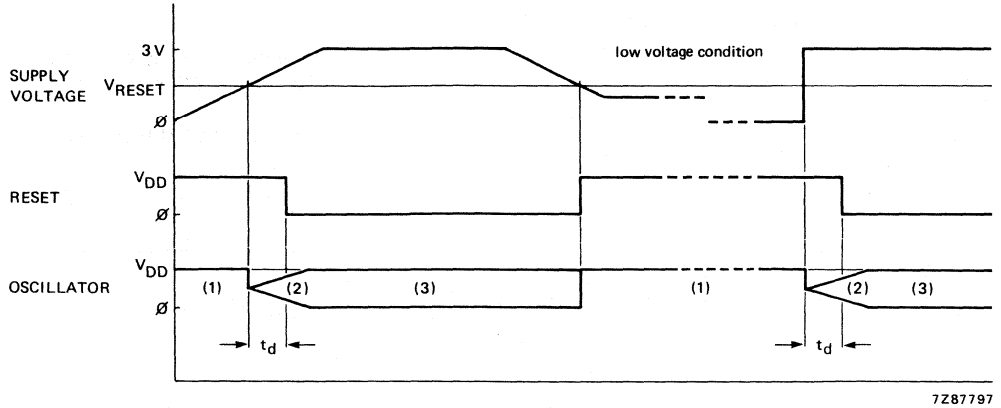


Fig. 20 Power-on-reset configuration.



Where: (1) Oscillator inhibited
(2) Oscillator starting
(3) Oscillator running, but may be stopped with a STOP condition

Fig. 21 Timing of power-on-reset and low-voltage detection.

DEVELOPMENT DATA

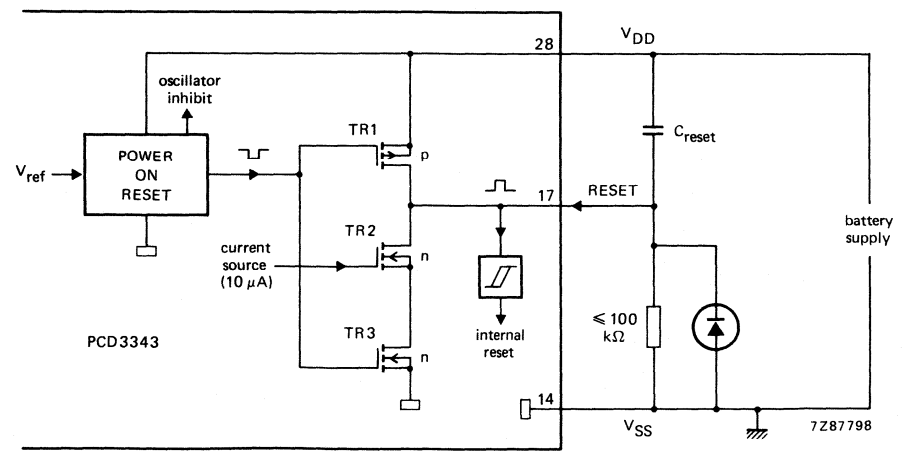


Fig. 22 Stretched power-on reset with external capacitor.

INSTRUCTION SET

The PCD3343 instruction set consists of over 80 one and two byte instructions and is based on the MAB8048 instruction set. New instructions include those for serial I/O operation and memory bank selection. Program code efficiency is high because all RAM locations and all ROM locations on a 256 byte page require only a single byte address.

Table 8 gives the instruction set of the PCD3343. Table 7 shows the instruction map and Table 6 details the symbols and definition descriptions that are used.

Table 6 Symbols and definitions used in Table 8

symbol	definition description
A	accumulator
addr	program memory address
Bb	bit designation (b = 0-7)
RBS	register bank select
C	carry bit (bit CY)
CNT	event counter
D	mnemonic for 4-bit digit (nibble)
data	8-bit number or expression
I	interrupt
MB	memory bank
MBFF	memory bank flip-flop
P	mnemonic for 'in-page' operation
PC	program counter
Pp	port designation (p = 0, 1 or 2)
PSW	program status word
RB	register bank
Rr	register designation (r = 0-7)
Sn	serial I/O register
SP	stack pointer
T	timer
TF	timer flag
T0, T1	test 0 and 1 inputs
#	immediate data prefix
@	indirect address prefix
(X)	contents of X
((X))	contents of location addressed by X
←	is replaced by
↔	is exchanged with

Table 7 PCD3343 instruction map

first hexadecimal character of opcode ↓	second hexadecimal character of opcode															
	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	NOP	IDLE		ADD A,#data	JMP page 0	EN I	JNTF addr	DEC A	IN A,Pp 0	1	2		MOV A,Sn 0	1		
1	INC @Rr 0	1	JBO addr	ADDC A,#data	CALL page 0	DIS I	JTF addr	INC A	INC Rr 0	1	2	3	4	5	6	7
2	XCH A,@Rr 0	1	STOP	MOV A,#data	JMP page 1	EN TCNTI	JNTO addr	CLR A	XCH A,Rr 0	1	2	3	4	5	6	7
3	XCHD A,@Rr 0	1	JB1 addr		CALL page 1	DIS TCNTI	JTO addr	CPL A	OUTL Pp,A 0	1	2		MOV Sn,A 0	1	2	
4	ORL A,@Rr 0	1	MOV A,T	ORL A,#data	JMP page 2	STRT CNT	JNT1 addr	SWAP A	ORL A,Rr 0	1	2	3	4	5	6	7
5	ANL A,@Rr 0	1	JB2 addr	ANL A,#data	CALL page 2	STRT T	JT1 addr	DA A	ANL A,Rr 0	1	2	3	4	5	6	7
6	ADD A,@Rr 0	1	MOV T,A		JMP page 3	STOP TCNT		RRC A	ADD A,Rr 0	1	2	3	4	5	6	7
7	ADDC A,@Rr 0	1	JB3 addr		CALL page 3			RR A	ADDC A,Rr 0	1	2	3	4	5	6	7
8				RET	JMP page 4	EN SI			ORL Pp,#data 0	1	2					
9			JB4 addr	RETR	CALL page 4	DIS SI	JNZ addr	CLR C	ANL Pp,#data 0	1	2		MOV Sn,#data 0	1	2	
A	MOV @Rr,A 0	1		MOVP A,@A	JMP page 5	SEL MB2		CPL C	MOV Rr,A 0	1	2	3	4	5	6	7
B	MOV @Rr,#data 0	1	JB5 addr	JMPP @A	CALL page 5	SEL MB3			MOV Rr,#data 0	1	2	3	4	5	6	7
C	DEC @Rr 0	1			JMP page 6	SEL RB0	JZ addr	MOV A,PSW	DEC Rr 0	1	2	3	4	5	6	7
D	XRL A,@Rr 0	1	JB6 addr	XRL A,#data	CALL page 6	SEL RB1		MOV PSW,A	XRL A,Rr 0	1	2	3	4	5	6	7
E	DJNZ @Rr,addr 0	1			JMP page 7	SEL MB0	JNC addr	RL A	DJNZ Rr, addr 0	1	2	3	4	5	6	7
F	MOV A,@Rr 0	1	JB7 addr		CALL page 7	SEL MB1	JC addr	RLC A	MOV A,Rr 0	1	2	3	4	5	6	7

INSTRUCTION SET (continued)

Table 8 Instruction set

	mnemonic	opcode (hex.)	bytes/ cycles	description	function		notes
ACCUMULATOR	ADD A, Rr	6*	1/1	Add register contents to A	(A)←(A) + (Rr)	r = 0–7	1
	ADD A, @Rr	60 61	1/1	Add RAM data, addressed by Rr, to A	(A)←(A) + ((R0)) (A)←(A) + ((R1))		1
	ADD A, #data	03 data	2/2	Add immediate data to A	(A)←(A) + data		1
	ADDC A, Rr	7*	1/1	Add carry and register contents to A	(A)←(A) + (Rr) + (C)	r = 0–7	1
	ADDC A, @Rr	70 71	1/1	Add carry and RAM data, addressed by Rr, to A	(A)←(A) + ((R0)) + (C) (A)←(A) + ((R1)) + (C)		1
	ADDC A, #data	13 data	2/2	Add carry and immediate data to A	(A)←(A) + data + (C)		1
	ANL A, Rr	5*	1/1	'AND' Rr with A	(A)←(A) AND (Rr)	r = 0–7	
	ANL A, @Rr	50 51	1/1	'AND' RAM data, addressed by Rr, with A	(A)←(A) AND ((R0)) (A)←(A) AND ((R1))		
	ANL A, #data	53 data	2/2	'AND' immediate data with A	(A)←(A) AND data		
	ORL A, Rr	4*	1/1	'OR' Rr with A	(A)←(A) OR (Rr)	r = 0–7	
	ORL A, @Rr	40 41	1/1	'OR' RAM data, addressed by Rr, with A	(A)←(A) OR ((R0)) (A)←(A) OR ((R1))		
	ORL A, #data	43 data	2/2	'OR' immediate data with A	(A)←(A) OR data		
	XRL A, Rr	D*	1/1	'XOR' Rr with A	(A)←(A) XOR (Rr)	r = 0–7	
	XRL A, @Rr	D0 D1	1/1	'XOR' RAM, addressed by Rr, with A	(A)←(A) XOR ((R0)) (A)←(A) XOR ((R1))		
	XRL A, #data	D3 data	2/2	'XOR' immediate data with A	(A)←(A) XOR data		
	INC A	17	1/1	increment A by 1	(A)←(A) + 1		
	DEC A	07	1/1	decrement A by 1	(A)←(A) −1		
	CLR A	27	1/1	clear A to zero	(A)←0		
	CPL A	37	1/1	one's complement A	(A)←NOT(A)		
	RL A	E7	1/1	rotate A left	$(A_{n+1})\leftarrow(A_n)$ $(A_0)\leftarrow(A_7)$	n = 0–6	

DEVELOPMENT DATA

ACCUMULATOR (cont.)	RLC A	F7	1/1	rotate A left through carry	$(A_{n+1})\leftarrow A_n$ $(A_0)\leftarrow(C), (C)\leftarrow(A_7)$	n = 0–6	2
	RR A	77	1/1	rotate A right	$(A_n)\leftarrow(A_{n+1})$ $(A_7)\leftarrow(A_0)$	n = 0–6	
	RRC A	67	1/1	rotate A right through carry	$(A_n)\leftarrow(A_{n+1})$ $(A_7)\leftarrow(C), (C)\leftarrow(A_0)$	n = 0–6	2
	DA A	57	1/1	decimal adjust A			2
	SWAP A	47	1/1	swap nibbles of A	$(A_{4-7})\leftrightarrow(A_{0-3})$		
DATA MOVES	MOV A, Rr	F*	1/1	move register contents to A	(A)←(Rr)	r = 0–7	
	MOV A, @Rr	F0 F1	1/1	move RAM data, addressed by Rr, to A	(A)←((R0)) (A)←((R1))		
	MOV A, #data	23 data	2/2	move immediate data to A	(A)←data		
	MOV Rr, A	A*	1/1	move accumulator contents to register	(Rr)←(A)	r = 0–7	
	MOV @Rr, A	A0 A1	1/1	move accumulator contents to RAM location addressed by Rr	((R0))←(A) ((R1))←(A)		
	MOV Rr, #data	B* data	2/2	move immediate data to Rr	(Rr)←data		
	MOV @Rr, #data	B0 data B1 data	2/2	move immediate data to RAM location addressed by Rr	((R0))←data ((R1))←data		
	XCH A, Rr	2*	1/1	exchange accumulator contents with Rr	$(A)\leftrightarrow(Rr)$	r = 0–7	
	XCH A, @Rr	20 21	1/1	exchange accumulator contents with RAM data addressed by Rr	$(A)\leftrightarrow((R0))$ $(A)\leftrightarrow((R1))$		
	XCHD A, @Rr	30 31	1/1	exchange lower nibbles of A and RAM data addressed by Rr	$(A_{0-3})\leftrightarrow((R0_{0-3}))$ $(A_{0-3})\leftrightarrow((R1_{0-3}))$		
	MOV A, PSW	C7	1/1	move PSW contents to accumulator	(A)←(PSW)		
	MOV PSW, A	D7	1/1	move accumulator bit 3 to PSW_3	$(PSW_3)\leftarrow(A_3)$		3
	MOVP A, @A	A3	1/2	move indirectly addressed data in current page to A	$(PC_{0-7})\leftarrow(A), (A)\leftarrow((PC))$		
FLAGS	CLR C	97	1/1	clear carry bit	(C)←0		2
	CPL C	A7	1/1	complement carry bit	(C)←NOT(C)		2

	mnemonic	opcode (hex.)	bytes/ cycles	description	function	notes
REGISTER	INC Rr	1*	1/1	increment register by 1	(Rr)←(Rr) + 1 r = 0–7	
	INC @Rr	10 11	1/1	increment RAM data, addressed by Rr, by 1	((R0))←((R0)) + 1 ((R1))←((R1)) + 1	
	DEC Rr	C*	1/1	decrement register by 1	(Rr)←(Rr) – 1 r = 0–7	
	DEC @Rr	C0 C1	1/1	decrement RAM data, addressed by Rr, by 1	((R0))←((R0)) – 1 ((R1))←((R1)) – 1	
BRANCH	JMP addr	● 4 address	2/2	unconditional jump within a 2 K bank	(PC_{8-10})←$addr_{8-10}$ (PC_{0-7})←$addr_{0-7}$ (PC_{11-12})←MBFF 0–1	
	JMPP @A	B3	1/2	indirect jump within a page	(PC_{0-7})←((A))	
	DJNZ Rr, addr	E* address	2/2	decrement Rr by 1 and jump if not zero to addr	(Rr)←(Rr) – 1 r = 0–7 if (Rr) not zero (PC_{0-7})←addr	
	DJNZ @Rr, addr	E0	2/2	decrement RAM data, addressed by Rr by 1 and jump if not zero to addr	((R0))←((R0)) – 1 if ((R0)) not zero (PC_{0-7})←addr	
		E1			((R1))←((R1)) – 1 if ((R1)) not zero (PC_{0-7})←addr	
	JBb addr	▲ 2 address	2/2	jump to addr if Acc. bit b = 1	if b = 1 : (PC_{0-7})←addr b = 0–7	
	JC addr	F6 address	2/2	jump to addr if C = 1	if C = 1 : (PC_{0-7})←addr	
	JNC addr	E6 address	2/2	jump to addr if C = 0	if C = 0 : (PC_{0-7})←addr	
	JZ addr	C6 address	2/2	jump to addr if A = 0	if A = 0 : (PC_{0-7})←addr	
	JNZ addr	96 address	2/2	jump to addr if A is NOT zero	if A≠0 : (PC_{0-7})←addr	
	JT0 addr	36 address	2/2	jump to addr if T0 = 0	if T0 = 0: (PC_{0-7})←addr	
	JNT0 addr	26 address	2/2	jump to addr if T0 = 1	if T0 = 1: (PC_{0-7})←addr	
	JT1 addr	56 address	2/2	jump to addr if T1 = 1	if T1 = 1: (PC_{0-7})←addr	
	JNT1 addr	46 address	2/2	jump to addr if T1 = 0	if T1 = 0: (PC_{0-7})←addr	
	JTF addr	16 address	2/2	jump to addr if Timer Flag = 1	if TF = 1: (PC_{0-7})←addr	4
	JNTF addr	06 address	2/2	jump to addr if Timer Flag = 0	if TF = 0: (PC_{0-7})←addr	

TIMER/EVENT COUNTER	MOV A, T	42	1/1	move timer/event counter contents to accumulator	(A)←(T)	
	MOV T, A	62	1/1	move accumulator contents to timer/event counter	(T)←(A)	
	STRT CNT	45	1/1	start event counter		
	STRT T	55	1/1	start timer		
	STOP TCNT	65	1/1	stop timer/event counter		
	EN TCNTI	25	1/1	enable timer/event counter interrupt		
	DIS TCNTI	35	1/1	disable timer/event counter interrupt		
CONTROL	EN I	05	1/1	enable external interrupt		
	DIS I	15	1/1	disable external interrupt		
	SEL RB0	C5	1/1	select register bank 0	(RBS)←0	5
	SEL RB1	D5	1/1	select register bank 1	(RBS)←1	5
	SEL MB0	E5	1/1	select program memory bank 0	(MBFF0)←0, (MBFF1)←0	
	SEL MB1	F5	1/1	select program memory bank 1	(MBFF0)←1, (MBFF1)←0	
	SEL MB2	A5	1/1	select program memory bank 2	(MBFF0)←0, (MBFF1)←1	
	SEL MB3	B5	1/1	select program memory bank 3	(MBFF0)←1, (MBFF1)←1	
	STOP	22	1/1	enter STOP mode		
	IDLE	01	1/1	enter IDLE mode		
SUBROUTINE	CALL addr	▲ 4 address	2/2	jump to subroutine	$((SP))\leftarrow(PC), (PSW_{4,6,7})$ 6 $(SP)\leftarrow(SP)+1$ $(PC_{8-10})\leftarrow addr_{8-10}$ $(PC_{0-7})\leftarrow addr_{0-7}$ $(PC_{11-12})\leftarrow$MBFF 0–1	6
	RET	83	1/2	return from subroutine	$(SP)\leftarrow(SP)-1$ $(PC)\leftarrow((SP))$	6
	RETR	93	1/2	return from interrupt and restore bits 4, 6, 7 of PSW	$(SP)\leftarrow(SP)-1$ $(PSW_{4,6,7}) + (PC)\leftarrow((SP))$	6

	mnemonic	opcode (hex.)	bytes/ cycles	description	function	notes
PARALLEL INPUT/OUTPUT	IN A, Pp	08 09 0A	1/2	input port p data to accumulator	(A)←(P0) (A)←(P1) (A)←(P2)	 7
	OUTL Pp, A	38 39 3A	1/2	output accumulator data to port p	(P0)←(A) (P1)←(A) (P2)←(A)	
	ANL Pp, #data	98 99 9A	2/2	AND port p data with immediate data	(P0)←(P0) AND data (P1)←(P1) AND data (P2)←(P2) AND data	
	ORL Pp, #data	88 89 8A	2/2	OR port p data with immediate data	(P0)←(P0) OR data (P1)←(P1) OR data (P2)←(P2) OR data	
SERIAL INPUT/OUTPUT	MOV A, S_n	0C 0D	1/2	move serial I/O register contents to accumulator	(A)←(S0) (A)←(S1)	 8
	MOV S_n, A	3C 3D 3E	1/2	move accumulator contents to serial I/O register	(S0)←(A) (S1)←(A) (S2)←(A)	 9
	MOV S_n, #data	9C 9D 9E	2/2	move immediate data to serial I/O register	(S0)←data (S1)←data (S2)←data	
	EN SI	85	1/1	enable serial I/O interrupt		
	DIS SI	95	1/1	disable serial I/O interrupt		
	NOP	00	1/1	no operation		

Notes to Table 8

1. PSW CY, AC affected
2. PSW CY affected
3. PSW PS affected
4. Execution of JTF and JNTF instructions resets the Timer Flag (TF).

* : 8, 9, A, B, C, D, E, F
● : 0, 2, 4, 6, 8, A, C, E
▲ : 1, 3, 5, 7, 9, B, D, F

5. PSW RBS affected
6. PSW SP_0, SP_1, SP_2 affected
7. (A) = 1111 P23, P22, P21, P20.
8. (S1) has a different meaning for read and write operation, see serial I/O interface.
9. (S2) is a write only register. Reading S2 will give value FFH.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 28)	V_{DD}		−0,8 to + 8	V
All input voltages	V_I		0,8 to V_{DD} + 0,8	V
D.C. current into any input or output	$\pm I_I, \pm I_O$	max.	10	mA
Total power dissipation (see note)	P_{tot}	max.	500	mW
Power dissipation per output				
except P23, SCLK	P_O	max.	50	mW
P23, SCLK	P_O	max.	180	mW
Storage temperature range	T_{stg}		−65 to + 150	°C
Operating ambient temperature range	T_{amb}		−25 to + 70	°C
Operating junction temperature	T_j	max.	125	°C

Note

Thermal resistance (junction to ambient)				
for SOT-117	$R_{th\ j\text{-}a}$	max.	120	K/W
for SOT-135A	$R_{th\ j\text{-}a}$	max.	60	K/W
for SOT-136A	$R_{th\ j\text{-}a}$	max.	150	K/W

DEVELOPMENT DATA

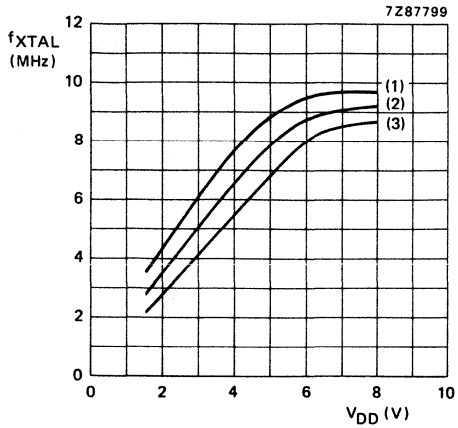
D.C. CHARACTERISTICS

V_{DD} = 2,75 to 6 V; V_{SS} = 0 V; T_{amb} = −25 to + 70 °C; all voltages with respect to V_{SS}; f = 3,58 MHz with R_S = 50 Ω; unless otherwise specified.

parameter	symbol	min.	typ.	max.	unit
Supply voltage					
operating (see Fig. 23)	V_{DD}	1,8	–	6	V
STOP mode for RAM retention	V_{DD}	1,0	–	6	V
Supply current					
operating					
at V_{DD} = 3 V (see Fig. 24)	I_{DD}	–	600	–	μA
IDLE mode					
at V_{DD} = 3 V (see Fig. 25)	I_{DD}	–	300	–	μA
STOP mode (see Fig. 26 and note 1)					
at V_{DD} = 1,8 V; T_{amb} = 25 °C	I_{DD}	–	1,2	2,5	μA
at V_{DD} = 1,8 V; T_{amb} = 55 °C	I_{DD}	–	–	5	μA
at V_{DD} = 1,8 V; T_{amb} = 70 °C	I_{DD}	–	–	10	μA
RESET I/O					
Switching level	V_{RESET}	–	1,3	–	V
Sink current					
at $V_{DD} > V_{RESET}$	I_{OL}	–	7	–	μA
Inputs					
Input voltage LOW	V_{IL}	0	–	$0{,}3V_{DD}$	V
Input voltage HIGH	V_{IH}	$0{,}7V_{DD}$	–	V_{DD}	V
Input leakage current					
at $V_{SS} < V_I < V_{DD}$	$\pm I_{IL}$	–	–	1	μA
Outputs					
Output voltage LOW					
at $V_I = V_{SS}$ or V_{DD}; $\lvert I_O \rvert < 1$ μA	V_{OL}	–	–	0,05	V
Output sink current LOW					
at V_{DD} = 3 V; V_O = 0,4 V					
except P23/SDA, SCLK (see Fig. 27)	I_{OL}	0,75	1,5	–	mA
P23/SDA, SCLK (see Fig. 28)	I_{OL}	1,5	–	–	mA
Pull-up output source current HIGH (see Fig. 29)					
at V_{DD} = 3 V; $V_O = 0{,}9V_{DD}$	$-I_{OH}$	25	–	–	μA
at V_{DD} = 3 V; $V_O = V_{SS}$	$-I_{OH}$	–	–	200	μA
Push-pull output source current HIGH					
at V_{DD} = 3 V; $V_O = V_{DD}$−0,4 V	$-I_{OH}$	0,75	1,5	–	mA

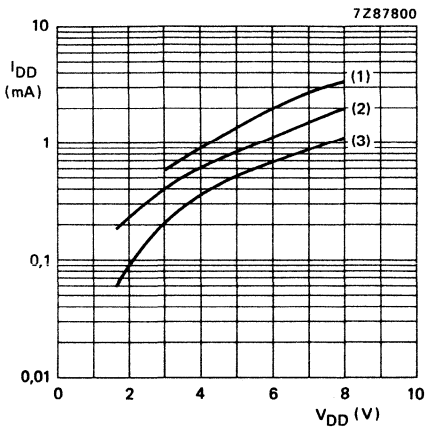
Note 1

Crystal connected between XTAL 1 and XTAL 2; SCL and SDA pulled to V_{DD} via 5,6 kΩ resistor; CE and T1 at V_{SS}.



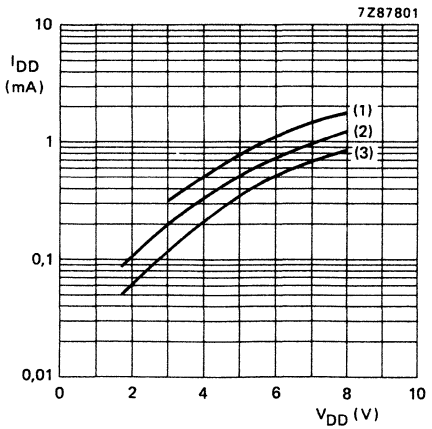
(1) T_{amb} = −25 °C
(2) T_{amb} = 25 °C
(3) T_{amb} = 70 °C

Fig. 23 Maximum clock frequency (f_{XTAL}) as a function of the supply voltage (V_{DD}).



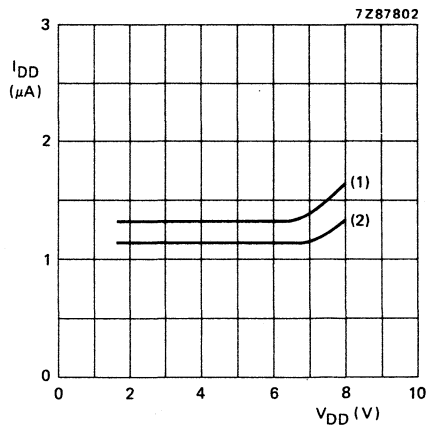
(1) clock frequency = 4 MHz
(2) clock frequency = 2 MHz
(3) clock frequency = 500 kHz

Fig. 24 Typical supply current (I_{DD}) in operating mode as a function of the supply voltage (V_{DD}); T_{amb} = 25 °C.



(1) clock frequency = 4 MHz
(2) clock frequency = 2 MHz
(3) clock frequency = 500 kHz

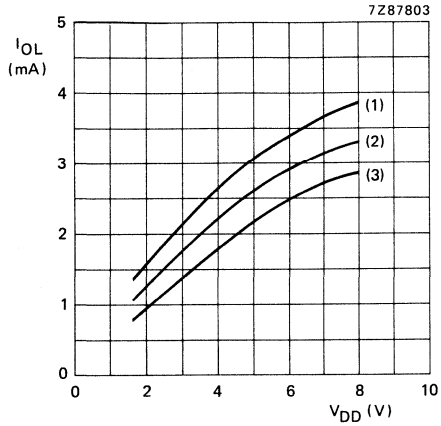
Fig. 25 Typical supply current (I_{DD}) in IDLE mode as a function of the supply voltage (V_{DD}); T_{amb} = 25 °C.



(1) T_{amb} = 70 °C
(2) T_{amb} = 25 °C

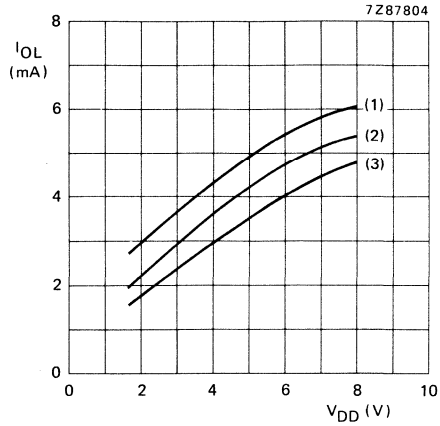
Fig. 26 Typical supply current (I_{DD}) in STOP mode as a function of the supply voltage (V_{DD}).

DEVELOPMENT DATA



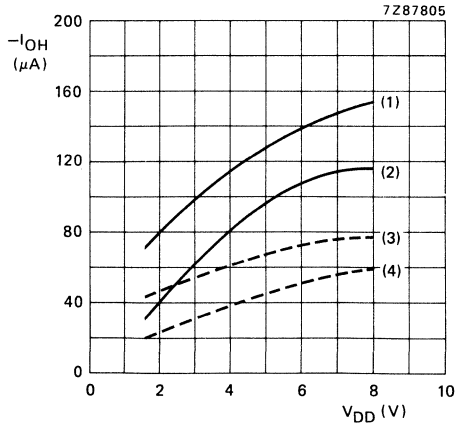
(1) $T_{amb} = -25\ ^{o}C$
(2) $T_{amb} = 25\ ^{o}C$
(3) $T_{amb} = 70\ ^{o}C$

Fig. 27 Output sink current LOW (I_{OL}), except outputs P23/SDA and SCLK, as a function of supply voltage (V_{DD}); V_O = 0,4 V.



(1) $T_{amb} = -25\ ^{o}C$
(2) $T_{amb} = +25\ ^{o}C$
(3) $T_{amb} = +70\ ^{o}C$

Fig. 28 Output current LOW (I_{OL}), outputs P23/SDA and SCLK, as a function of supply voltage (V_{DD}); V_O = 0,4 V.



(1) $T_{amb} = 25\ ^{o}C$; $V_O = V_{SS}$
(2) $T_{amb} = 25\ ^{o}C$; $V_O = 0{,}9V_{DD}$
(3) $T_{amb} = 70\ ^{o}C$; $V_O = V_{SS}$
(4) $T_{amb} = 70\ ^{o}C$; $V_O = 0{,}9V_{DD}$

Fig. 29 Output source current HIGH ($-I_{OH}$) as a function of supply voltage (V_{DD}).

A.C. CHARACTERISTICS

Rise and fall times between 10 and 90% levels; C_L = 50 pF

parameter	symbol	at 70 °C max. value			unit
	V_{DD}	1,8	3,0	6,0	V
Fall time	t_f	200	100	70	ns
Rise time	t_r	200	100	80	ns

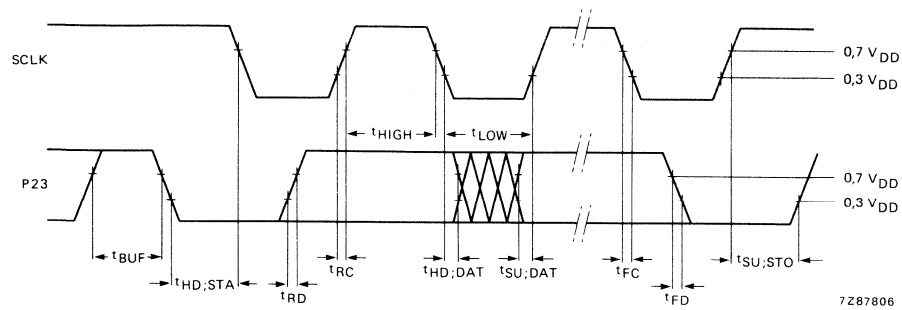


Fig. 30 PCD3343 timing requirements for the P23 and SCLK *input* signals.

Table 9 Input timing shown in figure 30

symbol	timing
t_{BUF}	$\geqslant 14t_{XTAL}$
$t_{HD;STA}$	$\geqslant 14t_{XTAL}$
t_{HIGH}	$\geqslant 17t_{XTAL}$
t_{LOW}	$\geqslant 17t_{XTAL}$
$t_{SY;STO}$	$\geqslant 14t_{XTAL}$
$t_{HD;DAT}$	> 0
$t_{SU;DAT}$	$\geqslant 250$ ns
t_{RD}	$\leqslant 1\ \mu s$
t_{RC}	$\leqslant 1\ \mu s$
t_{FD}	$\leqslant 1\ \mu s$
t_{FC}	$\leqslant 0{,}3\ \mu s$

Notes to Table 9

t_{XTAL} = one period of the XTAL input frequency (f_{XTAL})
= 280 ns for f_{XTAL} = 3,58 MHz.
These figures apply to all modes.

DEVELOPMENT DATA

A.C. CHARACTERISTICS (continued)

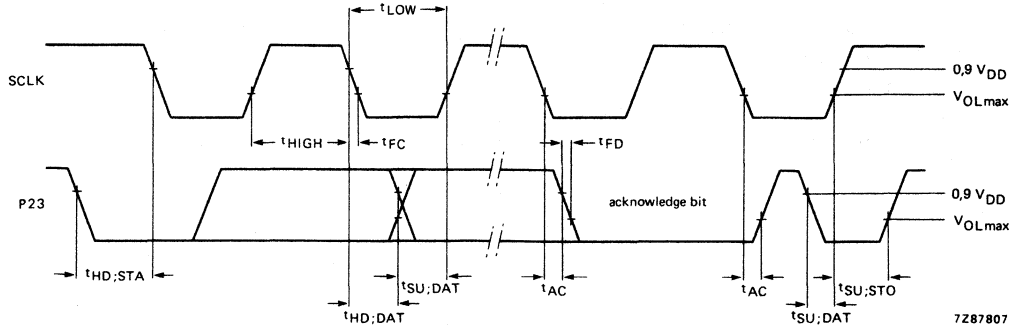


Fig. 31 PCD3343 timing requirements for the P23 and SCLK *output* signals.

Table 10 Output timing shown in figure 31

symbol	timing	
	normal mode (ASC in S2 = 0)	low-speed mode (ASC in S2 = 1)
$t_{HD;STA}$	½ (DF + 9) t_{XTAL}	¾ (DF + 9) t_{XTAL}
t_{HIGH}	½ (DF) t_{XTAL}	¾ (DF) t_{XTAL}
t_{LOW}	½ (DF) t_{XTAL}	¼ (DF) t_{XTAL}
$t_{SU;STO}$	½ (DF − 3) t_{XTAL}	¼ (DF − 3) t_{XTAL}
$t_{HD;DAT}$ (slave transmitter)		
any DF	$\geqslant 9t_{XTAL}$ $\leqslant 12t_{XTAL}$	$\geqslant 9t_{XTAL}$ $\leqslant 12t_{XTAL}$
$t_{HD;DAT}$ (master transmitter)		
for DF $\leqslant$ 51	$\geqslant 9t_{XTAL}$ $\leqslant 12t_{XTAL}$	– –
for DF $\leqslant$ 99	– –	$\geqslant 9t_{XTAL}$ $\leqslant 12t_{XTAL}$
$t_{SU;DAT}$ (master transmitter)		
for DF > 51	$\geqslant 15t_{XTAL}$ $\leqslant 24t_{XTAL}$	– –
for DF > 99	–	$\geqslant 15t_{XTAL}$ $\leqslant 24t_{XTAL}$
for DF $\leqslant$ 51	$\geqslant 9t_{XTAL}$	$\geqslant 9t_{XTAL}$
for DF $\leqslant$ 99	–	$\geqslant 9t_{XTAL}$
t_{AC}	$\geqslant 9t_{XTAL}$ $\leqslant 12t_{XTAL}$	$\geqslant 9t_{XTAL}$ $\leqslant 12t_{XTAL}$
t_{FD}, t_{FC}	$\leqslant$ 100 ns at C_b = 400 pF	$\leqslant$ 100 ns at C_b = 400 pF

Notes to Table 10

t_{XTAL} = one period of the XTAL input frequency (f_{XTAL})
= 280 ns for f_{XTAL} = 3,58 MHz.
DF = divisor (see Table 2 Serial I/O section).
C_b = the maximum bus capacitance for each line.

DEVELOPMENT DATA

APPLICATION INFORMATION

A block diagram of an electronic featurephone built around the PCD3343 is shown in figure 32. It comprises the following dedicated telephony IC's:

- TEA1060/1061 — transmission circuit for telephony
- PCD3312 — DTMF generator with Serial I/O
- PCE2111 or PCF8577 — 2 LCD drivers in LCD module MB7020160
- PCD8571 — 1 K RAM's with Serial I/O; the number of RAM's depends on the required amount of stored telephone numbers
- PCD3360/3361 — programmable multi-tone ringer

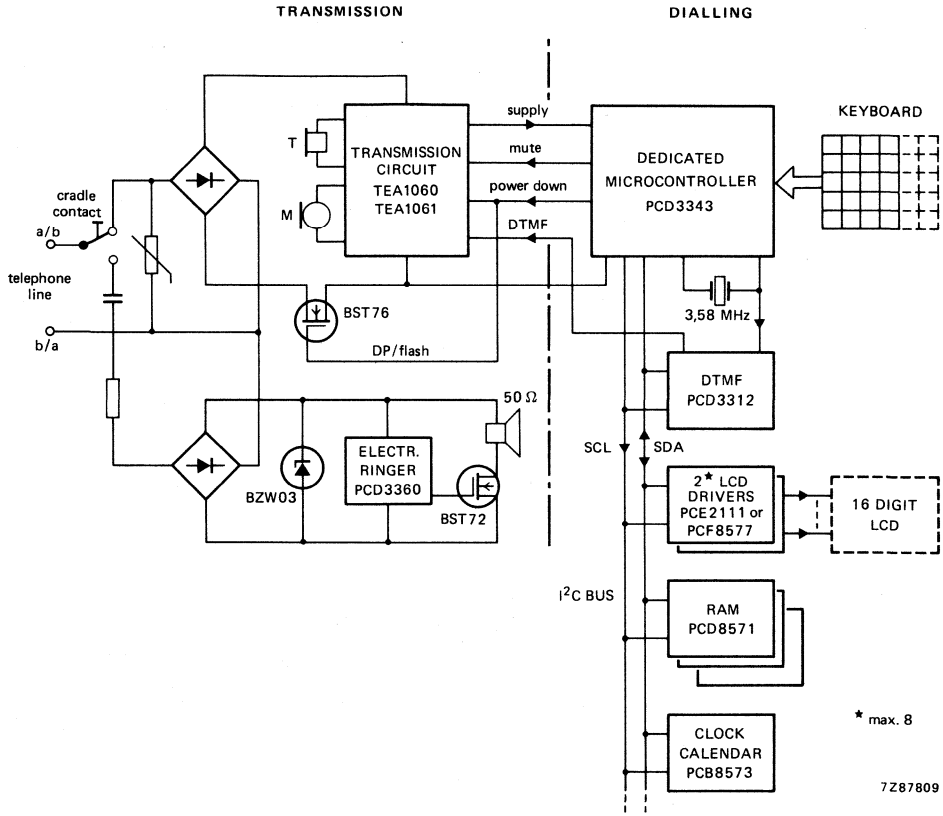


Fig. 32 Block diagram of electronic featurephone with common line interface.

A detailed application diagram of the PCD3343 with PCD3312 (DTMF), two PCD8571 (RAM) and two PCE2111 (LCD display drivers) is shown in figure 33.

Row 5 of the keyboard contains the following special keys:

- P — program and autodial
- FL — flash or register recall
- R — redial or extended redial
- AP — access pause

Row 6 contains the different diode options.

Columns 5 and 6 contain the button keys M0 to M9; single name keys for repertory telephone numbers.

APPLICATION INFORMATION (continued)

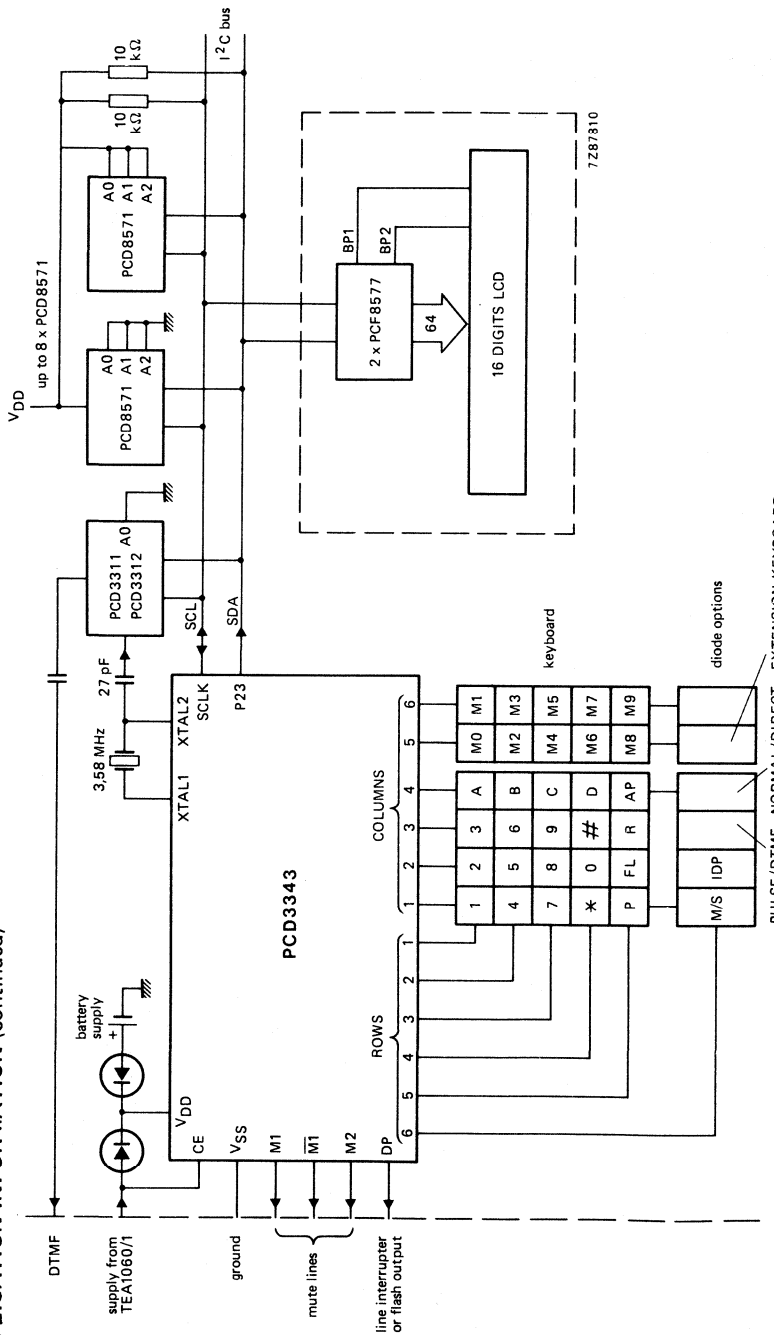


Fig. 33 Application diagram of PCD3343 for electronic featurephone with associated keyboard.

Additional information is available on request for the following:

- Serial I/O
- I²C bus specification
- Interrupt logic
- Instruction set descriptions
- Software routines for an intelligent telephone set

SINGLE-CHIP 8-BIT MICROCONTROLLER

DESCRIPTION

An advanced CMOS process is used to manufacture the PCF84CXX family of microcontrollers. The family consists of the following devices:

- PCF84C00 – 256 x 8 RAM, external program memory
- PCF84C21 – 2 K x 8 ROM, 64 x 8 RAM
- PCF84C41 – 4 K x 8 ROM, 128 x 8 RAM
- PCF84C81 – 8 K x 8 ROM, 256 x 8 RAM

Each version has 20 quasi-bidirectional I/O port lines, a serial I/O interface, a single-level vectored interrupt structure, an 8-bit timer/event counter and on-chip clock oscillator and clock circuits.

Each member of this microcontroller family is an efficient controller as well as an arithmetic processor. The instruction set is similar to that of the MAB8048 and the PCF84CXX family is pin- and instruction set compatible with the MAB8400 family.
The microcontrollers have facilities for both binary and BCD arithmetic plus bit-handling capabilities.

For detailed information see the user manual "Single-chip 8-bit microcontrollers".

Features

- 8-bit CPU, ROM, RAM, I/O in a single 28-lead DIL or SO package
- 2 K, 4 K or 8 K x 8 ROM; also a ROM-less version
- 64, 128 or 256 x 8 RAM
- 20 quasi-bidirectional I/O port lines
- Two test inputs: one of which is also the external interrupt input
- Single-level vectored interrupts: external, timer/event counter, serial I/O
- I^2C hardware interface for serial data transfer on two lines (serial I/O data via an existing port line and clock via a dedicated line)
- 8-bit programmable timer/event counter
- Clock frequency range: 100 kHz to 10 MHz
- Over 80 instructions (similar to those of the MAB8048) all of 1 or 2 cycles
- Single supply voltage (2,5 V to 5,5 V)
- STOP and IDLE modes
- Power-on-reset circuit
- Operating temperature range: −40 to +85 °C
- High current output on Port 1: I_{OL} = 10 mA at V_{OL} = 1,2 V (all versions except the PCF84C00)

PACKAGE OUTLINES

PCF84C21/41/81P : 28-lead DIL; plastic (SOT-117).
PCF84C21/41/81T : 28-lead mini-pack; plastic (SO-28; SOT-136A).
PCF84C00B : 28-lead 'piggy-back' package (with up to 28-pin EPROM on top).
PCF84C00T : 56-lead mini-pack; plastic (VSO-56; SOT-190).

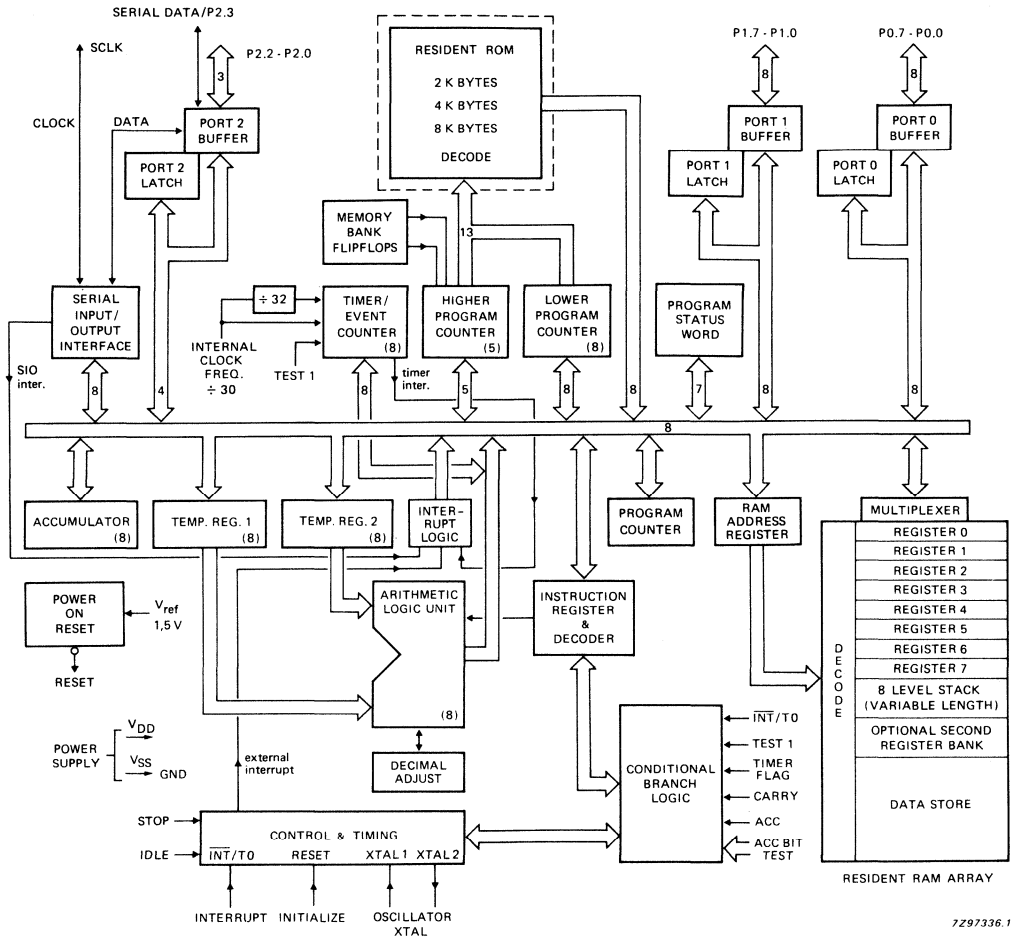


Fig. 1 PCF84CXX block diagram.

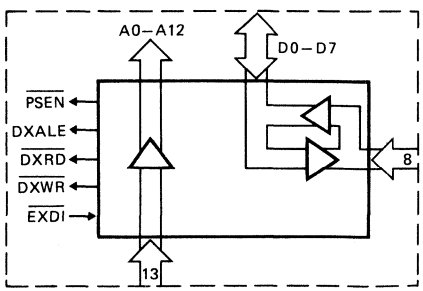


Fig. 1a Replacement of dotted section in Fig. 1, for the PCF84C00T ROM-less version.

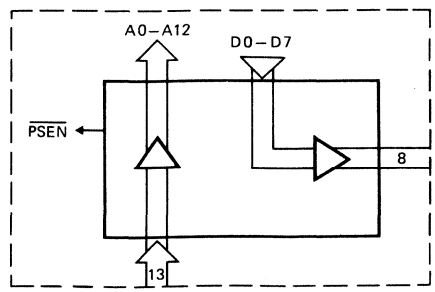


Fig. 1b Replacement of dotted section in Fig. 1, for the PCF84C00B 'piggy-back' version.

DEVELOPMENT DATA

PINNING

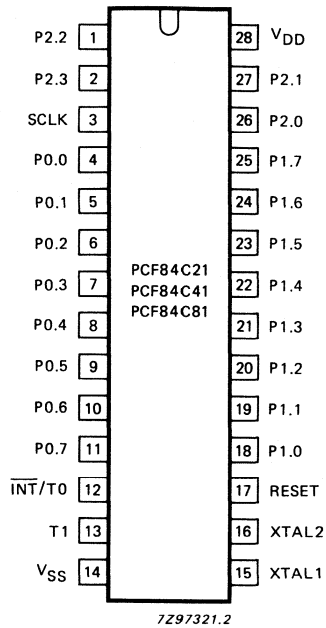


Fig. 2 Pin designation of the PCF84C21/41/81.

PIN FUNCTION

Pin	*Symbol*	*Type*	*Function*
3	SCLK	I/O	**Clock:** bidirectional clock for serial I/O.
4-11	P0.0-P0.7	I/O	**Port 0:** 8-bit quasi-bidirectional I/O port.
12	$\overline{\text{INT}}$/T0	I	**Interrupt/Test 0:** external interrupt input (negative edge triggered)/ test input pin; when used as a test input, this pin is directly tested by conditional branch instructions JT0 and JNT0.
13	T1	I	**Test 1:** test input pin, directly tested by conditional branch instructions JT1 and JNT1. T1 may also be selected as an input to the 8-bit timer/event counter via the STRT CNT instruction.
14	V_{SS}	I	**Ground:** circuit earth potential.
15	XTAL 1	I	**Oscillator input:** input from a crystal which determines the internal oscillator frequency or an external clock generator.
16	XTAL 2	I/O	**Oscillator output:** output of the inverting amplifier.
17	RESET	I/O	**Reset input:** used to initialize the microcontroller (active HIGH); also output of power-on-reset circuit.
18-25	P1.0-P1.7	I/O	**Port 1:** 8-bit quasi-bidirectional I/O port.
26, 27, 1, 2	P2.0-P2.3	I/O	**Port 2:** 4-bit quasi-bidirectional I/O port. P2.3 is the serial data input/output in serial I/O mode.
28	V_{DD}	I	**Power supply:** 2,5 V to 5,5 V.

PINNING (continued)

Pin diagram of the PCF84C00B 'piggy-back' version

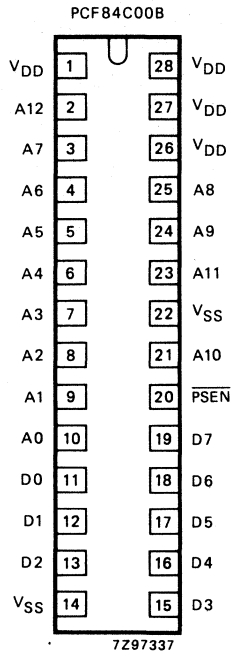


Fig. 3(a) Pinning diagram (top pins) of the PCF84C00B 'piggy-back' version.

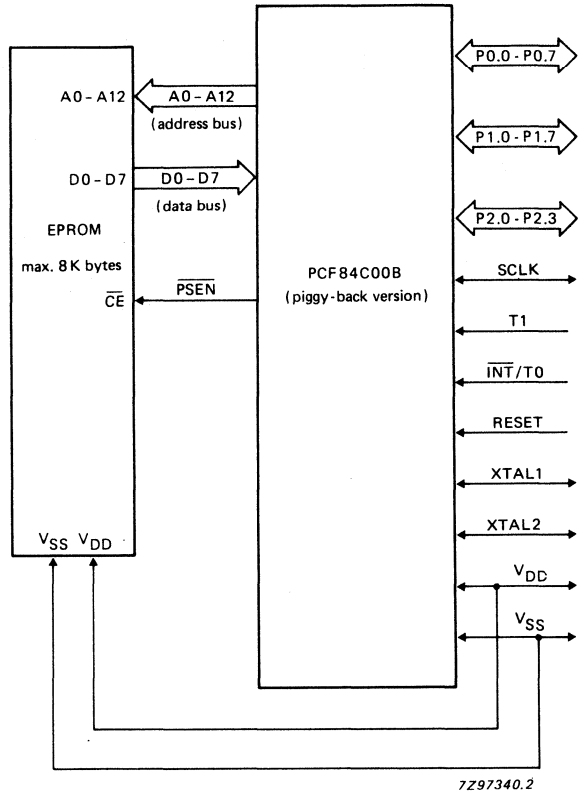


Fig. 3(b) Connection of EPROM to the PCF84C00B 'piggy-back' version.

The PCF84C00B is mainly used for prototyping and for low production volume applications. This device is packaged in a 'piggy-back' package. i.e. a 4 K or 8 K byte EPROM (2732 or 2764) may be mounted in the 24/28 pin socket on top of the package.

Notes

1. RAM capacity of PCF84C00B is 256 bytes.
2. Access time for ROMS/EPROMS must be less than 7 x $1/f_{XTAL}$.
3. Bottom pinning is identical to that of Fig. 2.

DEVELOPMENT DATA

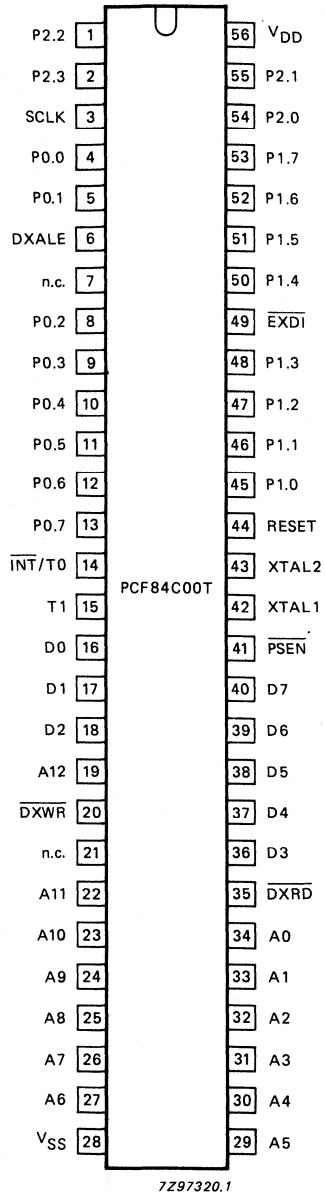


Fig. 4 Pinning diagram; ROM-less version PCF84C00T.

The PCF84C00T may be used for prototyping future derivatives of the PCF84CXX family or for low production volume applications. This device is packaged in a 56-lead VSO outline. Additional signals are available (see pinning information following) to control external program memory and derivative functions.

PIN FUNCTION (continued)

Pin	*Symbol*	*Type*	*Function*
34-29, 27-22,19	A00-A12	O	**Address bus.** For external memory and peripherals.
16-18, 36-40	D0-D7	I/O	**Data bus.** For external memory and peripherals. The specified STOP mode supply current is valid only if external pull-ups are connected to all data lines.
41	$\overline{\text{PSEN}}$	O	**Program store enable** (active LOW). $\overline{\text{PSEN}}$ is for enabling external program memory and is active during TS9 and TS10 of each machine cycle and TS1 of each following cycle. $\overline{\text{PSEN}}$ is HIGH during the STOP mode.
6	DXALE	O	**Address latch enable.** Using the falling edge, the Dx address can be latched in an appropriate external latch. This signal occurs only during execution of the MOV Dx,A, MOV A,Dx, ANL Dx,A and ORL Dx,A instructions (x = 0 to FF H).
35	$\overline{\text{DXRD}}$	O	**Read strobe** (active LOW). When this signal is active, external registers emulating Dx registers can be gated to the data bus of the PCF84C00. This signal occurs only during execution of MOV A,Dx, ANL Dx,A and ORL Dx,A instructions (x = 0 to FF H).
20	$\overline{\text{DXWR}}$	O	**Write strobe** (active LOW). On the rising edge, data on D0-D7 can be latched in appropriate external registers emulating Dx. This signal occurs only during execution of MOV Dx,A, ANL Dx,A and ORL Dx,A instructions (x = 0 to FF H).
49	$\overline{\text{EXDI}}$	I	**External derivative interrupt** (active LOW). $\overline{\text{EXDI}}$ is 'OR-ed' with the internal serial interrupt and can be used to initiate an interrupt from external hardware emulating derivative functions. An internal pull-up is provided. A derivative interrupt is internally polled during time slot TS6*, and is only accepted if an EN SI instruction has been executed and the device is not already executing an interrupt routine. Derivative interrupts are not latched in the PCF84C00.

* The interrupt signal must remain active until the vector address (05 H) is present on the address bus.

FUNCTIONAL DESCRIPTION

ROM-less version PCF84C00T

The PCF84C00T microcontroller contains no on-board ROM, but has all address and data lines brought-out to access an external ROM or EPROM. This version has more pins than the PCF84CXX with on-board ROM (see Fig. 1a). The PCF84C00T can address up to 8 K of external program memory, and has 256 bytes of internal data RAM.

'Piggy-back' version PCF84C00B

The PCF84C00B is a special package that has standard pinning to the bottom which facilitates insertion as a mask-programmed device. An EPROM can be mounted on top in an additional socket. The total package height is greater than the standard DIL package. The PCF84C00B can address up to 8 K of external ROM/RAM, and has 256 bytes of internal data RAM.

Program memory

The program memory consists of 2, 4 or 8 K bytes of read-only memory (ROM). Each location is directly addressable by the program counter. The ROM is mask-programmed at the factory. Figure 5 shows the program memory map.

Four program memory locations are of special importance:

- Location 0: contains the first instruction to be executed after the microcontroller is initialized (RESET)
- Location 3: contains the first byte of an external interrupt service routine
- Location 5: contains the first byte of a serial I/O and derivative interrupt service routine
- Location 7: contains the first byte of a timer/event counter interrupt service routine

Program memory is arranged in banks of 2 K bytes, which are selected by SEL MB instructions. The program memory is further divided into location 'pages', each of 256 bytes. This latter division applies only for conditional branches. Memory bank boundaries can be crossed only by using unconditional branch instructions after the appropriate memory bank has been selected. A CALL instruction can transfer control to a subroutine on any 'page'; RET and RETR instructions can transfer control from a subroutine back to the main program.

Data memory

Data memory consists of 64, 128 or 256 bytes of random-access memory (RAM). All locations are indirectly addressable using RAM pointer registers; up to 16 designated locations are directly addressable. Memory also includes an 8-level program counter stack addressed by a 3-bit stack pointer. Figure 6 shows the data memory map.

Working registers

Locations 0 to 7 are designated as working registers, directly addressable by the direct register instructions. Ease of addressing, and a minimum requirement of instruction bytes to manipulate their contents, makes these locations suitable for storing frequently addressed intermediate results. This bank of registers can be selected by the SEL RB0 instruction.

Executing the select register bank instruction SEL RB1, designates locations 24 to 31 as working registers, instead of locations 0 to 7, and these are then directly addressable. This second bank of working registers may be used as an extension of the first or reserved for use during interrupt service routines saving the first bank for use in the main program. If the second bank is not used, locations 24 to 31 may serve as general purpose RAM.

The first two locations of each bank contain the RAM pointer registers R0, R1, R0' and R1', which indirectly address all RAM locations.

All RAM locations make efficient program loop counters when used with the decrement register and test instruction DJNZ.

FUNCTIONAL DESCRIPTION (continued)

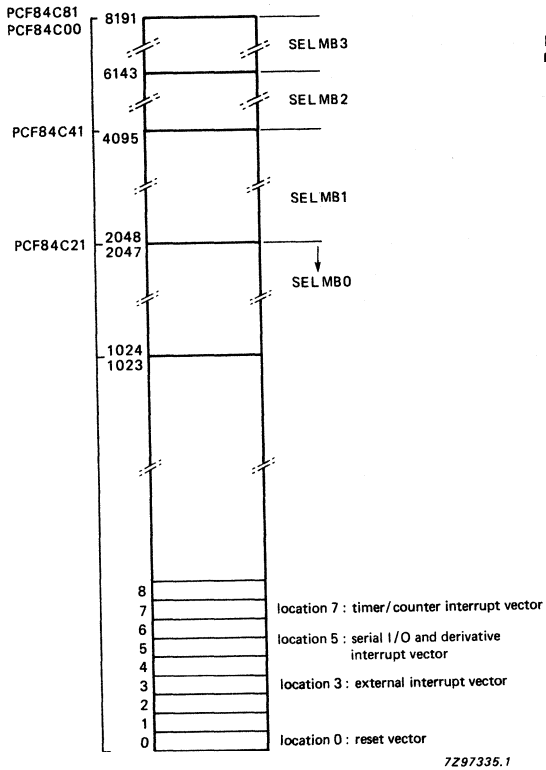


Fig. 5 Program memory map.

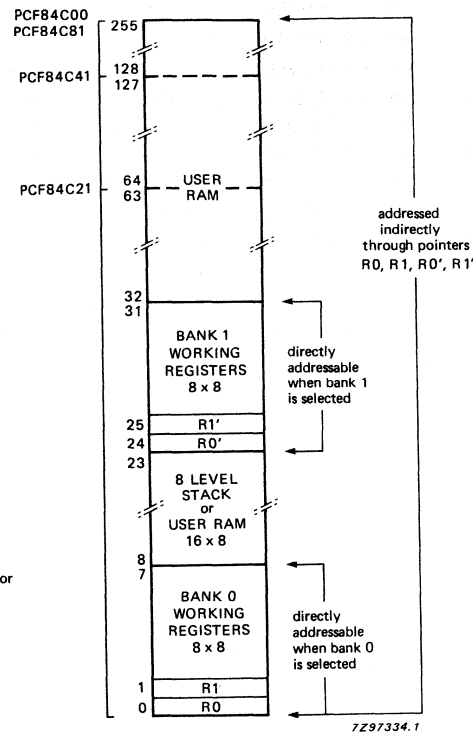


Fig. 6 Data memory map.

Program counter stack

Locations 8 to 23 may be designated as an 8-level prógram counter stack (2 locations per level), or as general purpose RAM. The program counter stack (Fig. 7) enables the microcontroller to keep track of the return addresses and status prior to interrupts or CALL instructions by storing the contents of the program counter before servicing the subroutine. A 3-bit stack pointer determines which of the eight register pairs of the program counter stack will be loaded with the next return address and status.

The stack pointer, when initialized to 000 by RESET, points to RAM locations 8 and 9. On the first subroutine CALL or interrupt, the contents of the program counter and bits 4, 6 and 7 of the program status word (PSW) are transferred to locations 8 and 9. The stack pointer increments by one and points to locations 10 and 11 ready, for another CALL. Because an address may be up to 13 bits long, two bytes must be used to store each address.

At the end of a subroutine, which is signalled by a return instruction (RET or RETR), the stack pointer decrements by one and the contents of the register pair on top of the stack are transferred to the program counter. The saved PSW bits are transferred to the PSW only by the RETR instruction.

If all 8 levels of subroutine and interrupt nesting are not used, the unused portion of the stack may be used as any other indirectly addressable RAM locations.

Nesting of subroutines within subroutines can continue up to 8 times without overflowing the stack. If overflow does occur the deepest address stored (locations 8 and 9) will be overwritten and lost since the stack pointer overflows from 111 to 000. It also underflows from 000 to 111.

FUNCTIONAL DESCRIPTION (continued)

The value of the saved contents of the program counter during an interrupt CALL is not the same as the value saved during a normal CALL to subroutine. During an interrupt CALL, the program counter return address is saved; during a subroutine CALL, the saved program counter value is one less than the program counter return address.

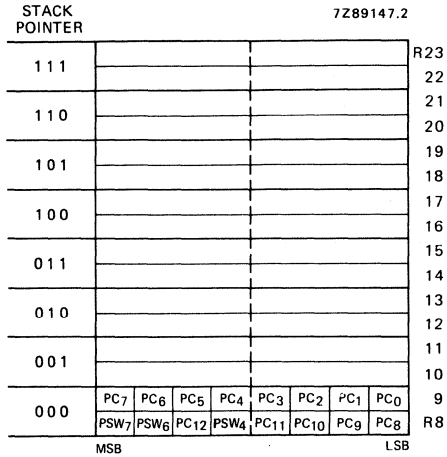


Fig. 7 Program counter stack.

IDLE and STOP modes

IDLE mode

When the microcontroller enters the IDLE mode via the IDLE instruction (01 H), the oscillator, timer/counter and serial I/O are kept running. The microcontroller exits from the IDLE mode via a RESET or one of three interrupts if they are enabled. If the interrupt is not enabled, the microcontroller will remain in the IDLE mode. An active signal on the RESET pin restarts the microcontroller and a normal RESET sequence is executed (see Fig. 8).

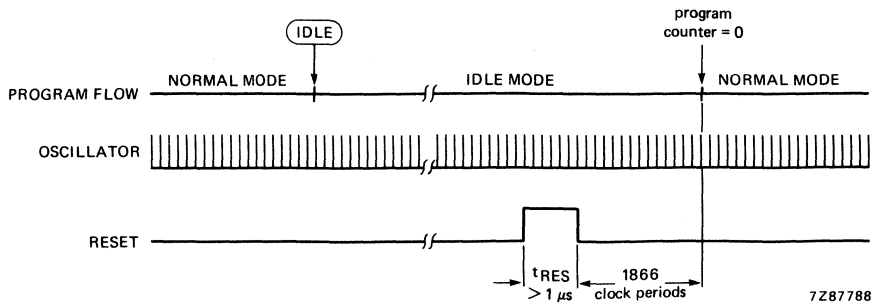


Fig. 8 Exit from IDLE mode via a RESET.

An active signal coming from an enabled interrupt causes the execution of the normal interrupt routine since normal interrupt scanning is still being carried out. A HIGH-to-LOW transition on the external interrupt pin ($\overline{INT}$/T0) reactivates the microcontroller. A LOW level applied to $\overline{INT}$/T0 will reactivate the microcontroller only in the STOP mode. Thus, if $\overline{INT}$/T0 was LOW before the microcontroller entered the IDLE mode, it must go HIGH before the microcontroller can be reactivated (see Fig. 9).

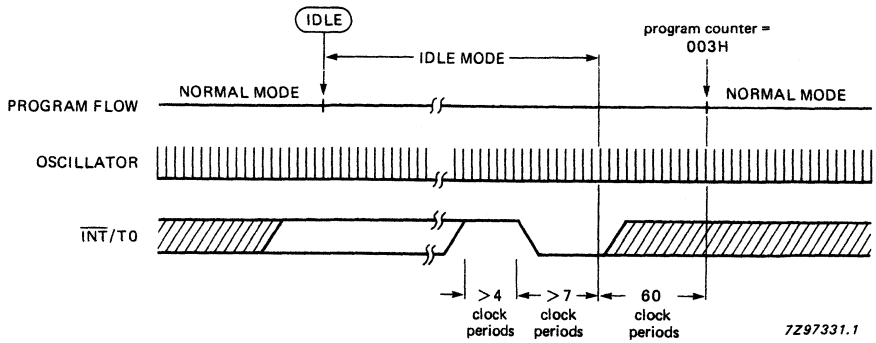


Fig. 9 Exit from IDLE mode via an interrupt.

Wake-up from the IDLE mode is ensured when $\overline{INT}$/T0 is HIGH for at least 4 CP (clock periods) and then LOW for 7 CP. After the initial forced CALL 003 H operation (60 CP) the program continues with the external interrupt service routine. During IDLE mode operation, the address of the instruction immediately following the instruction that caused the microcontroller to enter the IDLE mode is present on the address bus.

STOP mode

The microcontroller enters the STOP mode via the STOP instruction (22 H). The oscillator is switched off and the internal status of the CPU, RAM contents and the state of I/O ports are not affected. The microcontroller can be brought out of the STOP mode by an active signal at the external interrupt input or by an external RESET signal. When one of these two signals is applied, an internal delay of 1866 CP is provided to ensure that all internal clocks are operating correctly before restart (see Fig. 10).

Note: the start-up time of a crystal oscillator is measured in milliseconds, and the 1866 CP count begins after this start-up time.

If the microcontroller exits from the STOP mode via a RESET, a normal RESET sequence is executed.

FUNCTIONAL DESCRIPTION (continued)

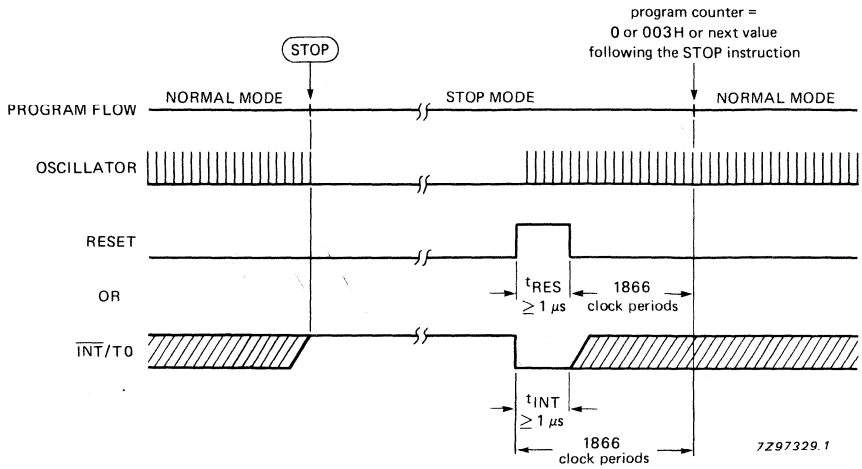


Fig. 10 Entering and exiting the STOP mode.

If the microcontroller is brought out of the STOP mode by pulling the external interrupt input pin LOW, an interrupt sequence is executed only if the external interrupt is enabled. In this event the microcontroller resumes the normal program sequence after returning from the interrupt routine, as in the normal mode. If the interrupt is not enabled, it continues the normal program sequence by executing the first instruction following the STOP instruction.

The microcontroller is restarted by a LOW level applied at the $\overline{INT}$/T0 pin, and not by a HIGH-to-LOW transition as in the normal interrupt mechanism.
Note: when exiting the STOP mode via an interrupt, a further instruction in the main program series is executed before the interrupt routine is entered.

If the $\overline{INT}$/T0 input is active (LOW) during the STOP instruction, no STOP is executed.

A LOW level on the external interrupt input of at least 1 µs will cause the microcontroller to exit the STOP mode. During the STOP mode, the address of the instruction immediately following the instruction that caused the microcontroller to enter the STOP mode is present on the address bus.

I/O facilities

The PCF84CXX family has 23 I/O lines arranged as:

- Port 0 8-bit parallel port (P0.0-P0.7)
- Port 1 8-bit parallel port (P1.0-P1.7)
- Port 2 4-bit parallel port (P2.0-P2.3)
- SCLK serial I/O clock line
- $\overline{INT}$/T0 external interrupt and test input. When used as a test input, it can be directly tested by conditional branch instructions JT0 and JNT0
- T1 test input which can alter program sequences when tested by conditional jump instructions JT1 and JNT1. T1 also functions as an input to the 8-bit timer/event counter

Parallel ports

All parallel port lines can be individually configured as outputs or inputs; their structure is quasi-bidirectional.
Output data written to a port is latched and remains unchanged until rewritten.
Input data is not latched and must be present until read by an input instruction.

Input lines are fully CMOS compatible; output lines can drive one TTL or CMOS load.

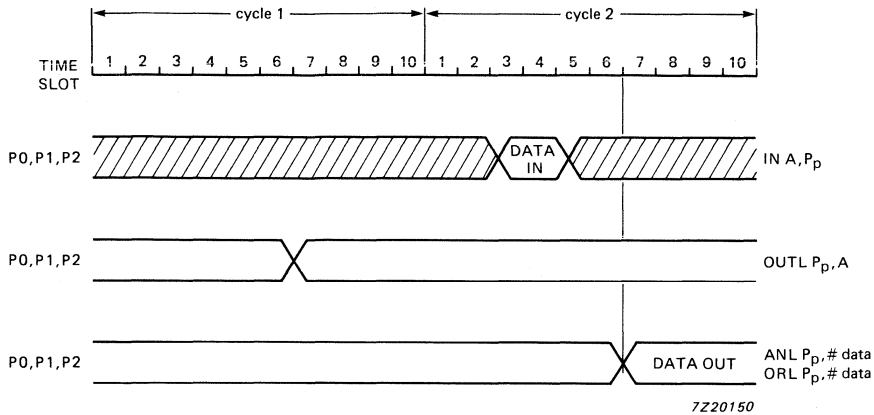


Fig. 11 Timing diagram for all ports using IN, OUTL, ANL and ORL instructions.

Figure 11 shows the timing diagram for all ports using IN, OUTL, ANL and ORL instructions. For the OUTL instruction data changes on time slot 7 of cycle 1. For the MOV, ANL and ORL instructions, the ports change on time slot 7 of cycle 2.

Figure 12 shows the quasi-bidirectional I/O interface with push-pull output and switched pull-up current source.

Each line is pulled up to V_{DD} via a constant current source (TR4), which is enabled via TR3 whenever one of the two output latches contains a logic 1. This current source is sufficient for a TTL HIGH level, yet can be pulled LOW by an external CMOS device, thus allowing the same pin to be used for both input and output.

When a logic 1 is written to a port line for the first time (MQ = 1, SQ = 0), TR2 is switched on for the duration of the internal write pulse (one oscillator period), to provide a fast transition from logic 0 to logic 1. Subsequent writing of a logic 1 to a port line will not switch TR2 on. This ensures that the port lines can be pulled LOW when configured as inputs.

When a logic 0 is written to a port line, TR3 switches off the current source. Current sinking capability is provided by TR1, which is now switched on. When used as an input, a logic 1 must first be written to the port line; otherwise TR1 will remain low impedance.

FUNCTIONAL DESCRIPTION (continued)

PCF84CXX mask options make it possible for 19 of the 20 port pins to be individually configured as one of the following. The PCF84C00 is available with Standard Ports only:

1. STANDARD PORT: quasi-bidirectional I/O with switched pull-up current source of 100 μA (typ.) and P-channel booster transistor TR2. TR2 is only active during 1 clock cycle (Fig. 12).
2. OPEN DRAIN: quasi-bidirectional I/O with only an N-channel open drain output. Application as an output requires connection of an external pull-up resistor (Fig. 13).
3. PUSH-PULL OUTPUT: with V_{DD} = 5 V, the output can sink and source 1,6 mA (min.). To avoid a large current flowing through the output transistors, these push-pull pins must only be used as outputs (Fig. 14).

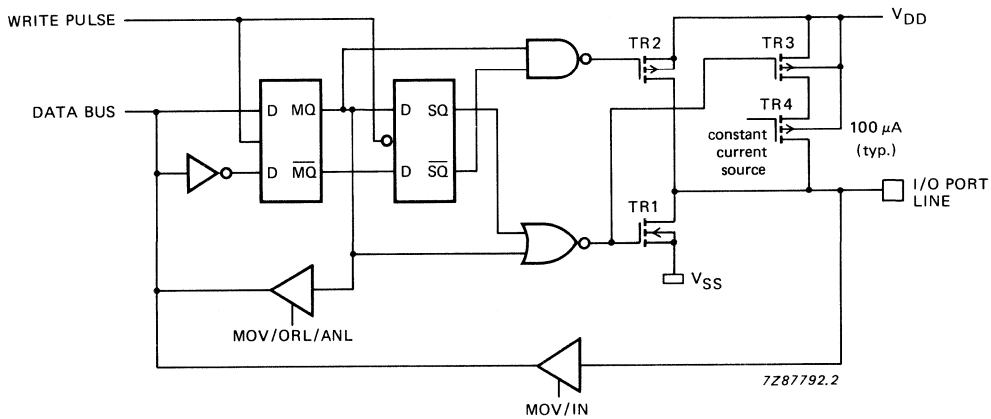


Fig. 12 Standard output with switched pull-up current source.

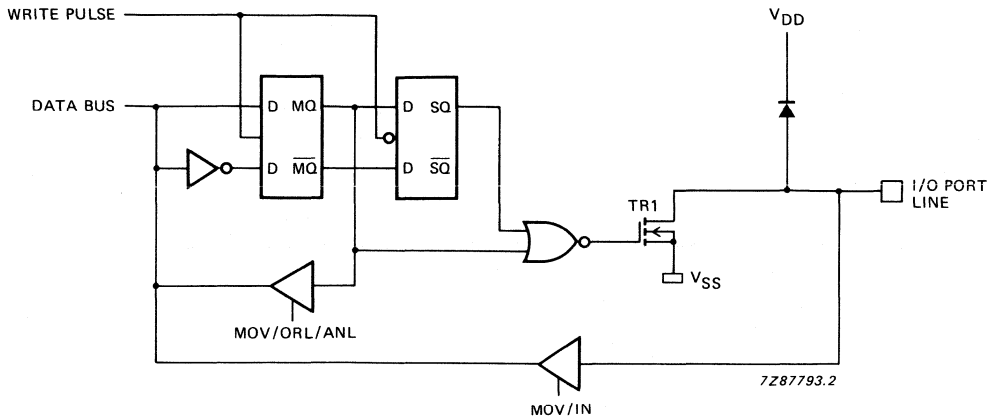


Fig. 13 Open drain output.

DEVELOPMENT DATA

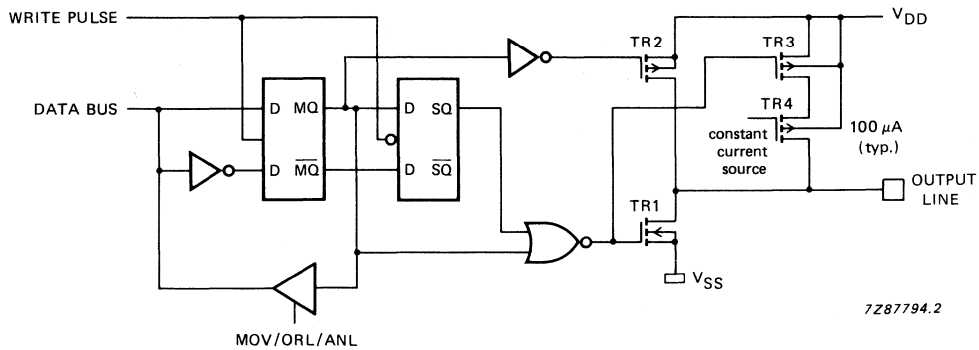


Fig. 14 Push-pull output.

FUNCTIONAL DESCRIPTION (continued)

Serial I/O (SIO)

The PCF84CXX has an on-chip serial I/O interface that supports the I^2C-bus. Whereas a normal microcontroller must regularly monitor the serial data bus for the presence of data, the serial I/O interface detects, receives and converts the serial data stream into parallel format without interrupting the execution of the current program. An interrupt is sent to the PCF84CXX only when a complete byte is received. It then reads the data byte in one instruction.

The design of the PCF84CXX serial I/O system allows any number of devices from the PCF8500 family (clips) to be connected via the two-line serial bus. The ability of any devices to communicate, without interrupting the operation of any other devices on the bus, is an outstanding attribute of the system. This is achieved by allocating a specific 7-bit address to each device and providing a system whereby a device reacts only to a message prefixed with its own address or the 'general CALL' address. Address recognition is performed by the interface hardware so that operation of the microcontroller need only be interrupted when a valid address had been received. This saves significant processing time and memory space compared with a conventional microcontroller employing a software serial interface. When the addressing facility is not required, for instance in a system with only two microcontrollers, direct data transfer without addressing can be performed. In multi-master systems, an automatically invoked arbitration procedure prevents two or more devices from continuing simultaneous transmission.

In NORMAL (running) and IDLE mode, the serial I/O logic remains active; its internal system clock will be switched off when there is no activity on the serial bus.

After execution of the STOP instruction, the oscillator of the PCF84CXX is switched off. This means that the serial I/O logic will remain in the state it was in when the STOP mode was entered. To avoid "bus block" problems and to assure correct start-up of the bus after exit from the STOP mode, the user should disable the serial logic (ESO = 0) prior to the execution of the STOP instruction.

Serial I/O interface

Figure 15 shows a block diagram of the serial I/O interface. The clock line of the serial bus has exclusive use of pin 3 (SCLK) while the data line shares pin 2 (serial data) with the I/O line P2.3 of Port 2. When the serial I/O is enabled, P2.3 is disabled as a parallel port line; (P2.3 and SCLK are open drain).

The microcontroller and interface communicate via the internal microcontroller bus and the Serial Interrupt Request line. Data and information controlling the operation of the interface are stored in four registers:

- Data shift register (S0)
- Serial I/O interface status word (S1)
- Serial clock control word (S2)
- Address register

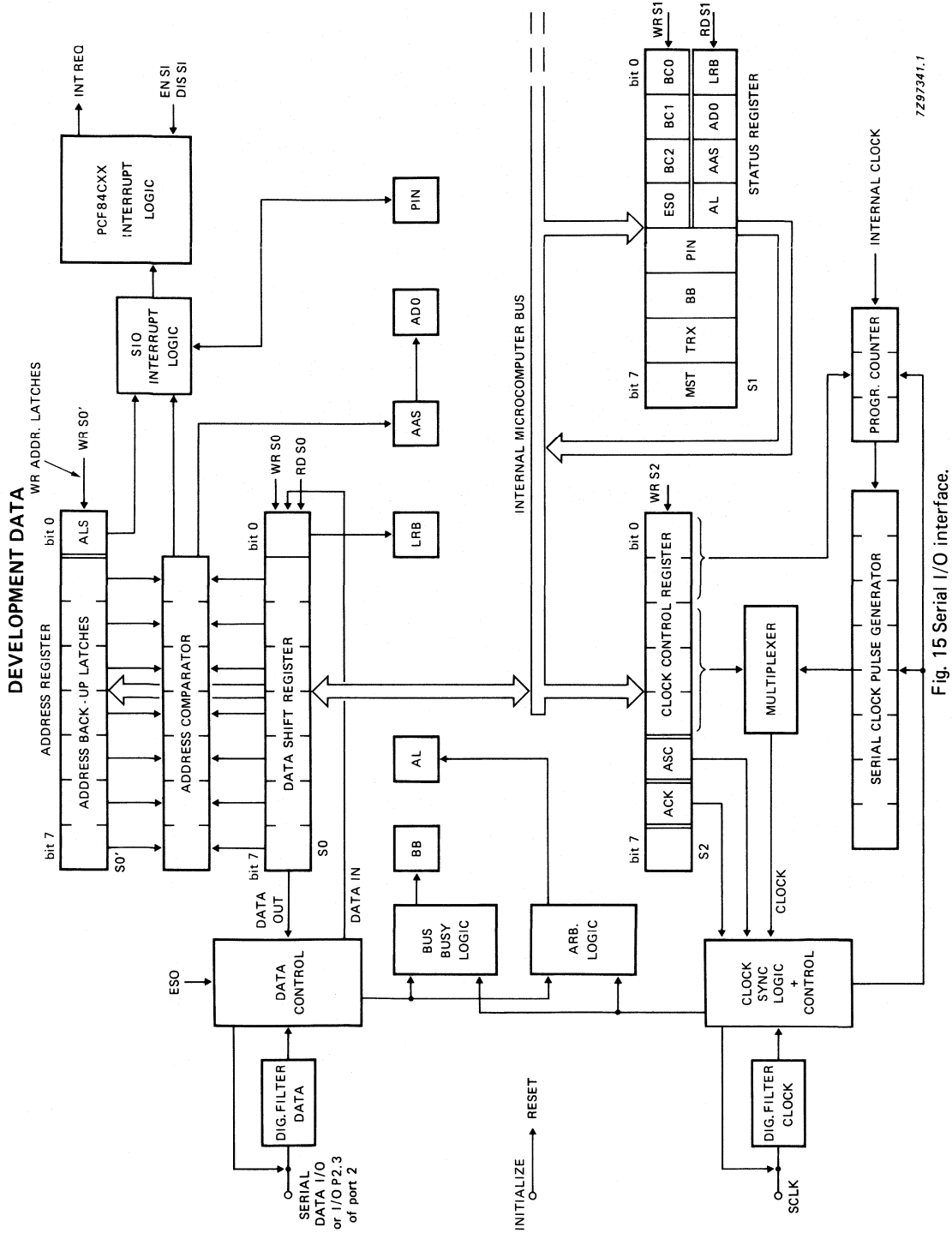


Fig. 15 Serial I/O interface.

FUNCTIONAL DESCRIPTION (continued)

Data shift register (S0)

Register S0 converts serial data to parallel format and vice versa. An interrupt is generated only after a complete byte has been transmitted, or after a complete data byte, specific address or 'general CALL' address has been received. The most significant bit is transmitted first.

Serial I/O interface status word (S1)

Register S1 provides information concerning the state of the interface and stores information from the microcontroller. Bits 0 to 3 are duplicated: control bits in these positions can only be written by the microcontroller, while interface bits can only be read.

MST and TRX (see Table 1)

These bits determine the operating mode of the serial I/O interface.

Table 1 Operating modes of the serial I/O interface

MST	TRX	operating mode
0	0	slave receiver
1	0	master receiver
0	1	slave transmitter
1	1	master transmitter

BB: Bus Busy.

This flag indicates the status of the bus.

PIN: Pending Interrupt Not

PIN = '0' indicates the presence of a pending interrupt, which will cause a Serial Interrupt Request when the serial interrupt mechanism is enabled.

ESO: Enable Serial output

The ESO flag enables/disables the serial I/O interface: ESO = '1' enables, ESO = '0' disables. ESO can only be written by software.

BC0, BC1 and BC2

Bits BC0, BC1 and BC2 indicate the number of bits received or transmitted in a data stream. These bits can only be written by software.

AL: Arbitration Lost

The arbitration lost flag is set by hardware when the serial I/O interface, as master transmitter, loses a bus arbitration procedure.

AAS: Addressed As Slave

This flag is set by hardware when the interface detects either its own specific address or the 'general CALL' address as the first byte of a transfer and the interface has been programmed to operate in the address recognition mode.

AD0: Address Zero

This flag is set by hardware after detection of the 'general CALL' address when the interface is operating in the address recognition mode.

LRB: Last Received Bit

This contains either the last data bit received or, for a transmitting device in the acknowledgement mode, the acknowledgement signal from the receiving device.

Bits AL, AAS, AD0 and LRB can only be read by software.

Serial clock control word (S2)

Bits 0 to 4 of the clock register S2 determine the frequency of the serial clock signal. When a 6 MHz crystal is used, the frequency of the serial clock can be varied between 1 kHz and 154 kHz (see Table 2). An asymmetrical clock with a HIGH-to-LOW ratio of 3 : 1 can be generated using bit 5. The asymmetrical clock allows a microcontroller more time per clock period for sampling the data line, making the timing of this action less critical. Bit 6 can be used to activate the acknowledge mode of the serial I/O. S2 is a write only register.

Address register

The address register contains the 7-bit address back-up latches and the bit (ALS) used to enable/disable the address recognition mode. The address register can be written using the MOV S0, A and MOV S0, # data instructions, but only when ESO = logic 0.

Serial I/O interrupt logic

An EN SI instruction enables and a DIS SI instruction disables the interrupt logic. When the logic is enabled, a pending interrupt results in a serial I/O interrupt to the processor, causing a CALL to location 5 in the ROM. When disabled, the presence of an interrupt is still indicated by PIN in S1, allowing the interrupt to be serviced. However, vectored interrupt will not occur.

FUNCTIONAL DESCRIPTION (continued)

Table 2 SIO clock pulse frequency control when using a 6 MHz and a 10 MHz crystal

hexadecimal S20-S24 code	f_{OSC} divided by	f_{OSC} = 6 MHz f_{SCLK} (kHz)**	f_{OSC} = 10 MHz f_{SCLK} (kHz)**
0	not allowed		
1	39	*154	*256
2	45	*133	*222
3	51	*118	*196
4	63	95	*159
5	75	80	*133
6	87	69	*115
7	99	61	*101
8	123	49	81
9	147	41	68
A	171	35	58
B	195	31	51
C	243	25	41
D	291	21	34
E	339	18	29
F	387	16	26
10	483	12	21
11	579	10	17
12	675	8,9	15
13	771	7,8	13,4
14	963	6,2	10,4
15	1155	5,2	8,7
16	1347	4,5	7,4
17	1539	3,9	6,5
18	1923	3,1	5,2
19	2307	2,6	4,3
1A	2691	2,2	3,7
1B	3075	2,0	3,3
1C	3843	1,6	2,6
1D	4611	1,3	2,2
1E	5379	1,1	1,9
1F	6147	1,0	1,6

* Not permitted for I^2C operation.

** The maximum clock frequency in the I^2C systems is 100 kHz.

Interrupts (see Fig. 16(a) and Fig. 16(b))

When an interrupt routine is entered, the contents of the program counter and bits 4, 6 and 7 of the PSW are saved in the program counter stack. The contents of the accumulator can only be saved by user software. Interrupt acknowledgement can be carried out by software via I/O ports. All interrupt routines must reside in memory bank 0; the SEL MB1, SEL MB2 and SEL MB3 instructions may not be used in an interrupt routine. An interrupt routine can only be terminated by the RETR (return and restore) instruction. During an interrupt routine, subroutine calls must be terminated by the RET instruction. Using the RETR instruction to terminate a subroutine called in an interrupt routine would terminate the interrupt routine prematurely and result in a wrong return address.

External Interrupts

When the external interrupt is enabled, a HIGH-to-LOW transition on the $\overline{\text{INT}}$/T0 input initiates the external interrupt routine and forces a CALL to program memory location 3. The program counter points to the external interrupt vector address (003 H) between 2,6 and 3,6 machine cycles after the transition occurs. Interrupt latency depends on the instruction that is being executed when the transition occurs. External interrupts are latched in the External Interrupt Flag (EIF) even when they are not enabled. Execution of a DIS I instruction clears previously latched interrupts, the digital filter latch and the external interrupt flag.

SIO Interrupt

When enabled, a serial I/O interrupt forces a CALL to program memory location 5. SIO interrupts are latched within the SIO hardware regardless of the SIO Interrupt Enable Flag and can only be cleared by setting the PIN bit of register S1, by accessing (read or write) register S0 or by a hardware RESET. There is no automatic reset of the SIO Interrupt Flag after the SIO interrupt routine is called and this flag must be cleared by software to avoid recurring interrupts.

Timer/Counter Interrupt

When the timer interrupt is enabled, a timer/counter overflow sets the Timer Interrupt Flag (TIF) and forces a CALL to program memory location 7. Timer interrupts are only latched when they are enabled. The timer flag is set every time the timer/counter overflows and is not automatically reset when the timer/counter interrupt routine is called. It can only be cleared by the JTF and JNTF instructions or by a hardware RESET.

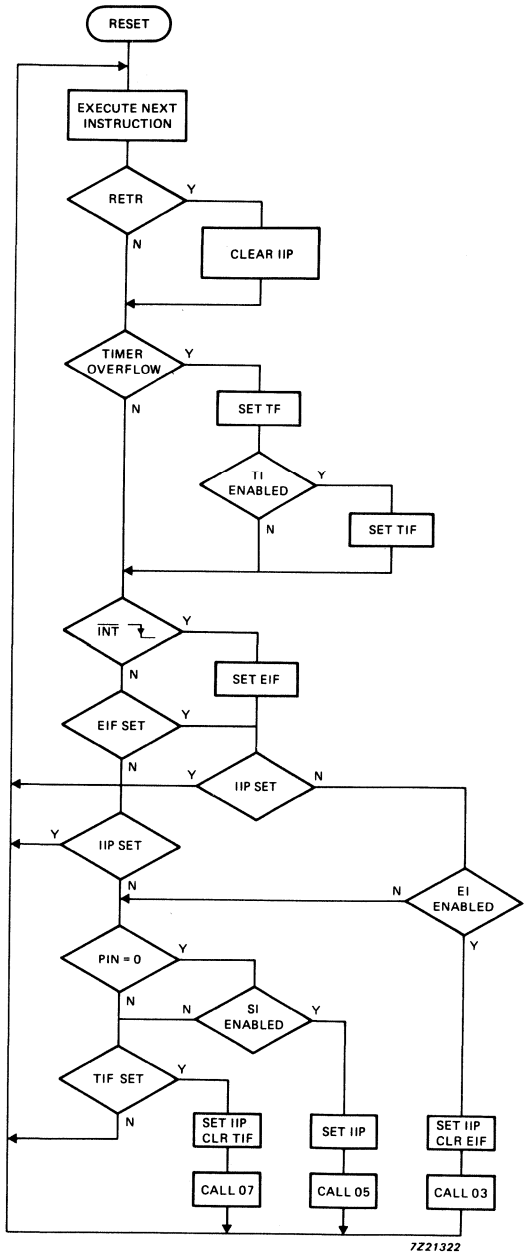
Interrupt Priority

If simultaneous interrupts occur, their priority is as follows:

- External (highest)
- SIO
- Timer/Counter (lowest)

An interrupt routine can only be interrupted by a hardware RESET and cannot be interrupted by other interrupts (which will be latched). When the interrupt routine is terminated by the RETR instruction, at least one instruction of the main program will be executed before another interrupt routine is entered.

FUNCTIONAL DESCRIPTION (continued)



EI	External Interrupt
SI	Serial Interrupt
TI	Timer/counter Interrupt
EIF	External Interrupt Flag
TF	Timer Flag
TIF	Timer Interrupt Flag
PIN	Pending Interrupt Not (SIO)
IIP	Interrupt In Progress flag

Fig. 16(a) Flow chart illustrating the interrupt handling sequence.

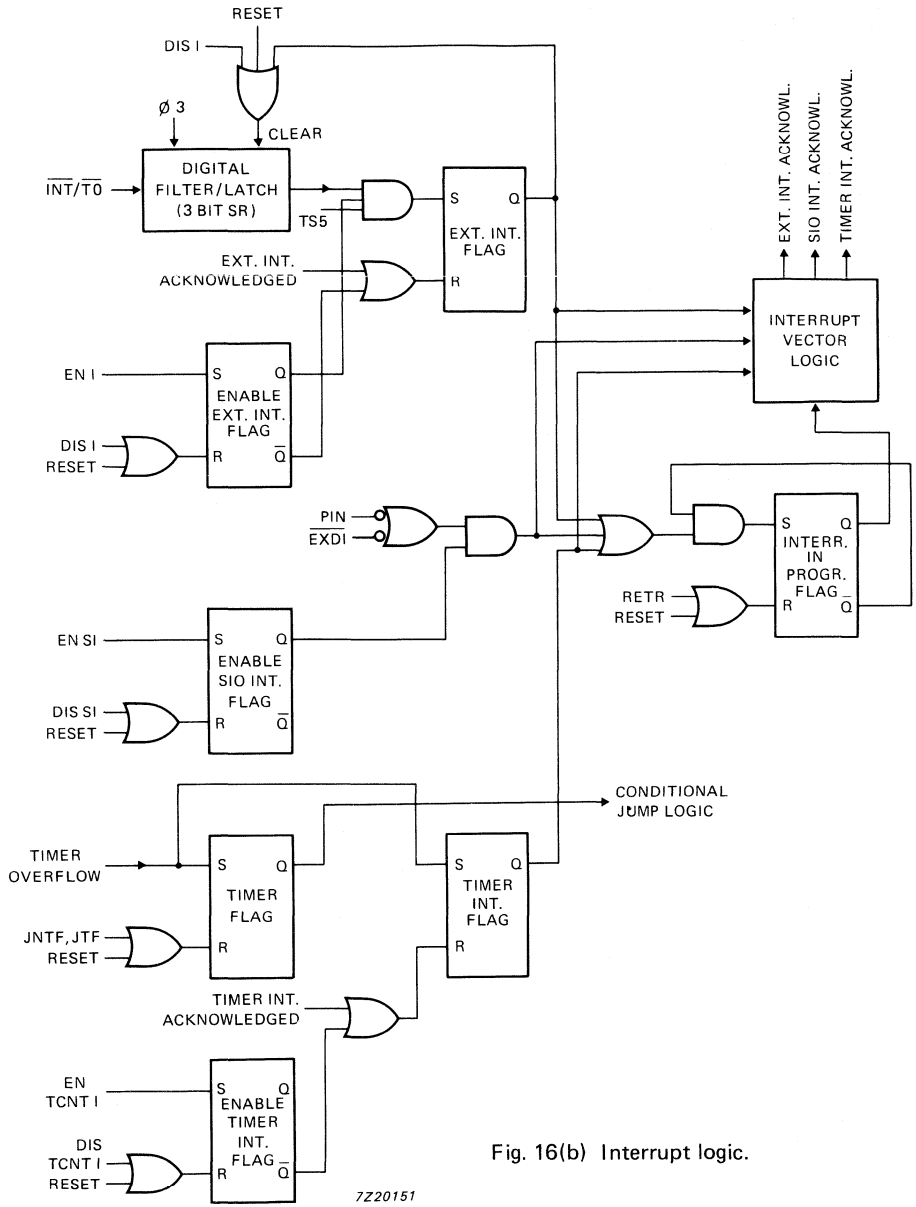


Fig. 16(b) Interrupt logic.

Notes to Figure 16

1. $\overline{INT}$/T0 negative edge is always latched in the digital filter/latch.
2. Correct interrupt timing is ensured when $\overline{INT}$/T0 is HIGH for $>$ 4 CP and then LOW for $>$ 7 CP.
3. When the interrupt in progress flag is set, further external and timer interrupts are latched but ignored, until RETR is executed.
4. A DIS I instruction always clears a pending external interrupt.
5. For all flip-flops, RESET overrules SET.
6. EXDI is an input of PCF84C00T, in other versions it is connected internally to a logic 1.

FUNCTIONAL DESCRIPTION (continued)

Oscillator (see Fig. 17)

The oscillator can be inhibited by the STOP instruction under software control. It is also inhibited when a low-supply voltage condition is present to prevent discharge of a weak back-up battery. Provided the supply voltage is within the operating range, the oscillator will be restarted after a STOP instruction by a LOW level at the $\overline{INT}$/T0 pin or a HIGH level at the RESET pin.

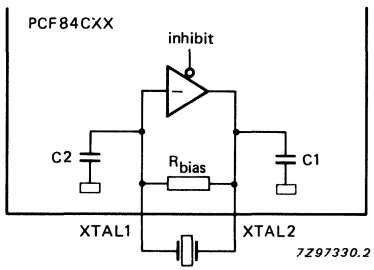


Fig. 17 Oscillator with integrated elements.

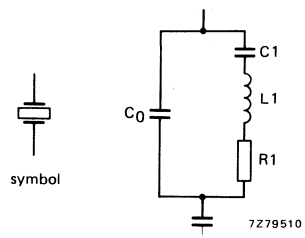


Fig. 18 Crystal unit equivalent circuit.

The values of crystal series resistance R1 and the crystal's total load capacitance C_L (C_O + wiring + external capacitors) must not be above the curve (Fig. 19) for the corresponding frequency.
Note: if external capacitors are connected to XTAL1 and XTAL2, they must be of equal value.

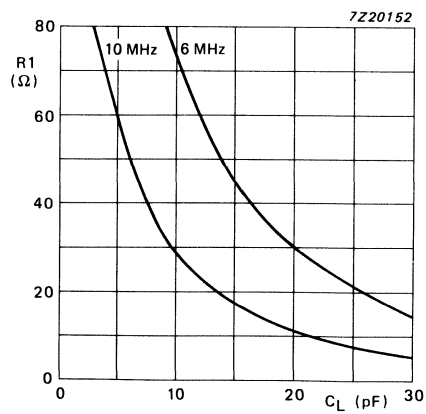


Fig. 19 Crystal circuit criteria.

XTAL2 is the output of the inverting amplifier. An external clock can be applied to XTAL1.
A machine cycle consists of 10 time slots; each time slot is 3 oscillator periods.

Timer/event counter (see Fig. 20)

An internal 8-bit up-counter is provided. This can count external events, modulo-32 machine cycles, or machine cycles directly. Table 3 shows the instructions that control the counter and the prescaler, and the functions performed.

When used as a timer, the input to the counter is either the overflow or input of a 5-bit prescaler. When used a an event counter, LOW-to-HIGH transitions on pin 13 (T1) are counted. The counter is incremented during a machine cycle only if the falling edge occurs during the first 7 time slots; otherwise it is incremented during the next cycle. The maximum rate at which the counter may be incremented is once every machine cycle. When the counter overflows, the timer flag is set. The flag can be tested and reset using the JTF (jump is timer flag = logic 1) or JNTF instruction. An overflow also generates an interrupt to the microcontroller by setting the Timer Interrupt Flag when the timer/event counter interrupt is enabled.

Table 3 Timer/event counter control

function	timer mode modulo-1, modulo-32*	counter mode
CLEAR	MOV T,A (A) = 0 or RESET	MOV T,A (A) = 0 or RESET
PRESET	MOV T,A	MOV T,A
START	STRT T	STRT CNT
STOP	STOP TCNT or RESET	STOP TCNT or RESET
TEST	JTF/JNTF	JTF/JNTF
READ**	MOV A,T	MOV A,T

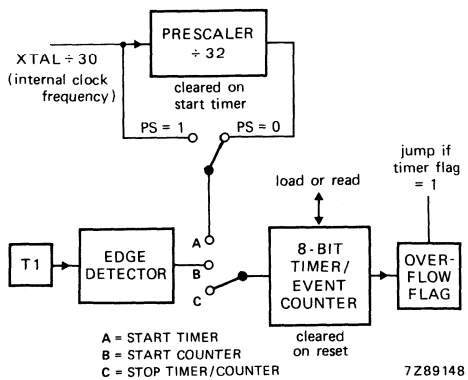


Fig. 20 Timer/event counter.

* With prescaler select, PS = logic 0, the timer counts modulo-32 machine cycles; with PS = logic 1, it counts modulo-1 cycles (prescaler not used); the prescaler is cleared by the STRT T instruction and is not readable.

** READ does not disturb the counting process.

FUNCTIONAL DESCRIPTION (continued)

Program status word (see Fig. 21)

The program status word (PSW) is an 8-bit word (1 byte) in the CPU which stores information about the current status of the microcontroller.
The PSW bits are:

- Bits 0 to 2 stack pointer bits (SP_0, SP_1, SP_2)
- Bit 3 prescaler select (PS);
  0 = modulo-32; 1 = modulo-1 (no prescaling)
- Bit 4 working register bank select (RBS);
  0 = register bank 0; 1 = register bank 1
- Bit 5 not used (1)
- Bit 6 auxiliary carry (AC); half-carry bit generated by an ADD instruction and used by the decimal adjust instruction DA A
- Bit 7 carry (CY); the carry flag indicates that the previous operation resulted in an overflow of the accumulator

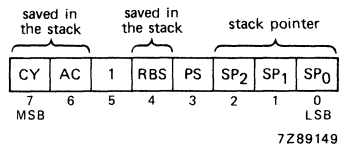


Fig. 21 Program status word.

All bits can be read using the MOV A, PSW instruction. Bits 7 and 6 are set and cleared by CPU operation. Bit 4 can be changed by the SEL RB instructions, bit 3 by the MOV PSW, A instruction, and bits 0, 1 and 2 by the CALL, RET or RETR instructions and in the event of an interrupt. Bits 7, 6 and 4 are stored in the program counter stack during subroutine and interrupt calls. These bits are restored in the PSW with a RETR (return and restore) instruction which must be used at the end of an interrupt service routine and can be used at the end of a normal subroutine. The RET instruction has no restore feature and cannot be used at the end of an interrupt service routine.

Program counter (see Fig. 22)

The 13-bit program counter is able to address 8 K bytes of ROM. The arrangement of the bits is shown in figure 22. During an interrupt routine PC_{11} and PC_{12} are forced to logic 0. All 13 bits are saved in the stack during CALL and interrupt routines.

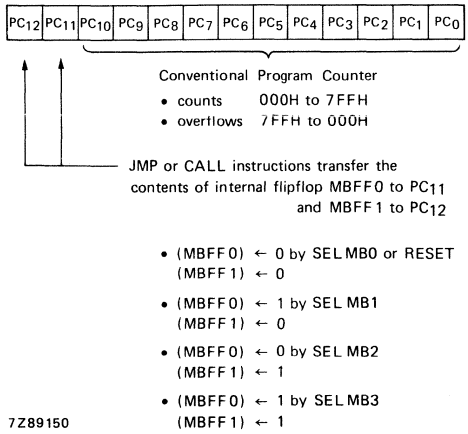


Fig. 22 Program counter.

Central processing unit

The PCF84CXX has arithmetic, logical and branching capabilities. The DA A, SWAP A and XCHD instructions simplify BCD arithmetic and the handling of nibbles. The MOVP A,@A instruction permits efficient table look-up from the current ROM page.

Conditional branch logic

The conditional branch logic within the microcontroller enables several conditions, internal and external to the microcontroller, to be tested by the user's program. Table 4 lists the conditional jump instructions used to change the program sequence. The DJNZ instruction decrements a designated register or data memory location and branches if the contents are not zero. This instruction is useful for looping control. The JMPP@A instruction allows multiway branches to destinations determined by the contents of the accumulator.

FUNCTIONAL DESCRIPTION (continued)

Table 4 Conditional branches

test	jump condition	jump instruction
accumulator	all bits zero	JZ
	any bit non-zero	JNZ
accumulator bit test	1	JB0 to JB7
carry flag	1	JC
	0	JNC
timer overflow flag	1	JTF
	0	JNTF
test input T0	1	JT0
	0	JNT0
test input T1	1	JT1
	0	JNT1
register	non-zero	DJNZ

Test input T1 (pin 13)

The T1 input line can be used as:

- A test input for branch instructions JT1 and JNT1
- An external input to the event counter

When used as a test input:

- JT1 instruction tests for logic 1 level
- JNT1 instruction tests for logic 0 level

When used as an input to the event counter, T1 must be LOW for $>$ 4 CP, and then HIGH for $>$ 4 CP. A transition can be recognized every 30 oscillator clock periods (1 machine cycle).

There is no internal pull-up or pull-down resistor connected to the T1 input. When T1 is not used, it must be tied to V_{DD} or V_{SS}.

Reset (pin 17)

A positive-going signal on the RESET input:

- Sets the program counter to zero
- Selects location 0 of memory bank 0 and register bank 0
- Sets the stack pointer to zero (000 points to RAM address 8)
- Disables the interrupts (external, timer and serial I/O)
- Stops the timer/event counter, then sets it to zero
- Sets the timer prescaler to modulo-32
- Resets the timer flag
- Sets all ports to input mode
- Sets the serial I/O to slave receiver mode and disables the serial I/O
- Cancels IDLE and STOP modes

Power-on-reset

The internal power-on-reset circuit monitors the PCF84CXX supply voltage V_{DD}. For as long as the supply voltage remains below the internal reference level V_{ref} (typically 1,5 V), the oscillator is inhibited and RESET has un undefined level. When V_{DD} rises above the internal reference level, the oscillator is released and RESET is pulled high to V_{DD} by TR1 for a period t_D (typically 50 μs).

Note: because of the narrow bandwidth of the crystal, the start-up time of the oscillator is typically 10 ms.

Three modes of power-on-reset are possible:

1. If V_{DD} can be switched with a fast rise time i.e. V_{DD} reaches its minimum operating value (corresponding to the selected oscillator frequency) before the RESET signal has finished (t_D), then no extra components are required (see Figs 23 and 24). Note that the first instruction is executed after the oscillator start-up time plus 1866 clock periods have elapsed.
2. If V_{DD} has a slow rise time then the RESET signal should be stretched by an external RC circuit (see Figs 25 and 26). In the event of a short drop in the supply voltage, the diode path rapidly discharges the capacitor to ensure a reliable power-on-reset. To ensure a correct reset, the RESET signal should reach at least 70% of the final value of V_{DD}. Given that the RESET voltage and V_{DD} rise exponentially, the above requirement is satisfied when the time constant τ of the RESET pulse is $>$ 8 times the time constant of V_{DD}. If V_{DD} rises linearly, then a RESET time constant $>$ 2 times the rise time of V_{DD} is required.

   When a reset is completed (RESET goes LOW) before the oscillator has started up, program execution begins after the oscillator start-up time plus 1866 clock periods have elapsed (see Fig. 26). If the oscillator is started up prior to the completion of RESET, then program execution begins 1866 clock periods after RESET goes LOW.
3. Figure 27 shows an external reset to the PCF84CXX during power-on. The external reset signal must remain HIGH until V_{DD} has reached its minimum operating value corresponding to the selected oscillator frequency. When a reset is completed (RESET goes LOW) before the oscillator has started up, program execution begins after the oscillator start-up time plus 1866 clock periods have elapsed (see Fig. 28). If the oscillator is started up prior to the completion of RESET, then program execution begins 1866 clock periods after RESET goes LOW.

FUNCTIONAL DESCRIPTION (continued)

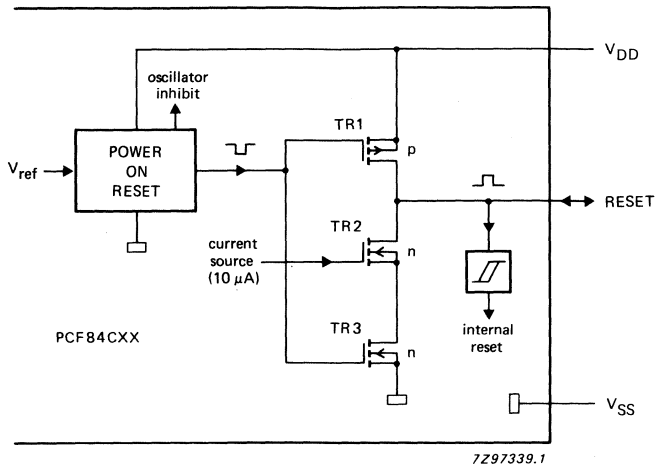


Fig. 23 Power-on-reset configuration.

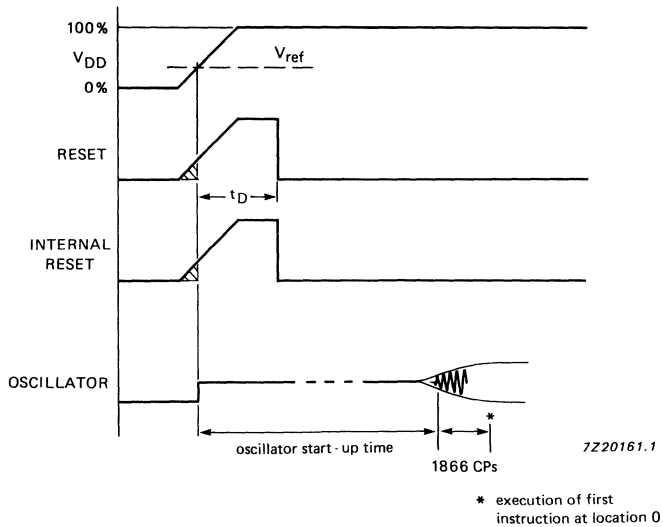


Fig. 24 Timing of power-on-reset with fast V_{DD} rise time.

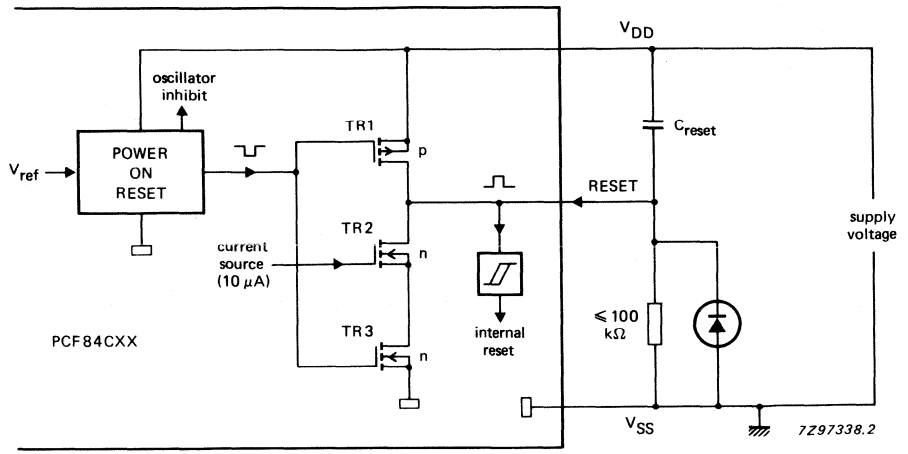


Fig. 25 Stretched power-on-reset with external components.

DEVELOPMENT DATA

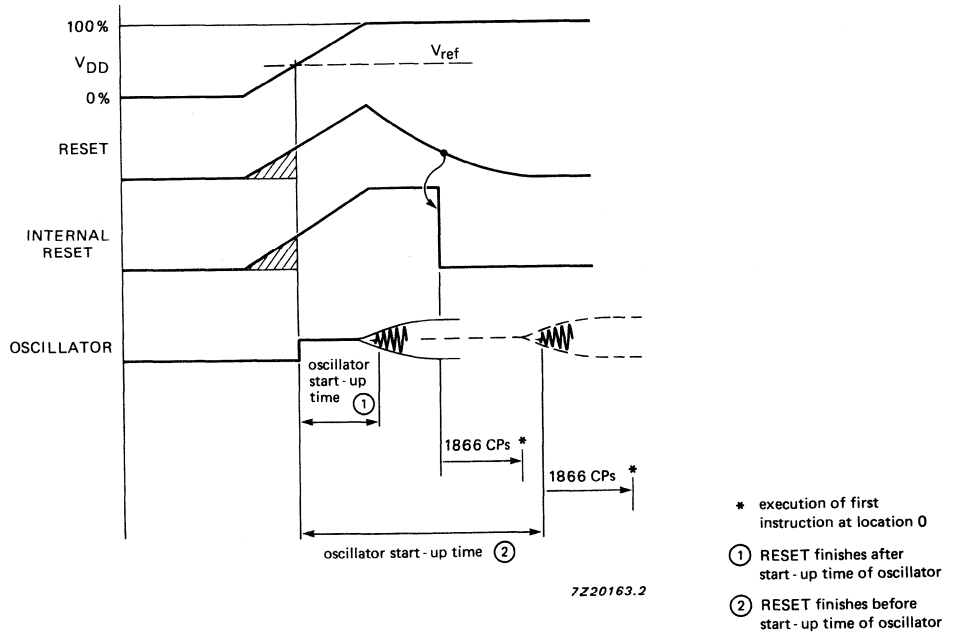


Fig. 26 Timing of power-on-reset with a slowly rising V_{DD} and a stretched RESET pulse.

FUNCTIONAL DESCRIPTION (continued)

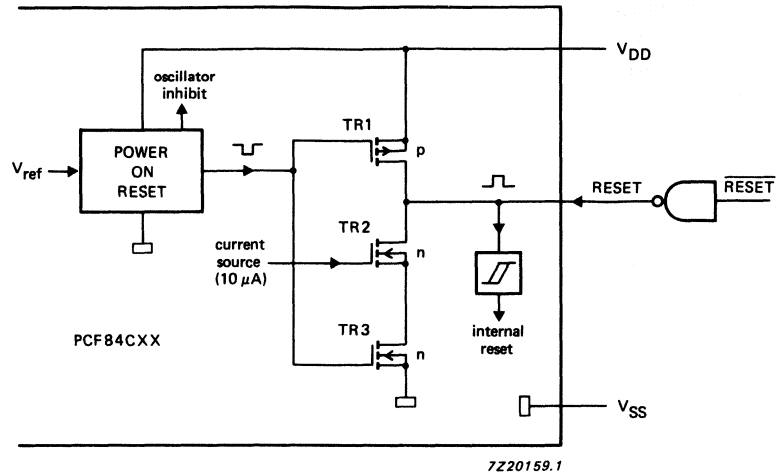


Fig. 27 External power-on-reset configuration.

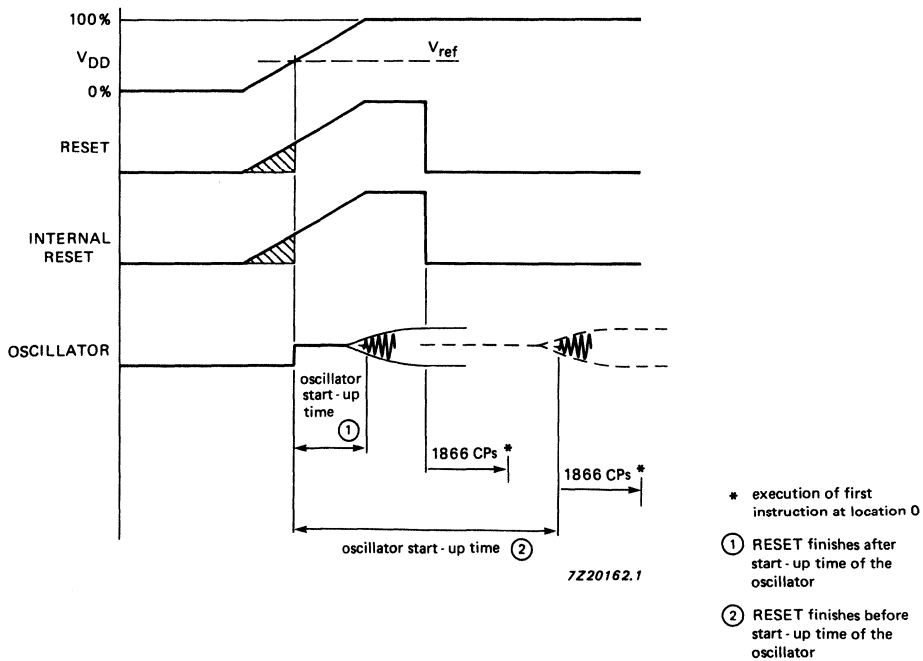


Fig. 28 Timing of external power-on-reset.

INSTRUCTION SET

The PCF84CXX instruction set consists of over 80 one and two byte instructions. Program code efficiency is high because all RAM locations and all ROM locations on a 256 type page require only a single byte address.

Table 7 gives the instruction set of the PCF84CXX. Table 6 shows the instruction map and Table 5 details the symbols that are used.

Table 5 Symbols and definitions used in Table 7

symbol	description
A	accumulator
addr	program memory address
Bb	bit designation (b = 0-7)
RBS	register bank select
C	carry bit (bit CY)
CNT	event counter
Dx	mnemonic derivative register (x = 0 ... 255)
data	8-bit number or expression
I	interrupt
MB	memory bank
MBFF	memory bank flip-flop
P	mnemonic for 'in-page' operation
PC	program counter
Pp	port designation (p = 0, 1 or 2)
PSW	program status word
RB	register bank
Rr	register designation (r = 0-7)
Sn	serial I/O register
SP	stack pointer
T	timer
TF	timer flag
T0, T1	test 0 and 1 inputs
#	immediate data prefix
@	indirect address prefix
(X)	contents of X
((X))	contents of location addressed by X
←	is replaced by
↔	is exchanged with

INSTRUCTION SET (continued)

Table 6 PCF84CXX instruction map

first hexadecimal character of opcode ↓ / second hexadecimal character of opcode →	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	NOP	IDLE		ADD A, # data	JMP page 0	EN I	JNTF addr	DEC A	IN A,Pp 0	IN A,Pp 1	IN A,Pp 2		MOV A,Sn 0	MOV A,Sn 1		
1	INC ∂Rr 0	INC ∂Rr 1	JB0 addr	ADDC A, # data	CALL page 0	DIS I	JTF addr	INC A	INC Rr 0	INC Rr 1	INC Rr 2	INC Rr 3	INC Rr 4	INC Rr 5	INC Rr 6	INC Rr 7
2	XCH A,∂Rr 0	XCH A,∂Rr 1	STOP	MOV A, # data	JMP page 1	EN TCNTI	JNT0 addr	CLR A	XCH A,Rr 0	XCH A,Rr 1	XCH A,Rr 2	XCH A,Rr 3	XCH A,Rr 4	XCH A,Rr 5	XCH A,Rr 6	XCH A,Rr 7
3	XCHD A,∂Rr 0	XCHD A,∂Rr 1	JB1 addr		CALL page 1	DIS TCNTI	JT0 addr	CPL A	OUTL Pp,A 0	OUTL Pp,A 1	OUTL Pp,A 2		MOV Sn,A 0	MOV Sn,A 1	MOV Sn,A 2	
4	ORL A,∂Rr 0	ORL A,∂Rr 1	MOV A, T	ORL A, # data	JMP page 2	STRT CNT	JNT1 addr	SWAP A	ORL A,Rr 0	ORL A,Rr 1	ORL A,Rr 2	ORL A,Rr 3	ORL A,Rr 4	ORL A,Rr 5	ORL A,Rr 6	ORL A,Rr 7
5	ANL A,∂Rr 0	ANL A,∂Rr 1	JB2 addr	ANL A, # data	CALL page 2	STRT T	JT1 addr	DA A	ANL A,Rr 0	ANL A,Rr 1	ANL A,Rr 2	ANL A,Rr 3	ANL A,Rr 4	ANL A,Rr 5	ANL A,Rr 6	ANL A,Rr 7
6	ADD A,∂Rr 0	ADD A,∂Rr 1	MOV T, A		JMP page 3	STOP TCNT		RRC A	ADD A,Rr 0	ADD A,Rr 1	ADD A,Rr 2	ADD A,Rr 3	ADD A,Rr 4	ADD A,Rr 5	ADD A,Rr 6	ADD A,Rr 7
7	ADDC A,∂Rr 0	ADDC A,∂Rr 1	JB3 addr		CALL page 3			RR A	ADDC A,Rr 0	ADDC A,Rr 1	ADDC A,Rr 2	ADDC A,Rr 3	ADDC A,Rr 4	ADDC A,Rr 5	ADDC A,Rr 6	ADDC A,Rr 7
8				RET	JMP page 4	EN SI			ORL Pp, 0	ORL Pp, 1	ORL Pp, 2		MOV A, Dx	MOV Dx, A	ANL Dx, A	ORL Dx, A
9			JB4 addr	RETR	CALL page 4	DIS SI	JNZ addr	CLR C	ANL Pp,# data 0	ANL Pp,# data 1	ANL Pp,# data 2		MOV Sn,# data 0	MOV Sn,# data 1	MOV Sn,# data 2	
A	MOV ∂Rr,A 0	MOV ∂Rr,A 1		MOVP A,∂A	JMP page 5	SEL MB2		CPL C	MOV Rr,A 0	MOV Rr,A 1	MOV Rr,A 2	MOV Rr,A 3	MOV Rr,A 4	MOV Rr,A 5	MOV Rr,A 6	MOV Rr,A 7
B	MOV ∂Rr, # data 0	MOV ∂Rr, # data 1	JB5 addr	JMPP ∂A	CALL page 5	SEL MB3			MOV Rr, # data 0	MOV Rr, # data 1	MOV Rr, # data 2	MOV Rr, # data 3	MOV Rr, # data 4	MOV Rr, # data 5	MOV Rr, # data 6	MOV Rr, # data 7
C	DEC ∂Rr 0				JMP page 6	SEL RB0	JZ addr	MOV A, PSW	DEC Rr 0	DEC Rr 1	DEC Rr 2	DEC Rr 3	DEC Rr 4	DEC Rr 5	DEC Rr 6	DEC Rr 7
D	XRL A,∂Rr 0	XRL A,∂Rr 1	JB6 addr	XRL A,# data	CALL page 6	SEL RB1		MOV PSW, A	XRL A,Rr 0	XRL A,Rr 1	XRL A,Rr 2	XRL A,Rr 3	XRL A,Rr 4	XRL A,Rr 5	XRL A,Rr 6	XRL A,Rr 7
E	DJNZ ∂Rr,addr 0	DJNZ ∂Rr,addr 1			JMP page 7	SEL MB0	JNC addr	RL A	DJNZ Rr, addr 0	DJNZ Rr, addr 1	DJNZ Rr, addr 2	DJNZ Rr, addr 3	DJNZ Rr, addr 4	DJNZ Rr, addr 5	DJNZ Rr, addr 6	DJNZ Rr, addr 7
F	MOV A,∂Rr 0	MOV A,∂Rr 1	JB7 addr		CALL page 7	SEL MB1	JC addr	RLC A	MOV A,Rr 0	MOV A,Rr 1	MOV A,Rr 2	MOV A,Rr 3	MOV A,Rr 4	MOV A,Rr 5	MOV A,Rr 6	MOV A,Rr 7

Table 7 Instruction set

	mnemonic	opcode (hex.)	bytes/ cycles	description	function		notes
ACCUMULATOR	ADD A, Rr	6*	1/1	Add register contents to A	(A)←(A) + (Rr)	r = 0–7	1
	ADD A, @Rr	60 61	1/1	Add RAM data, addressed by Rr, to A	(A)←(A) + ((R0)) (A)←(A) + ((R1))		1
	ADD A, #data	03 data	2/2	Add immediate data to A	(A)←(A) + data		1
	ADDC A, Rr	7*	1/1	Add carry and register contents to A	(A)←(A) + (Rr) + (C)	r = 0–7	1
	ADDC A, @Rr	70 71	1/1	Add carry and RAM data, addressed by Rr, to A	(A)←(A) + ((R0)) + (C) (A)←(A) + ((R1)) + (C)		1
	ADDC A, #data	13 data	2/2	Add carry and immediate data to A	(A)←(A) + data + (C)		1
	ANL A, Rr	5*	1/1	'AND' Rr with A	(A)←(A) AND (Rr)	r = 0–7	
	ANL A, @Rr	50 51	1/1	'AND' RAM data, addressed by Rr, with A	(A)←(A) AND ((R0)) (A)←(A) AND ((R1))		
	ANL A, #data	53 data	2/2	'AND' immediate data with A	(A)←(A) AND data		
	ORL A, Rr	4*	1/1	'OR' Rr with A	(A)←(A) OR (Rr)	r = 0–7	
	ORL A, @Rr	40 41	1/1	'OR' RAM data, addressed by Rr, with A	(A)←(A) OR ((R0)) (A)←(A) OR ((R1))		
	ORL A, #data	43 data	2/2	'OR' immediate data with A	(A)←(A) OR data		
	XRL A, Rr	D*	1/1	'XOR' Rr with A	(A)←(A) XOR (Rr)	r = 0–7	
	XRL A, @Rr	D0 D1	1/1	'XOR' RAM, addressed by Rr, with A	(A)←(A) XOR ((R0)) (A)←(A) XOR ((R1))		
	XRL A, #data	D3 data	2/2	'XOR' immediate data with A	(A)←(A) XOR data		
	INC A	17	1/1	increment A by 1	(A)←(A) + 1		
	DEC A	07	1/1	decrement A by 1	(A)←(A) −1		
	CLR A	27	1/1	clear A to zero	(A)←0		
	CPL A	37	1/1	one's complement A	(A)←NOT(A)		
	RL A	E7	1/1	rotate A left	$(A_{n+1})\leftarrow(A_n)$ $(A_0)\leftarrow(A_7)$	n = 0–6	

INSTRUCTION SET (continued)

ACCUMULATOR (cont.)	RLC A	F7	1/1	rotate A left through carry	$(A_{n+1})\leftarrow A_n$ $(A_0)\leftarrow(C)$, $(C)\leftarrow(A_7)$	n = 0–6	2
	RR A	77	1/1	rotate A right	$(A_n)\leftarrow(A_{n+1})$ $(A_7)\leftarrow(A_0)$	n = 0–6	
	RRC A	67	1/1	rotate A right through carry	$(A_n)\leftarrow(A_{n+1})$ $(A_7)\leftarrow(C)$, $(C)\leftarrow(A_0)$	n = 0–6	2
	DA A	57	1/1	decimal adjust A			2
	SWAP A	47	1/1	swap nibbles of A	$(A_{4-7})\leftrightarrow(A_{0-3})$		
DATA MOVES	MOV A, Rr	F*	1/1	move register contents to A	(A)←(Rr)	r = 0–7	
	MOV A, @Rr	F0 F1	1/1	move RAM data, addressed by Rr, to A	(A)←((R0)) (A)←((R1))		
	MOV A, #data	23 data	2/2	move immediate data to A	(A)←data		
	MOV Rr, A	A*	1/1	move accumulator contents to register	(Rr)←(A)	r = 0–7	
	MOV @Rr, A	A0 A1	1/1	move accumulator contents to RAM location addressed by Rr	((R0))←(A) ((R1))←(A)		
	MOV Rr, #data	B* data	2/2	move immediate data to Rr	(Rr)←data		
	MOV @Rr, #data	B0 data B1 data	2/2	move immediate data to RAM location addressed by Rr	((R0))←data ((R1))←data		
	XCH A, Rr	2*	1/1	exchange accumulator contents with Rr	(A)↔(Rr)	r = 0–7	
	XCH A, @Rr	20 21	1/1	exchange accumulator contents with RAM data addressed by Rr	(A)↔((R0)) (A)↔((R1))		
	XCHD A, @Rr	30 31	1/1	exchange lower nibbles of A and RAM data addressed by Rr	$(A_{0-3})\leftrightarrow((R0_{0-3}))$ $(A_{0-3})\leftrightarrow((R1_{0-3}))$		
	MOV A, PSW	C7	1/1	move PSW contents to accumulator	(A)←(PSW)		
	MOV PSW, A	D7	1/1	move accumulator bit 3 to PSW_3	$(PSW_3)\leftarrow(A_3)$		3
	MOVP A, @A	A3	1/2	move indirectly addressed data in current page to A	$(PC_{0-7})\leftarrow(A)$, (A)←((PC))		
FLAGS	CLR C	97	1/1	clear carry bit	(C)←0		2
	CPL C	A7	1/1	complement carry bit	(C)←NOT(C)		2

	mnemonic	opcode (hex.)	bytes/ cycles	description	function	notes
REGISTER	INC Rr	1*	1/1	increment register by 1	(Rr)←(Rr) + 1 r = 0–7	
	INC @Rr	10 11	1/1	increment RAM data, addressed by Rr, by 1	((R0))←((R0)) + 1 ((R1))←((R1)) + 1	
	DEC Rr	C*	1/1	decrement register by 1	(Rr)←(Rr) – 1 r = 0–7	
	DEC @Rr	C0 C1	1/1	decrement RAM data, addressed by Rr, by 1	((R0))←((R0)) – 1 ((R1))←((R1)) – 1	
BRANCH	JMP addr	• 4 address	2/2	unconditional jump within a 2 K bank	(PC_{8-10})←$addr_{8-10}$ (PC_{0-7})←$addr_{0-7}$ (PC_{11-12})←MBFF 0–1	
	JMPP @A	B3	1/2	indirect jump within a page	(PC_{0-7})←((A))	
	DJNZ Rr, addr	E* address	2/2	decrement Rr by 1 and jump if not zero to addr	(Rr)←(Rr) – 1 r = 0–7 if (Rr) not zero (PC_{0-7})←addr	
	DJNZ @Rr, addr	E0	2/2	decrement RAM data, addressed by Rr by 1 and jump if not zero to addr	((R0))←((R0)) – 1 if ((R0)) not zero (PC_{0-7})←addr	
		E1			((R1))←((R1)) – 1 if ((R1)) not zero (PC_{0-7})←addr	
	JBb addr	▲ 2 address	2/2	jump to addr if Acc. bit b = 1	if b = 1 : (PC_{0-7})←addr b = 0–7	
	JC addr	F6 address	2/2	jump to addr if C = 1	if C = 1 : (PC_{0-7})←addr	
	JNC addr	E6 address	2/2	jump to addr if C = 0	if C = 0 : (PC_{0-7})←addr	
	JZ addr	C6 address	2/2	jump to addr if A = 0	if A = 0 : (PC_{0-7})←addr	
	JNZ addr	96 address	2/2	jump to addr if A is NOT zero	if A≠0 : (PC_{0-7})←addr	
	JT0 addr	36 address	2/2	jump to addr if T0 = 1	if T0 = 1: (PC_{0-7})←addr	
	JNT0 addr	26 address	2/2	jump to addr if T0 = 0	if T0 = 0: (PC_{0-7})←addr	
	JT1 addr	56 address	2/2	jump to addr if T1 = 1	if T1 = 1: (PC_{0-7})←addr	
	JNT1 addr	46 address	2/2	jump to addr if T1 = 0	if T1 = 0: (PC_{0-7})←addr	
	JTF addr	16 address	2/2	jump to addr if Timer Flag = 1	if TF = 1: (PC_{0-7})←addr	4
	JNTF addr	06 address	2/2	jump to addr if Timer Flag = 0	if TF = 0: (PC_{0-7})←addr	

INSTRUCTION SET (continued)

TIMER/EVENT COUNTER	MOV A, T	42	1/1	move timer/event counter contents to accumulator	(A)←(T)	
	MOV T, A	62	1/1	move accumulator contents to timer/event counter	(T)←(A)	
	STRT CNT	45	1/1	start event counter		
	STRT T	55	1/1	start timer		
	STOP TCNT	65	1/1	stop timer/event counter		
	EN TCNTI	25	1/1	enable timer/event counter interrupt		
	DIS TCNTI	35	1/1	disable timer/event counter interrupt		
CONTROL	EN I	05	1/1	enable external interrupt		
	DIS I	15	1/1	disable external interrupt		
	SEL RB0	C5	1/1	select register bank 0	(RBS)←0	5
	SEL RB1	D5	1/1	select register bank 1	(RBS)←1	5
	SEL MB0	E5	1/1	select program memory bank 0	(MBFF0)←0, (MBFF1)←0	
	SEL MB1	F5	1/1	select program memory bank 1	(MBFF0)←1, (MBFF1)←0	10
	SEL MB2	A5	1/1	select program memory bank 2	(MBFF0)←0, (MBFF1)←1	10
	SEL MB3	B5	1/1	select program memory bank 3	(MBFF0)←1, (MBFF1)←1	10
	STOP	22	1/1	enter STOP mode		
	IDLE	01	1/1	enter IDLE mode		
SUBROUTINE	CALL addr	▲ 4 address	2/2	jump to subroutine	((SP))←(PC), ($PSW_{4, 6, 7}$) (SP)←(SP) + 1 (PC_{8-10})←$addr_{8-10}$ (PC_{0-7})←$addr_{0-7}$ (PC_{11-12})←MBFF 0–1	6
	RET	83	1/2	return from subroutine	(SP)←(SP) − 1 (PC)←((SP))	6
	RETR	93	1/2	return from interrupt and restore bits 4, 6, 7 of PSW	(SP)←(SP) − 1 ($PSW_{4, 6, 7}$) + (PC)←((SP))	6

DEVELOPMENT DATA

	mnemonic	opcode (hex.)	bytes/ cycles	description	function	notes
PARALLEL INPUT/OUTPUT	IN A, Pp	08 09 0A	1/2	input port p data to accumulator	(A)←(P0) (A)←(P1) (A)←(P2)	7
	OUTL Pp, A	38 39 3A	1/2	output accumulator data to port p	(P0)←(A) (P1)←(A) (P2)←(A)	
	ANL Pp, #data	98 data 99 data 9A data	2/2	AND port p data with immediate data	(P0)←(P0) AND data (P1)←(P1) AND data (P2)←(P2) AND data	
	ORL Pp, #data	88 data 89 data 8A data	2/2	OR port p data with immediate data	(P0)←(P0) OR data (P1)←(P1) OR data (P2)←(P2) OR data	
DERIVATIVE INPUT/OUTPUT	MOV A, Dx	8C	2/2	move derivative register contents to accumulator	(A)←(Dx) x = 0 to 255	8
	MOV Dx, A	8D	2/2	move accumulator contents to derivative register	(Dx)←(A) x = 0 to 255	8
	ANL Dx, A	8E	2/2	AND derivative register with accumulator	(Dx)←(Dx) AND (A) x = 0 to 255	8
	ORL Dx, A	8F	2/2	OR derivative register with accumulator	(Dx)←(Dx) OR (A) x = 0 to 255	8

INSTRUCTION SET (continued)

	mnemonic	opcode (hex.)	bytes/ cycles	description	function	notes
SERIAL INPUT/OUTPUT	MOV A, S_n	0C 0D	1/2	move serial I/O register contents to accumulator	(A)←(S0) (A)←(S1)	9
	MOV S_n, A	3C 3D 3E	1/2	move accumulator contents to serial I/O register	(S0)←(A) (S1)←(A) (S2)←(A)	
	MOV S_n, #data	9C data 9D data 9E data	2/2	move immediate data to serial I/O register	(S0)←data (S1)←data (S2)←data	
	EN SI	85	1/1	enable serial I/O interrupt		
	DIS SI	95	1/1	disable serial I/O interrupt		
	NOP	00	1/1	no operation		

Notes to Table 8

1. PSW CY, AC affected
2. PSW CY affected
3. PSW PS affected
4. Execution of a JTF or JNTF instruction resets the Timer Flag (TF).
5. PSW RBS affected
6. PSW SP_0, SP_1, SP_2 affected
7. (A) = 0000P23, P22, P21, P20.
8. Instructions for PCF84C00T only.
9. (S1) has a different meaning for read and write operation, see serial I/O interface.
10. SEL MB1, SEL MB2 and SEL MB3 may not be used within interrupt routines.

* : 8, 9, A, B, C, D, E, F
● : 0, 2, 4, 5, 6, A, C, E
▲ : 1, 3, 5, 7, 9, B, D, F

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 28)	V_{DD}		−0,8 to +8	V
All input voltages	V_I		−0,5 to V_{DD} +0,5	V
DC current into any input or output	$\pm I_I$, $\pm I_O$	max.	10	mA
Total power dissipation (see note)	P_{tot}	max.	125	mW
Storage temperature range	T_{stg}		−65 to +150	°C
Operating ambient temperature range (if P_{tot} max. = 100 mW)	T_{amb}		−40 to +70	°C
Operating ambient temperature range (if P_{tot} max. = 30 mW)	T_{amb}		−40 to +85	°C
Operating junction temperature	T_j	max.	90	°C

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, it is good practice to take normal precautions appropriate to handling MOS devices (see 'Handling MOS devices').

Note

Thermal resistance (junction to ambient)

for SOT-117	$R_{th\ j\text{-}a}$	max.	120	K/W
for SOT-135A	$R_{th\ j\text{-}a}$	max.	60	K/W
for SOT-136A	$R_{th\ j\text{-}a}$	max.	150	K/W

DEVELOPMENT DATA

DC CHARACTERISTICS

V_{DD} = 2,5 to 5,5 V; V_{SS} = 0 V; T_{amb} = −40 to +85 °C; all voltages with respect to V_{SS}; unless otherwise specified.

parameter	symbol	min.	typ.	max.	unit
Supply voltage					
operating (see Fig. 33)	V_{DD}	2,5	–	5,5	V
Supply current					
operating (see Fig. 34; not valid for PCF84C00)					
at V_{DD} = 5 V; f_{XTAL} = 10 MHz	I_{DD}	–	1,6	3,2	mA
at V_{DD} = 5 V; f_{XTAL} = 6 MHz	I_{DD}	–	1	2	mA
at V_{DD} = 3 V; f_{XTAL} = 3,58 MHz	I_{DD}	–	0,3	0,6	mA
IDLE mode (see Fig. 35; not valid for PCF84C00)					
at V_{DD} = 5 V; f_{XTAL} = 10 MHz	I_{DD}	–	0,8	1,6	mA
at V_{DD} = 5 V; f_{XTAL} = 6 MHz	I_{DD}	–	0,5	1	mA
at V_{DD} = 3 V; f_{XTAL} = 3,58 MHz	I_{DD}	–	0,15	0,4	mA
STOP mode (see Fig. 41 and note 1)					
at V_{DD} = 2,5 V; T_{amb} = 25 °C	I_{DD}	–	1,2	2,5	μA
at V_{DD} = 2,5 V; T_{amb} = 85 °C	I_{DD}	–	–	10	μA
Inputs					
Input voltage LOW	V_{IL}	0	–	$0{,}3V_{DD}$	V
Input voltage HIGH	V_{IH}	$0{,}7V_{DD}$	–	V_{DD}	V
Input leakage current					
at $V_{SS} < V_I < V_{DD}$	$\pm I_{IL}$	–	–	1	μA
Outputs					
Output voltage LOW					
at $V_I = V_{SS}$ or V_{DD}; $\|I_O\| < 1$ μA	V_{OL}	–	–	0,05	V
Output sink current LOW					
at V_{DD} = 5 V ± 10%; V_O = 0,4 V					
except P2.3/SDA, SCLK (see Fig. 37) and port 1	I_{OL}	1,6	3	–	mA
P2.3/SDA, SCLK (see Fig. 38)	I_{OL}	3	–	–	mA
P1.0-P1.7 (not PCF84C00) at V_{OL} = 1,2 V	I_{OL}	10	–	–	mA
Pull-up output source current HIGH (see Fig. 39)					
at V_{DD} = 5 V ± 10%; $V_O = 0{,}7V_{DD}$	$-I_{OH}$	40	–	–	μA
at V_{DD} = 5 V ± 10%; $V_O = V_{SS}$	$-I_{OH}$	–	–	400	μA
Push-pull output source current HIGH					
at V_{DD} = 5 V ± 10%; $V_O = V_{DD}$−0,4 V	$-I_{OH}$	1,6	3	–	mA

Note 1: Crystal connected between XTAL1 and XTAL2; T1 = V_{SS}; $\overline{INT}$ = V_{DD}

AC CHARACTERISTICS

V_{DD} = 2,5 to 5,5 V; V_{SS} = 0 V; T_{amb} = −40 to +85 °C. All voltages with respect to V_{SS} unless otherwise specified.

parameter	symbol	min.	typ.	max.	unit
Rise time all outputs (C_L = 50 pF)	t_R	–	30	–	ns
Fall time all outputs (C_L = 50 pF)	t_F	–	30	–	ns
Cycle time	t_{CY}	–	30	–	CP
PCF84C00/non-standard pins:					
Control pulse width	t_{CC}	–	9	–	CP
Address to $\overline{PSEN}$ set-up	t_{AS}	–	1,5	–	CP
Data to $\overline{PSEN}$ set-up	t_{DS}	–	2	–	CP
Data hold time	t_{DR}	0	–	–	ns
Address to data-in	t_{AD}	–	8,5	–	CP
Data out to $\overline{DWXR}$ set-up	t_{SDO}	–	2	–	CP
Data out to $\overline{DXWR}$ hold	t_{HDO}	–	1	–	CP
Time from DXALE to $\overline{PSEN}$	t_{SLPH}	–	1,5	–	CP
Data-in to $\overline{DXRD}$ set-up	t_{DS1}	–	2,5	–	CP
Data-in to $\overline{DXRD}$ hold	t_{DR1}	0	–	–	ns
HIGH time of DXALE	t_{DXALE}	–	4,5	–	CP
LOW time of $\overline{DXRD}$	t_{DXRD}	–	6	–	CP
LOW time of $\overline{DXWR}$	t_{DXWR}	–	3	–	CP

Note: 1 clock pulse (CP) = $1/f_{XTAL}$.

DEVELOPMENT DATA

AC CHARACTERISTICS (continued)

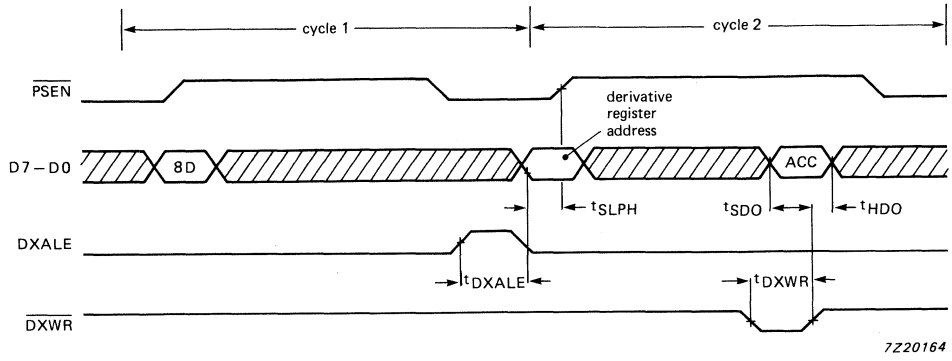


Fig. 29 MOV Dx,A timing (PCF84C00T only).

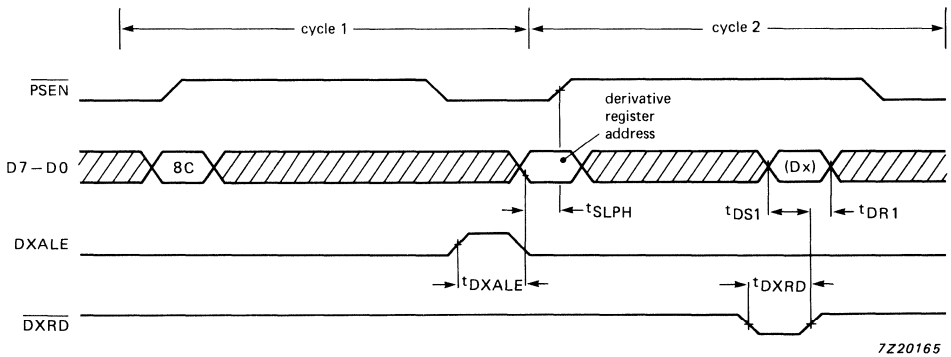


Fig. 30 MOV A,Dx timing (PCF84C00T only).

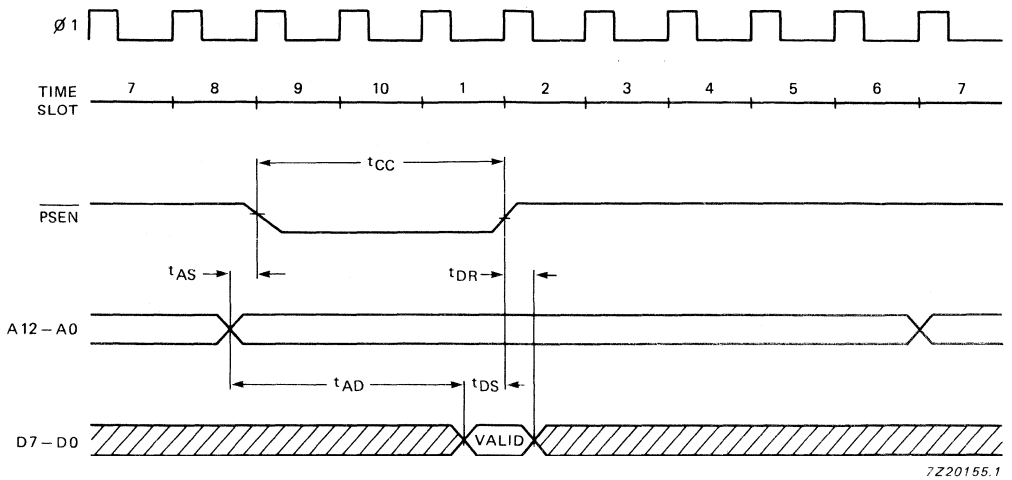


Fig. 31 External memory access timing (PCF84C00T only).

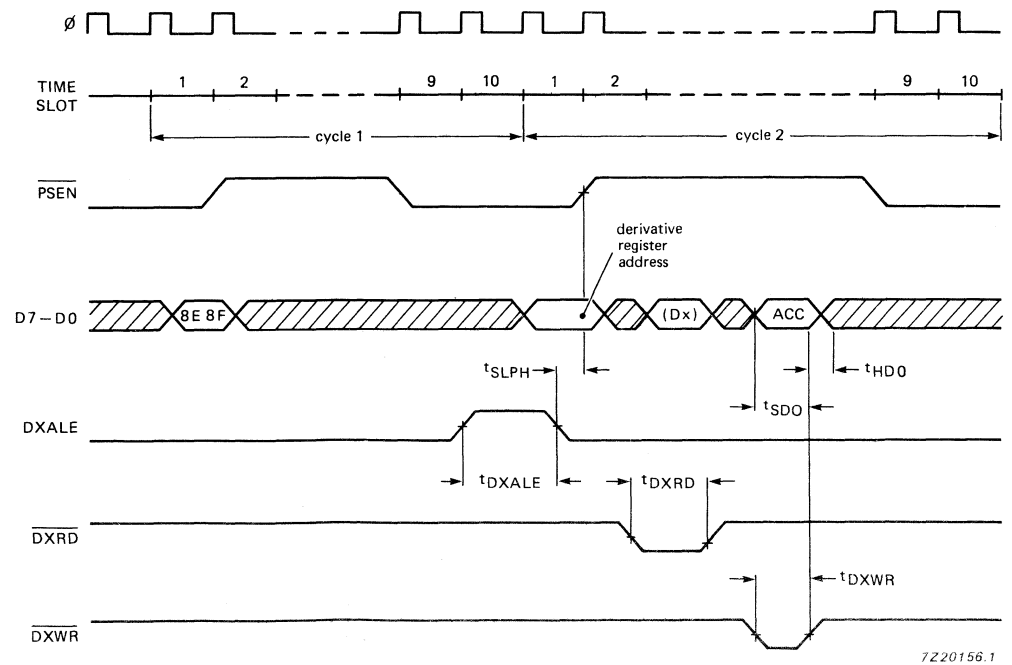
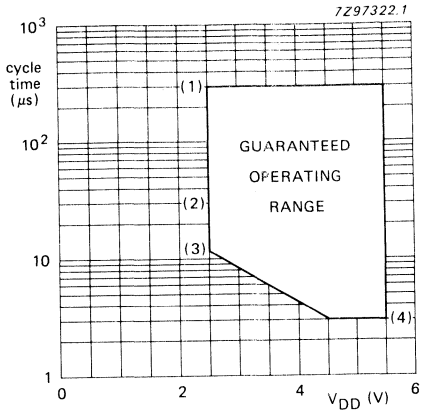


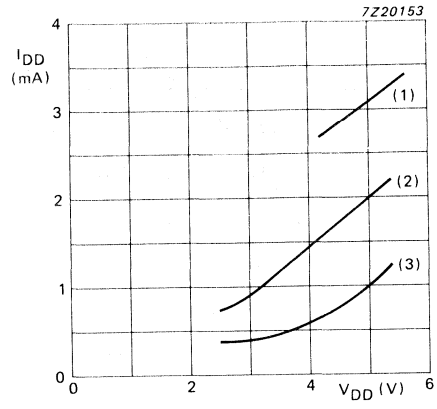
Fig. 32 ANL/ORL derivative interface timing (PCF84C00T only).

AC CHARACTERISTICS (continued)



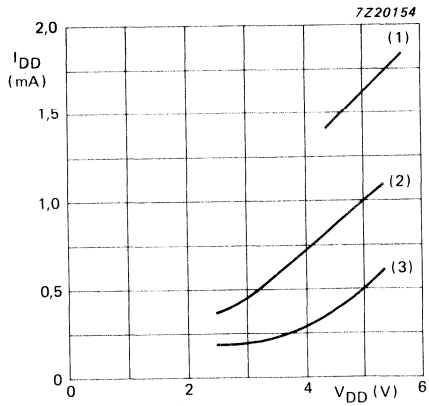
(1) clock frequency = 100 kHz
(2) clock frequency = 1 MHz
(3) clock frequency = 3 MHz
(4) clock frequency = 10 MHz

Fig. 33 Maximum clock frequency (f_{XTAL}) as a function of the supply voltage (V_{DD}).



(1) clock frequency = 10 MHz
(2) clock frequency = 6 MHz
(3) clock frequency = 3,58 MHz

Fig. 34 Maximum supply current (I_{DD}) in operation mode as a function of the supply voltage (V_{DD}).



(1) clock frequency = 10 MHz
(2) clock frequency = 6 MHz
(3) clock frequency = 3,58 MHz

Fig. 35 Maximum supply current (I_{DD}) in IDLE mode as a function of the supply voltage (V_{DD}).

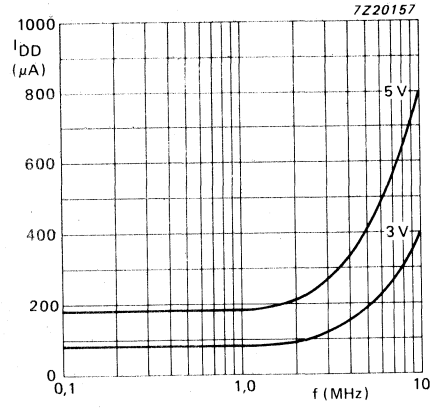


Fig. 36 Typical supply current during IDLE mode as a function of frequency at V_{DD} = 3 V and V_{DD} = 5 V.

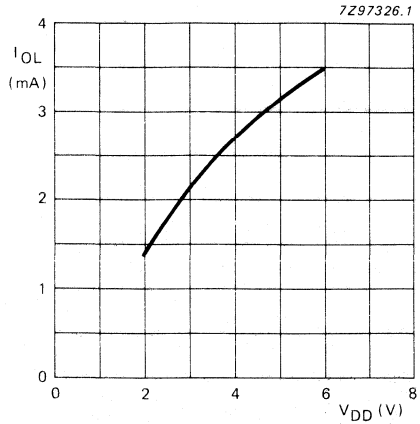


Fig. 37 Typical output sink current (I_{OL}), outputs P0.0 to P0.7 and P2.0 to P2.2, as a function of the supply voltage (V_{DD}); V_O = 0,4 V.

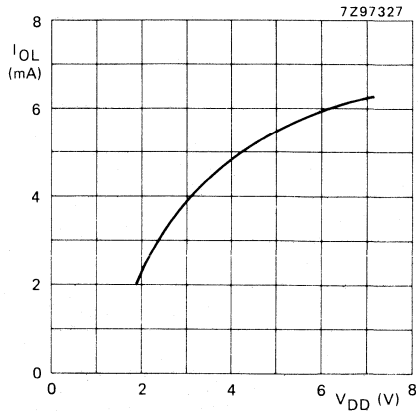


Fig. 38(a) Typical output sink current (I_{OL}), outputs P2.3/SDA and SCLK, as a function of the supply voltage (V_{DD}); V_O = 0,4 V.

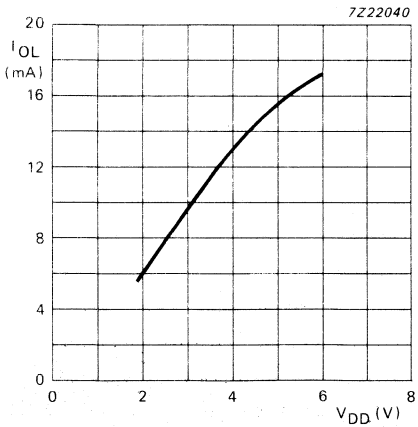
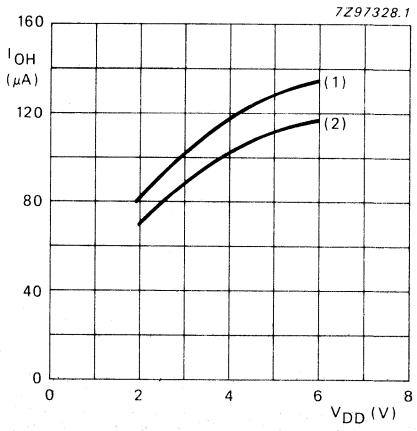


Fig. 38(b) Typical output sink current (I_{OL}), outputs P1.0 to P1.7, as a function of the supply voltage (V_{DD}); V_O = 1,2 V.



(1) $V_O = V_{SS}$
(2) $V_O = 0{,}7\ V_{DD}$

Fig. 39 Typical output source current ($-I_{OH}$) as a function of the supply voltage (V_{DD}).

DEVELOPMENT DATA

AC CHARACTERISTICS (continued)

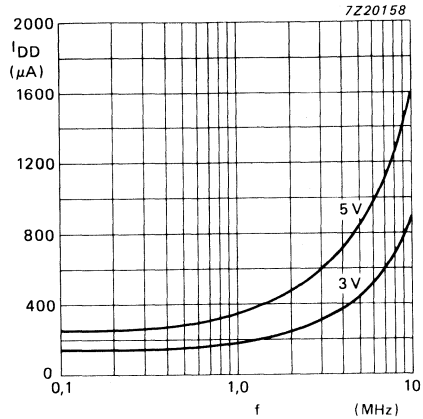
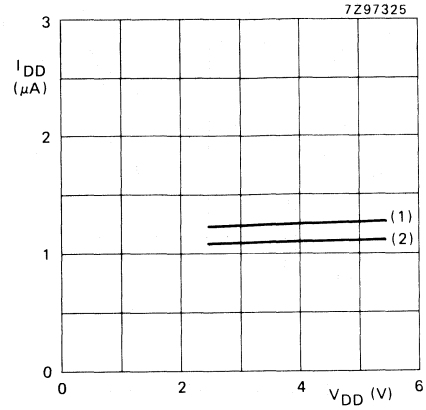


Fig. 40 Typical supply current during operating mode as a function of frequency at V_{DD} = 3 V and V_{DD} = 5 V.



(1) T_{amb} = 85 °C
(2) T_{amb} = 25 °C

Fig. 41 Typical supply current (I_{DD}) in STOP mode as a function of the supply voltage (V_{DD}).

Table 8 Input timing shown in figure 42.

symbol	timing
t_{BUF}	$\geqslant 14t_{XTAL}$
$t_{HD;STA}$	$\geqslant 14t_{XTAL}$
t_{HIGH}	$\geqslant 17t_{XTAL}$
t_{LOW}	$\geqslant 17t_{XTAL}$
$t_{SU;STO}$	$\geqslant 14t_{XTAL}$
$t_{HD;DAT}$	> 0
$t_{SU;DAT}$	$\geqslant 250$ ns
t_{RD}	$\leqslant 1$ μs
t_{RC}	$\leqslant 1$ μs
t_{FD}	$\leqslant 1$ μs
t_{FC}	$\leqslant 0{,}3$ μs

Notes to Table 8

t_{XTAL} = one period of the XTAL input frequency (f_{XTAL})
= 167 ns for f_{XTAL} = 6 MHz
These figures apply to all modes.

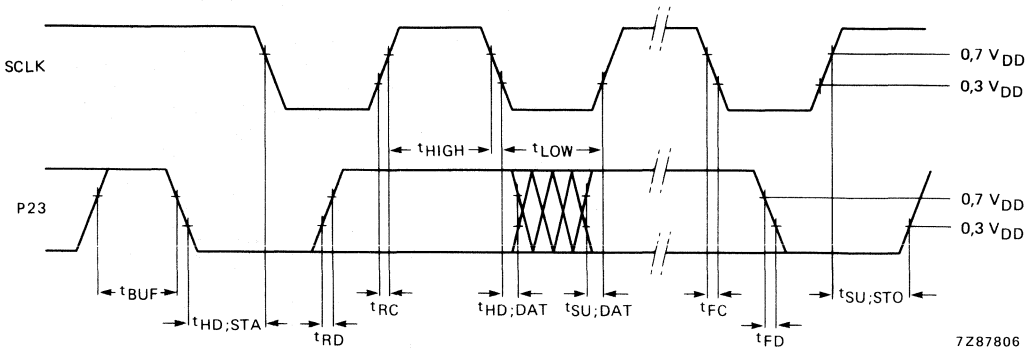


Fig. 42 PCF84CXX timing requirements for the P2.3 and SCLK *input* signals.

DEVELOPMENT DATA

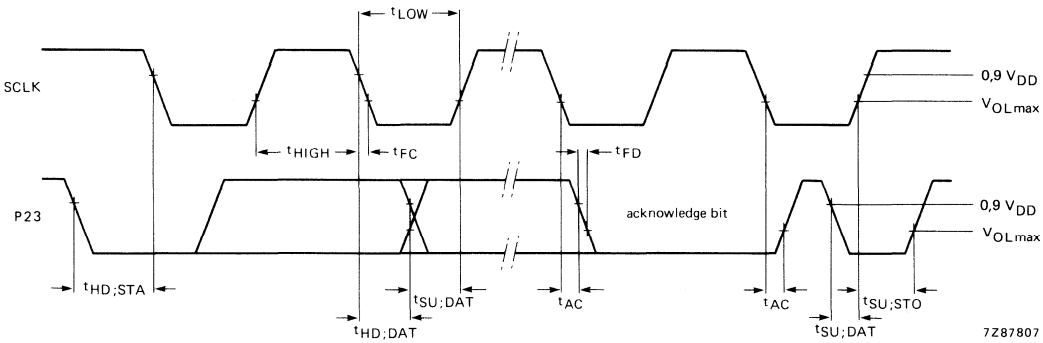


Fig. 43 PCF84CXX timing requirements for the P2.3 and SCLK *output* signals.

AC CHARACTERISTICS (continued)

Table 9 Output timing shown in figure 43

symbol	timing	
	normal mode (ASC in S2 = 0)	low-speed mode (ASC in S2 = 1)
$t_{HD;STA}$	½ (DF + 9) t_{XTAL}	¾ (DF + 9) t_{XTAL}
t_{HIGH}	½ (DF) t_{XTAL}	¾ (DF) t_{XTAL}
t_{LOW}	½ (DF) t_{XTAL}	¼ (DF) t_{XTAL}
$t_{SU;STO}$	½ (DF − 3) t_{XTAL}	¼ (DF − 3) t_{XTAL}
$t_{HD;DAT}$ (slave transmitter) any DF	$\geqslant 9t_{XTAL}$ $\leqslant 12t_{XTAL}$	$\geqslant 9t_{XTAL}$ $\leqslant 12t_{XTAL}$
$t_{HD;DAT}$ (master transmitter) for DF $\leqslant 51$	$\geqslant 9t_{XTAL}$ $\leqslant 12t_{XTAL}$	– –
for DF $\leqslant 99$	– –	$\geqslant 9t_{XTAL}$ $\leqslant 12t_{XTAL}$
$t_{SU;DAT}$ (master transmitter) for DF > 51	$\geqslant 15t_{XTAL}$ $\leqslant 24t_{XTAL}$	– –
for DF > 99	– –	$\geqslant 15t_{XTAL}$ $\leqslant 24t_{XTAL}$
t_{AC}	$\geqslant 9t_{XTAL}$ $\leqslant 12t_{XTAL}$	$\geqslant 9t_{XTAL}$ $\leqslant 12t_{XTAL}$
t_{FD}, t_{FC}	$\leqslant$ 100 ns at C_b = 400 pF	$\leqslant$ 100 ns at C_b = 400 pF

Notes to Table 9

t_{XTAL} = one period of the XTAL input frequency (f_{XTAL})
= 167 ns for f_{XTAL} = 6 MHz
DF = divisor (see Table 2 Serial I/O section).
C_b = the maximum bus capacitance for each line.

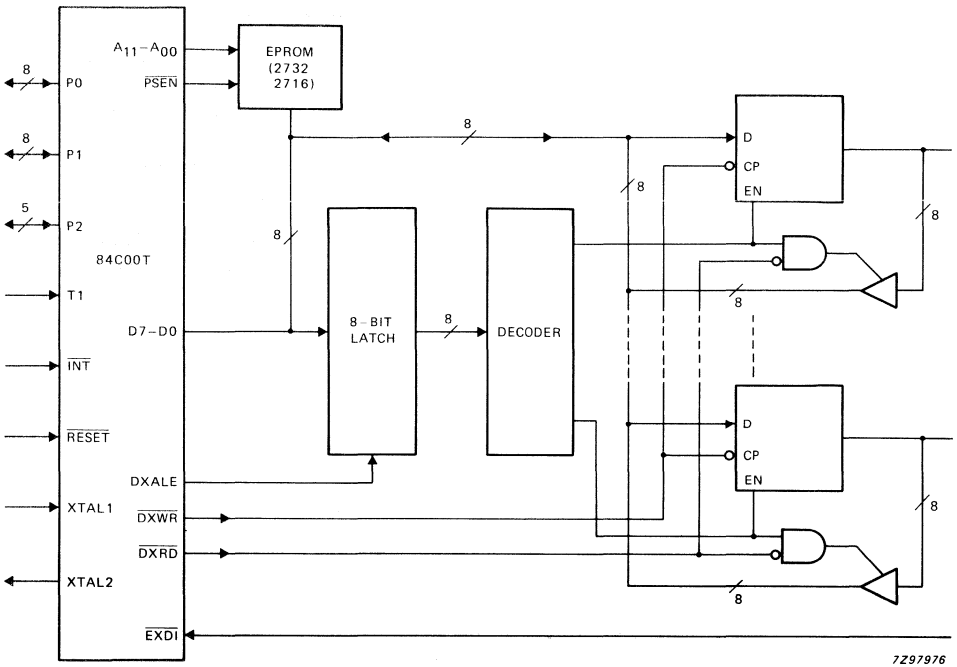


Fig. 44 Block diagram of the external Dx register interface.
The Dx interface can only be used with the PCF84C00T.

SINGLE-CHIP 8-BIT MICROCONTROLLER WITH 32 I/O LINES

DESCRIPTION

The PCF84C85 microcontroller is manufactured in CMOS, and is designed to be an efficient controller as well as an arithmetic processor. The instruction set is based on that of the MAB8048 and is software compatible with the PCF84CXX family. The PCF84C85 has two additional derivative ports and the microcontroller has bit handling abilities and facilities for both binary and BCD arithmetic.

For detailed information on the PCF84CXX see the "Single-chip 8-bit Microcontrollers" user manual.

Features

- 8-bit CPU, ROM, RAM, I/O in a single 40-lead DIL or mini-pack package
- 8 K ROM
- 256 RAM bytes
- 32 quasi-bidirectional I/O port lines
- Two test inputs: one of which is also the external interrupt input
- Single-level vectored interrupts: external, timer/event counter, serial I/O
- I^2C hardware interface for two-line serial data transfer (serial I/O data via an existing port line and clock via a dedicated line)
- 8-bit programmable timer/event counter
- Clock frequency 100 kHz to 10 MHz
- Over 80 instructions (based on MAB8048) all of 1 or 2 cycles
- Single supply voltage from 2,5 V to 5,5 V
- STOP and IDLE mode
- Power-on-reset circuit
- Operating temperature range: −40 to +85 °C

PACKAGE OUTLINES

PCF84C85P: 40-lead DIL; plastic (SOT-129)
PCF84C85T: 40-lead; mini-pack (VSO-40; SOT-158)

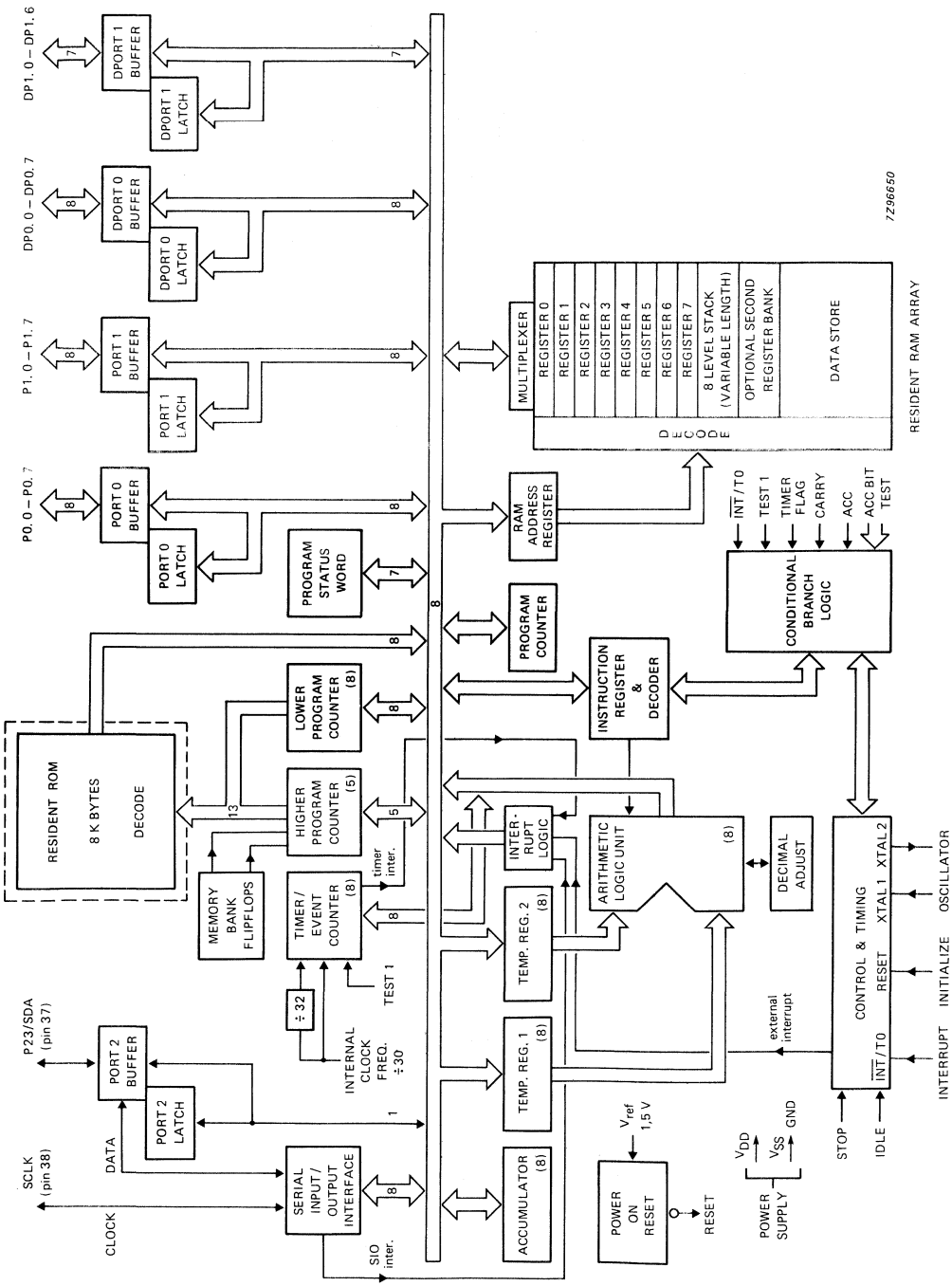


Fig. 1 Block diagram.

DEVELOPMENT DATA

PINNING

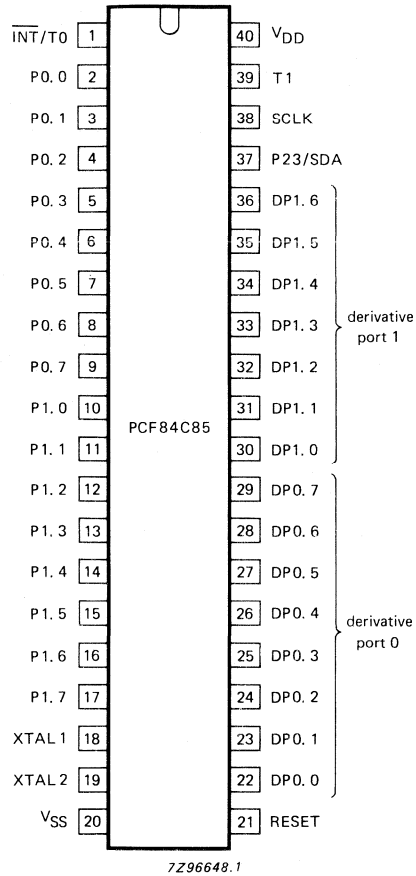


Fig. 2 Pinning diagram.

PIN DESIGNATION

38	SCLK	**Clock:** bidirectional clock for serial I/O.
1	$\overline{\text{INT}}$/T0	**Interrupt/Test 0:** external interrupt input (sensitive to negative-going edge)/test input pin; when used as a test input directly tested by conditional branch instructions JT0 and JNT0.
39	T1	**Test 1:** test input pin, directly tested by conditional branch instructions JT1 and JNT1. T1 also functions as an input to the 8-bit timer/event counter, using the STRT CNT instruction.
18	XTAL 1	**Crystal input:** connection to timing component (crystal) which determines the frequency of the internal oscillator; also the input for an external clock source.
19	XTAL 2	Connection to the other side of the timing component.
21	RESET	**Reset input:** used to initialize the processor (active HIGH), or output of power-on-reset circuit.

PIN DESIGNATION (continued)

2-9	P0.0-P0.7	**Port 0:** 8-bit quasi-bidirectional I/O port.
10-17	P1.0-P1.7	**Port 1:** 8-bit quasi-bidirectional I/O port.
37	P23/SDA	**Port 2:** 1-bit quasi-bidirectional I/O port or serial data input/output in serial I/O mode.
22-29	DP0.0-DP0.7	**Derivative port 0:** 8-bit quasi-bidirectional I/O port.
30-36	DP1.0-DP1.6	**Derivative port 1:** 7-bit quasi-bidirectional I/O port.
20	V_{SS}	**Ground:** circuit earth potentional.
40	V_{DD}	**Power supply:** 2,5 V to 5,5 V.

FUNCTIONAL DESCRIPTION

Program memory

The program memory consists of 8 K bytes, in a read-only memory (ROM). Each location is directly addressable by the program counter. The memory is mask-programmed at the factory. Figure 3 shows the program memory map.

Four program memory locations are of special importance:

- Location 0; contains the first instruction to be executed after the processor is initialized (RESET),
- Location 3; contains the first byte of an external interrupt service subroutine;
- Location 5; contains the first byte of a serial I/O interrupt service subroutine.
- Location 7; contains the first byte of a timer/event counter interrupt service subroutine.

Program memory is arranged in banks of 2 K bytes, which are selected by SEL MB instructions. The program memory is further divided into location 'pages', each of 256 bytes. This latter division applies only for conditional branches. Memory bank boundaries can be crossed only by using unconditional branch instructions after the appropriate memory bank has been selected. A CALL instruction can transfer control to a subroutine on any 'page'; RET and RETR instructions can transfer control from a subroutine back to the main program.

Data memory

Data memory consists of 256 bytes, random-access data memory (RAM). All locations are indirectly addressable using RAM pointer registers; up to 16 designated locations are directly addressable. Memory also includes an 8-level program counter stack addressed by a 3-bit stack pointer. Figure 4 shows the data memory map.

Working registers

Locations 0 to 7 are designated as working registers, directly addressable by the direct register instructions. Ease of addressing, and a minimum requirement of instruction bytes to manipulate their contents, makes these locations suitable for storing frequently addressed intermediate results. This bank of registers can be selected by the SEL RB0 instruction.

Executing the select register bank instruction SEL RB1, designates locations 24 to 31 as working registers, instead of locations 0 to 7, and these are then directly addressable. This second bank of working registers may be used as an extension of the first or reserved for use during interrupt service subroutines saving the first bank for use in the main program. If the second bank is not used, locations 24 to 31 may serve as general purpose RAM.

The first locations of each bank contain the RAM pointer registers R0, R1, R0' and R1', which indirectly address all RAM locations.

All RAM locations make efficient program loop counters when used with the decrement register and test instruction DJNZ.

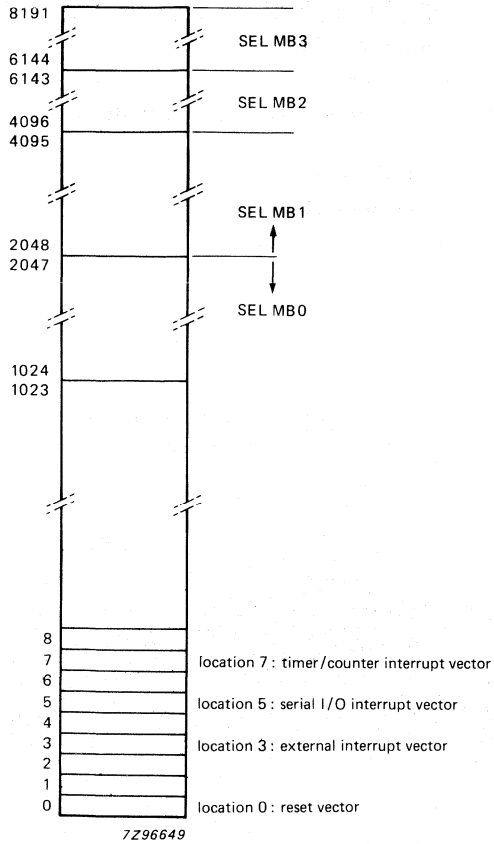


Fig. 3 Program memory map.

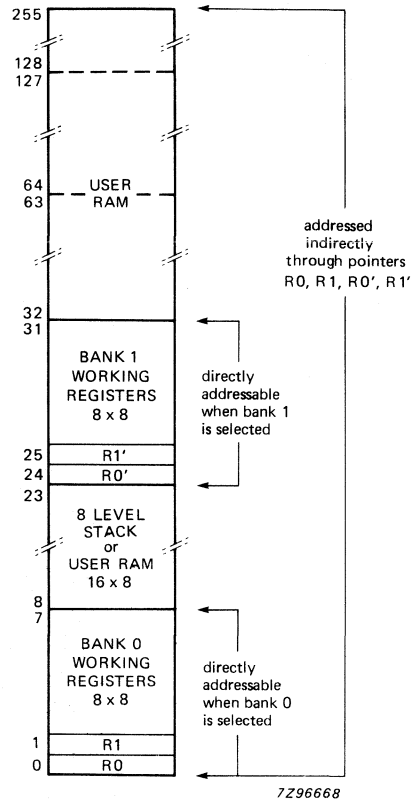


Fig. 4 Data memory map.

Program counter stack

Locations 8 to 23 may be designated as an 8-level program counter stack (2 locations per level), or as general purpose RAM. The program counter stack (Fig.5) enables the processor to keep track of the return addresses and status generated by interrupts or CALL instructions by storing the contents of the program counter prior to servicing the subroutine. A 3-bit stack pointer determines which of the eight register pairs of the program counter stack will be loaded with the next generated return address.

The stack pointer, when initialized to 000 by RESET, points to RAM locations 8 and 9. On the first subroutine CALL or interrupt, the contents of the program counter and bits 4, 6 and 7 of the program status word (PSW) are transferred to locations 8 and 9. The stack pointer increments by one and points to locations 10 and 11 ready for another CALL. Because an address may be up to 13 bits long, two bytes must be used to store each address.

At the end of a subroutine, which is signalled by a return instruction (RET or RETR), the stack pointer decrements by one and the contents of the register pair on top of the stack are transferred to the program counter. The saved PSW bits are transferred to the PSW only by the RETR instruction.

If not all 8 levels of subroutine and interrupt nesting are used, the unused portion of the stack may be used as any other indirectly addressable RAM locations.

Nesting of subroutines within subroutines can continue up to 8 times without overflowing the stack. If overflow does occur the deepest address stored (locations 8 and 9) will be overwritten and lost since the stack pointer overflows from 111 to 000. It also underflows from 000 to 111.

FUNCTIONAL DESCRIPTION (continued)

The value of the saved contents of the program counter is different for an interrupt CALL compared to a normal CALL to subroutine. With an interrupt CALL, the program counter return address is saved; with a subroutine CALL, the saved program counter value is one less than the program counter return address.

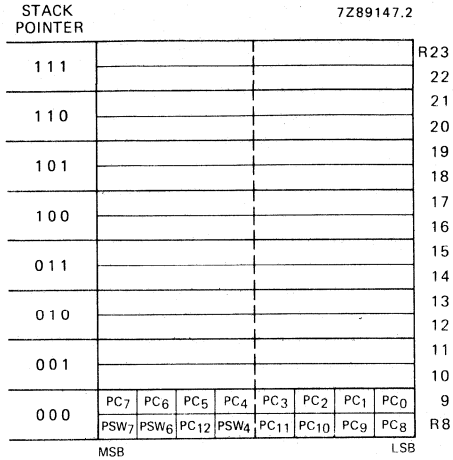


Fig. 5 Program counter stack.

IDLE and STOP modes

IDLE mode

When the microcontroller enters the IDLE mode via the IDLE instruction (01 H) the oscillator, timer/counter and serial I/O are kept running. The microcontroller exits from the IDLE mode by one of three interrupts if they are enabled or by activating a RESET. If the interrupt is not enabled the processor will remain in the IDLE mode. An active signal on the RESET pin restarts the microcontroller and a normal RESET sequence is executed (see Fig. 6).

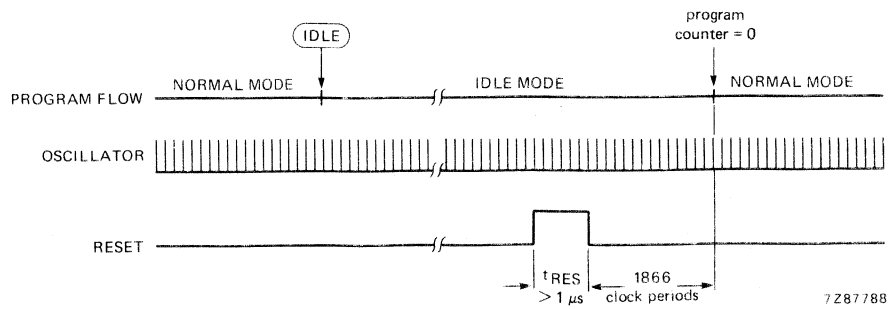


Fig. 6 Exit from IDLE mode via a RESET.

An active signal coming from an enabled interrupt causes the execution of the normal interrupt routine since normal interrupt scanning is still being carried out. A HIGH-to-LOW transition on the external interrupt pin ($\overline{INT}$/T0) reactivates the microcontroller. A LOW level applied to $\overline{INT}$/T0 will reactivate the microcontroller only in the STOP mode. Thus,if $\overline{INT}$/T0 was LOW before the microcontroller entered the IDLE mode, it must go HIGH before the microcontroller can be reactivated (see Fig. 7).

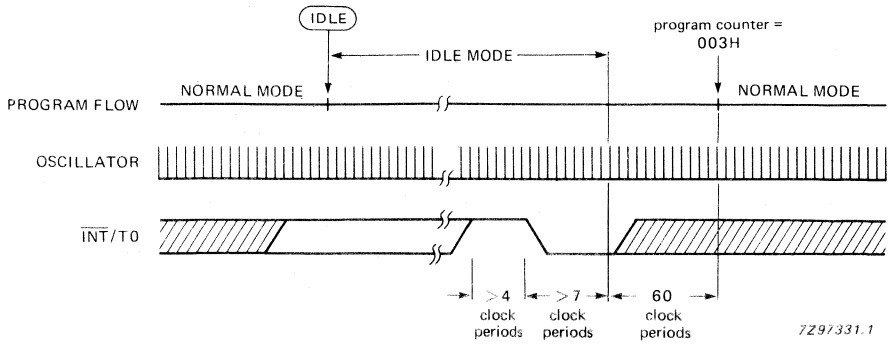


Fig. 7 Exit from IDLE mode via an interrupt.

Wake-up from the IDLE mode is ensured when $\overline{INT}$/T0 is HIGH for at least 4 CP (clock periods) followed by a LOW for 7 CP. After the initial forced CALL (*4H) operation (60 CP) the program continues with the external interrupt service routine.

* 1, 3, 5, 7, 9, B, D and F.

STOP mode

The microcontroller enters the STOP mode by the STOP instruction (22 H). The oscillator is switched off. The internal status of the CPU, RAM contents and the state of I/O ports are not affected. The microcontroller can be brought-out of the STOP mode by an active signal at the external interrupt input or by an external RESET signal. When one of these two signals is applied an internal delay of 1866 CP is provided to ensure that all internal clocks are operating correctly before restart (see Fig. 8). Note; the start-up time of a crystal oscillator is measured in milliseconds, and the 1866 CP count begins after this start-up time.

If the microcontroller exits from the STOP mode by activating RESET, a normal RESET sequence is executed.

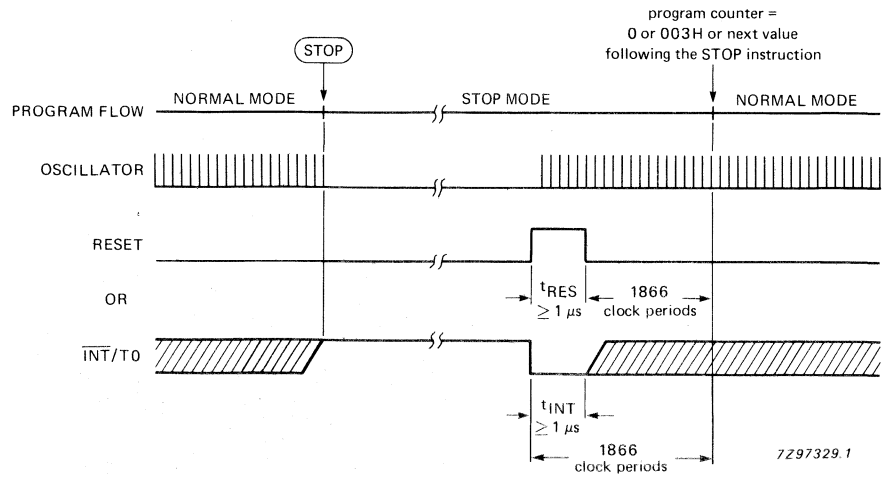


Fig. 8 Entering and exiting the STOP mode.

DEVELOPMENT DATA

FUNCTIONAL DESCRIPTION (continued)

If the microcontroller exits the STOP mode by pulling the external interrupt input pin LOW, an interrupt sequence is executed only if the external interrupt is enabled. In this event the microcontroller resumes the normal program sequence after returning from the interrupt routine, as in the normal mode. If the interrupt is not enabled, it continues the normal program sequence, executing the instruction following the STOP instruction.

The microcontroller is restarted by a LOW level applied at the $\overline{INT}$/T0 pin, and not by a HIGH-to-LOW transition as in a normal interrupt mechanism.
Note: when leaving the STOP mode with an interrupt, a further instruction in the main program series is executed prior to entering the interrupt routine.

When the $\overline{INT}$/T0 level is active during the STOP instruction then no STOP is executed.

A LOW level on the external interrupt input of at least 1 μs will cause the microcontroller to exit the STOP mode.

I/O facilities

The PCF84C85 family has 32 I/O lines arranged as:

- Port 0 parallel port of 8 lines (P0.0 to P0.7)
- Port 1 parallel port of 8 lines (P1.0 to P1.7)
- Port 2 parallel port of 1 line (P2.3)
- D port 0 parallel port of 8 lines (DP0.0-DP.7)
- D port 1 parallel port of 7 lines (DP1.0-DP1.6)

In addition to these the PCF84C43 also comprises four specialized I/O lines:

- SCLK I^2C-bus serial clock line
- SDA I^2C-bus serial data line (shared with P2.3)
- $\overline{INT}$/T0 external interrupt and test input. When used as a test input T0 can be directly tested by conditional branch instructions JT0 and JNT0
- T1 test input which can alter program sequences when tested by conditional jump instructions JT1 and JTN1. T1 also functions as an input to the 8-bit timer/event counter.

Parallel ports

All parallel ports can be used as outputs or inputs, their structure is quasi-bidirectional.
Output data written to a port is latched and remains unchanged until rewritten.
Input data is not latched and so must be present until read by an input instruction.
Input lines are fully CMOS compatible, output lines can drive one TTL or CMOS load.

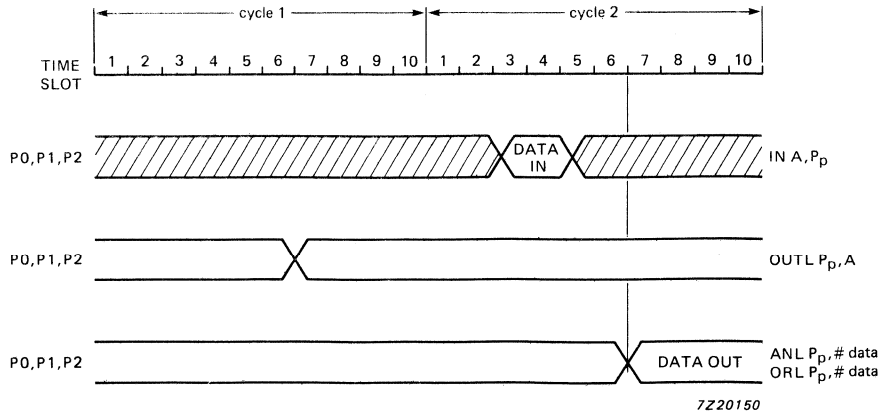


Fig. 9 Shows the timing diagram for all ports using IN, OUTL, ANL and ORL instructions. For the OUTL instruction data changes on time slot 7 of cycle 1. For the MOV, ANL and ORL instructions, the ports change on time slot 7 of cycle 2.

Fig. 10 shows the quasi-bidirectional I/O interface with push-pull output and switched pull-up current source. Each line is pulled up to V_{DD} via a constant current source (TR4), which is enabled via TR3 whenever one of the two output latches contains a logic 1. This current source is sufficient for a TTL HIGH level, yet can be pulled LOW by an external CMOS device, thus allowing the same pin to be used for both input and output.

When a logic 1 is written to the line for the first time (MQ = 1, SQ = 0), TR2 is switched on for the duration of the internal write pulse (one oscillator period), to provide a fast transition from logic 0 to logic 1. Subsequent writing of a logic 1 to the port lines will not switch TR2 on. This prevents unnecessary current through external components connected to the port lines of the same port which might be in the input mode and also connected to ground.

When a logic 0 is written to the line, TR3 switches off the current source. Current sinking capability is provided by TR1, which is now switched on. When used as an input, a logic 1 must first be written to the line, otherwise TR1 will remain low impedance.

The PCF84C85 family offers the possibility to select individually 31 of the 32 parallel port pins (not P23), by the following mask options:

Option 1 – STANDARD PORT; quasi-bidirectional I/O with switched pull-up current source of 100 μA (typ.) and P-channel booster transistor TR2.
TR2 is only active during 1 clock cycle (Fig. 10).

Option 2 – OPEN DRAIN; quasi-bidirectional I/O with only an N-channel open drain output. Application as an output requires connection of an external pull-up resistor (Fig. 11).

Option 3 – PUSH-PULL OUTPUT; drive capability of the output will be 1,6 mA (min.) at V_{DD} = 5 V in both polarities. To avoid a large current flowing through the output transistors during the input mode, these push-pull pins must only be used as outputs (Fig. 12).

DEVELOPMENT DATA

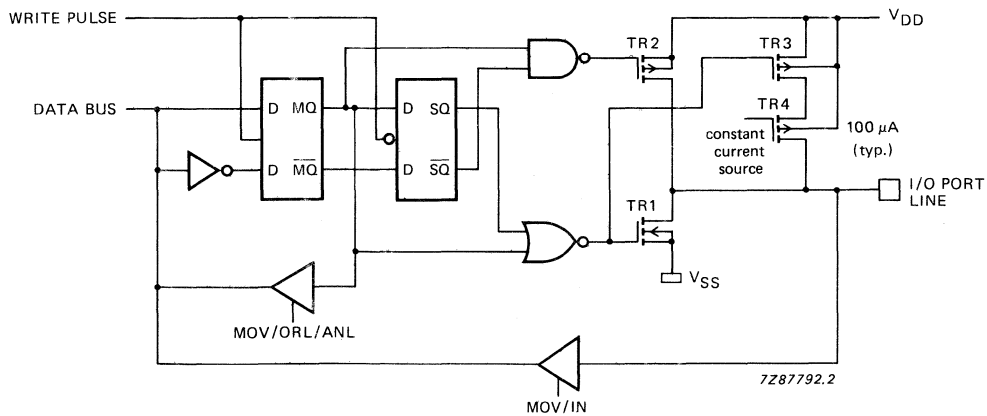


Fig. 10 Standard output with switched pull-up current source.

FUNCTIONAL DESCRIPTION (continued)

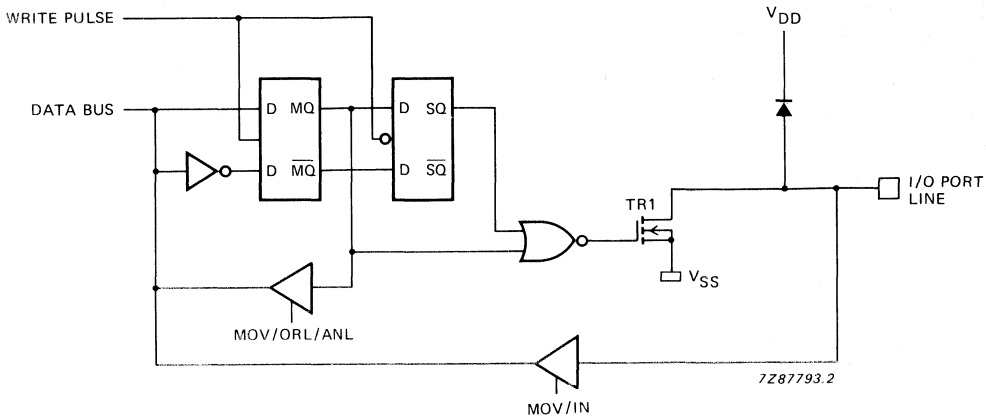


Fig. 11 Open drain output.

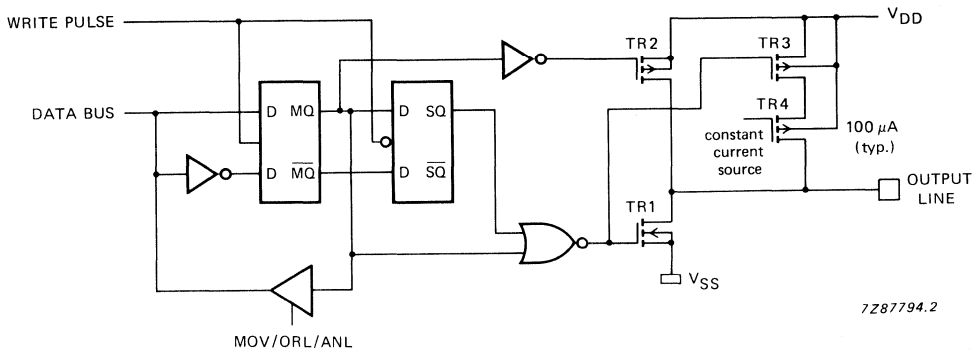


Fig. 12 Push-pull output.

Serial I/O (SIO)

The PCF84C85 has an on-chip serial I/O interface.

Whereas a normal microcontroller must regularly monitor the serial data bus for the presence of data, the serial I/O interface detects, receives and converts the serial data stream into parallel format without interrupting the execution of the current program. An interrupt is sent to the PCF84C85 only when a complete byte is received. It then reads the data byte in one instruction. Likewise during transmission the serial I/O interface performs parallel to serial conversion and subsequent serial output of the data. The microcontroller is only interrupted in the execution of its programmed tasks when a complete byte has been transmitted.

The design of the PCF84C85 serial I/O system allows any number of devices from PCF85XX family (clips) to be connected via the two-line serial bus. The ability of any devices to communicate, without interrupting the operation of any other devices on the bus, is an outstanding attribute of the system. This is achieved by allocating a specific 7-bit address to each device and providing a system whereby a device reacts only to a message prefixed with its own address or the 'general CALL' address. Address recognition is performed by the interface hardware so that operation of the microcontroller need only be interrupted when a valid address has been received. This saves significant processing time and memory space compared with a conventional microcontroller employing a software serial interface. When the addressing facility is not required, for instance in a system with only two microcontrollers, direct data transfer without addressing can be performed. In multi-master systems, an automatically invoked arbitration procedure prevents two or more devices from continuing simultaneous transmission.

In NORMAL (running) and IDLE mode, the serial I/O logic remains active; its internal system clock will be switched off when there is no activity on the serial bus.

After execution of the STOP instruction, the oscillator of the PCF84C85 is switched off. This means that the serial I/O logic will remain in the state it was at the occurance of the STOP instruction. To avoid "bus block" problems and to assure correct start-up of the bus after exit from the STOP mode, the user should disable the serial logic (ESO = 0) prior to the execution of the STOP instruction. This must be carried out only when the PCF84C85 has finished a serial data transfer.

DEVELOPMENT DATA

Serial I/O interface

Figure 13 shows the serial I/O interface. The clock line of the serial bus has exclusive use of pin 38 (SCLK) while the data line shares pin 37 (serial data) with the I/O line P23 of port 2. When the serial I/O is enabled, P23 is disabled as a parallel port line; (P23 and SCLK only open drain).

The microcontroller and interface communicate via the internal microcontroller bus and the Serial Interrupt Request line. Data and information controlling the operation of the interface are stored in four registers:

- Data shift register (S0)
- Serial I/O interface status word (S1)
- Serial clock control word (S2)
- Address register

FUNCTIONAL DESCRIPTION (continued)

Data shift register (S0)

Register S0 converts serial data to parallel format and vice versa. A pending interrupt is generated only after a complete byte has been transmitted, or after a complete data byte, specific address or 'general CALL' address has been received. The most significant bit is transmitted first.

Serial I/O interface status word (S1)

Register S1 provides information concerning the state of the interface and stores information from the microcontroller. Bits 0 to 3 are duplicated: control bits in these positions can only be written by the microcontroller, while interface bits can only be read.

MST and TRX (see Table 1)

These bits determine the operating mode of the serial I/O interface.

Table 1 Operating modes of the serial I/O interface

MST	TRX	operating mode
0	0	slave receiver
1	0	master receiver
0	1	slave transmitter
1	1	master transmitter

BB: Bus Busy.

This is the flag which indicates the status of the bus.

PIN: Pending Interrupt Not

PIN = '0' indicates the presence of a pending interrupt, which will cause a Serial Interrupt Request when the serial interrupt mechanism is enabled.

ESO: Enable Serial output

The ESO flag enables/disables the serial I/O interface: ESO = '1' enables, ESO = '0' disables. ESO can only be written by software.

BC0, BC1 and BC2

Bits BC0, BC1 and BC2 indicate the number of bits received or transmitted in a data stream. These bits can only be written by software.

AL: Arbitration Lost

The arbitration lost flag is set by hardware when the serial I/O interface, as master transmitter, loses a bus arbitration procedure.

AAS: Addressed As Slave

This flag is set by hardware when the interface detects either its own specific address or the 'general CALL' address as the first byte of a transfer and the interface has been programmed to operate in the address recognition mode.

AD0: Address Zero

This flag is set by hardware after detection of the 'general CALL' address when the interface is operating in the address recognition mode.

LRB: Last Received Bit

This contains either the last data bit received or, for a transmitting device in the acknowledgement mode, the acknowledgement signal from the receiving device.

Bits AL, AAS, AD0 and LRB can only be read by software.

Serial clock control word (S2)

Bits 0 to 4 of the clock control register S2 are used to set the frequency of the serial clock signal. When a 6 MHz crystal is used, the frequency of the serial clock can be varied between 154 kHz and 1 kHz (see Table 2). An asymmetrical clock with a HIGH-to-LOW ratio of 3 : 1 can be generated using bit 5. The asymmetrical clock allows a microcontroller more time per clock period for sampling the data line, making the timing of this action less critical. Bit 6 can be used to activate the acknowledge mode of the serial I/O. S2 is a write only register.

Address register

The address register contains the 7-bit address back-up latches and the bit (ALS) used to enable/disable the address recognition mode. The address register can be written using the MOV S0, A and MOV S0, # data instructions, but only when ES0 = '0'.

Serial I/O interrupt logic

An EN SI instruction enables and a DIS SI instruction disables the interrupt logic. When the logic is enabled, a pending interrupt results in a serial I/O interrupt to the processor, causing a CALL to location 5 in the ROM. When disabled, the presence of an interrupt is still indicated by PIN in S1, allowing the interrupt to be serviced. However, vectored interrupt will not occur.

FUNCTIONAL DESCRIPTION (continued)

Table 2 SIO clock pulse frequency control when using 6 MHz crystal

hexadecimal S20-S24 code	divisor	f_{XTAL}(6 MHz) f_{SCLK} (kHz)	f_{XTAL} (10 MHz) f_{SCLK} (kHz)
0	not allowed		
1	39	*154	*256
2	45	*133	*222
3	51	*118	*196
4	63	95	*159
5	75	80	*133
6	87	69	*115
7	99	61	*101
8	123	49	81
9	147	41	68
A	171	35	58
B	195	31	51
C	243	25	41
D	291	21	34
E	339	18	29
F	387	16	26
10	483	12	21
11	579	10	17
12	675	8,9	15
13	771	7,8	13,4
14	963	6,2	10,4
15	1155	5,2	8,7
16	1347	4,5	7,4
17	1539	3,9	6,5
18	1923	3,1	5,2
19	2307	2,6	4,3
1A	2691	2,2	3,7
1B	3075	2,0	3,3
1C	3843	1,6	2,6
1D	4611	1,3	2,2
1E	5379	1,1	1,9
1F	6147	1,0	1,6

* Not permitted for I^2C operation; the maximum clock frequency in the I^2C systems is 100 kHz.

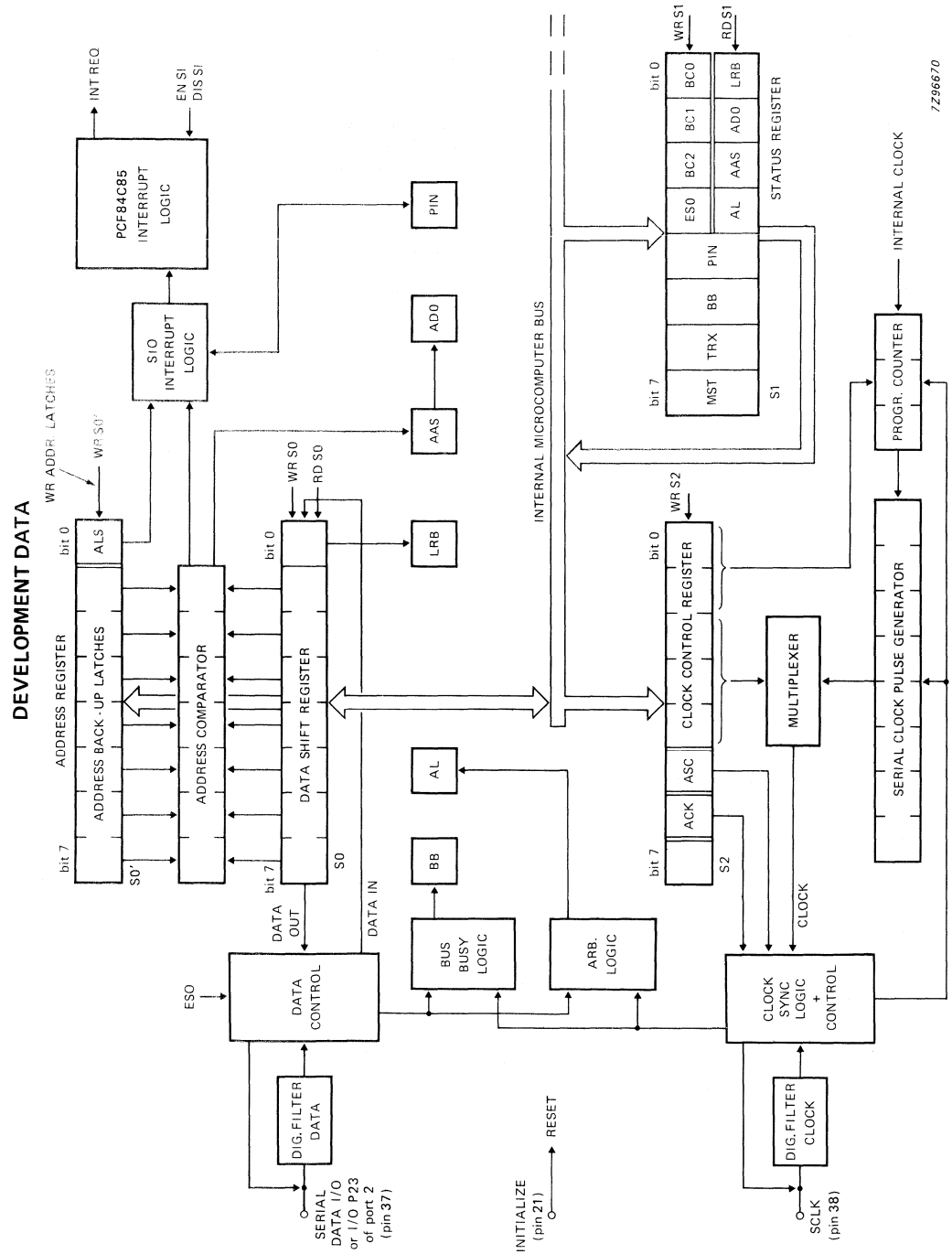


Fig. 13 Serial I/O interface.

FUNCTIONAL DESCRIPTION (continued)

Interrupts (see Fig. 14)

When the external interrupt is enabled, a HIGH-to-LOW transition on the $\overline{INT}$/T0 input initiates an external interrupt subroutine which causes a CALL to program memory location 3 following completion of the current instruction.

Serial I/O interrupt, when enabled, causes a CALL to location 5, and a timer/event counter overflow forces a CALL to location 7 when the timer interrupt is enabled.

When an interrupt subroutine starts, the contents of the program counter and bits 4, 6 and 7 of the PSW have been saved in the program counter stack. Accumulator contents have to be saved by software. Interrupt acknowledgement can be carried out by software via port pins. All interrupt subroutines must reside in memory bank 0.

Since the interrupt system is single level, once an interrupt is detected, all further interrupt requests are latched, but ignored, pending a RETR instruction to re-enable the interrupt input logic. After executing RETR, the program continues in the main part; this is independent of the occurance of a second interrupt during the running of the first routine. If 2 or 3 interrupts occur simultaneously, their priority is:

- (1) external
- (2) serial I/O
- (3) timer/event counter

An external interrupt can be generated by using the timer/counter in the event counter mode. The counter is first preset to (FFH), then EN TCNTI instruction is executed. A LOW-to-HIGH transition of the T1 input will then initiate an interrupt subroutine and cause a CALL to location 7.

On execution of a DIS I instruction, the PCF84C85 always clears the digital filter/latch and the External Interrupt Flag.

The Timer Flag (TF) is reset only when the JTF or JNTF instruction is executed or after RESET.

The Timer Interrupt Flag is set when timer overflow occurs, only if the timer interrupt is enabled.

The microcontroller will exit the IDLE mode when any one of the following three interrupts is enabled:

- External
- Serial I/O
- Timer/event counter

There is no internal pull-up or pull-down device connected to the external interrupt input (pin 1). If required pin 1 must be externally connected to a resistor ($R \leqslant 100\ k\Omega$). When the external interrupt is not used pin 1 must be connected to V_{DD}.

Improvements to interrupt and timer logic with respect to the MAB8400 family

For detailed information see the user manual "Single-chip 8-bit Microcontrollers".

DEVELOPMENT DATA

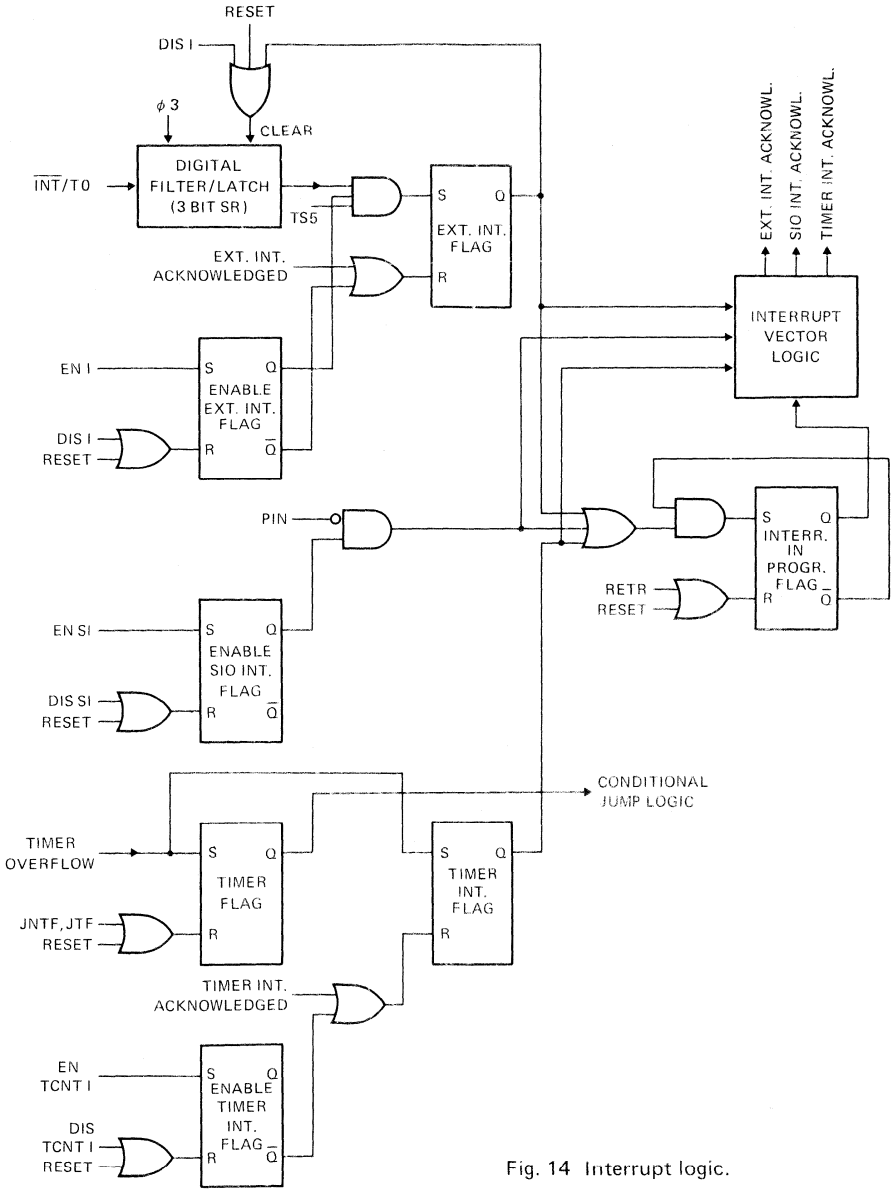


Fig. 14 Interrupt logic.

Notes to figure 14

1. $\overline{INT}$/T0 negative edge is always latched in the digital filter/latch.
2. Correct interrupt timing is ensured when INT/T0 is HIGH for $>$ 4 CP followed by a LOW for $>$ 7 CP.
3. When the interrupt in progress flag is set, further interrupts are latched but ignored, until RETR is executed.
4. A DIS I instruction always clears a pending external interrupt.
5. For all flip-flops, RESET overrules SET.

FUNCTIONAL DESCRIPTION (continued)

Oscillator (see Fig. 15)

The oscillator can be inhibited by the STOP instruction under software control. It is also inhibited when a low-supply voltage condition is present to prevent discharge of a weak back-up battery. Provided the supply voltage is within the operating range the oscillator will be restarted after a STOP instruction by a LOW level at the $\overline{INT}$/T0 pin or a HIGH level at the RESET pin.

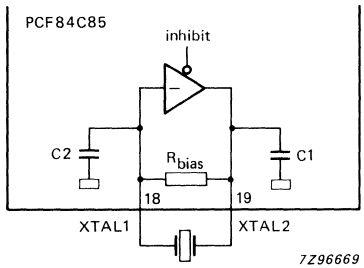


Fig. 15 Oscillator with integrated elements.

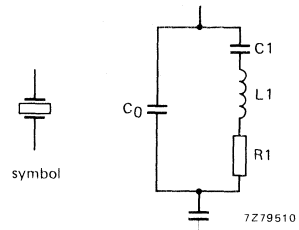


Fig. 16 Crystal unit equivalent circuit.

The values of crystal series resistance R1 and the crystal's total load capacitance C_L (C_0 + wiring + external capacitors) must not be above the curve (Fig. 17) for the corresponding frequency.
Note; if external capacitors are connected to XTAL 1 and XTAL2 they must be of equal value.

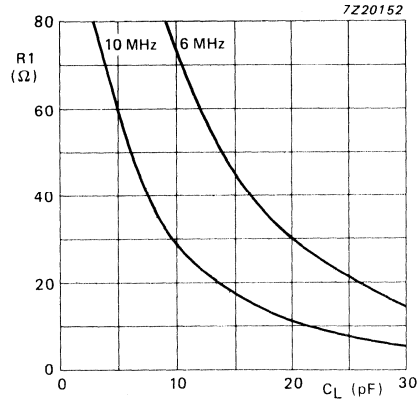


Fig. 17 Crystal circuit criteria.

The oscillator has the output drive capability via pin 19 (XTAL2). An external clock can be applied to pin 18 (XTAL1). A machine cycle consists of 10 time slots, each time slot being 3 oscillator periods.

Timer/event counter (see Fig. 18)

An internal 8-bit up-counter is provided. This can count external events, modulo-32 machine cycles, or machine cycles directly. Table 3 gives the instructions that control the counter and the prescaler, and the functions performed.

When used as a timer, the input to the counter is either the overflow or input of a 5-bit prescaler. When used as an event counter, LOW-to-HIGH transitions on pin 39 (T1) are counted. The maximum rate at which the counter may be incremented is once every machine cycle. When the counter overflows, the timer flag is set. The flag can be tested and reset using the JTF (jump is timer flag = 1) or JNTF instruction. Overflow also generates an interrupt to the processor via setting of the Timer Interrupt Flag when the timer/event counter interrupt is enabled.

Table 3 Timer/event counter control

function	timer mode modulo-1, modulo-32*	counter mode
CLEAR	MOV T,A (A) = 0 or RESET	MOV T,A (A) = 0 or RESET
PRESET	MOV T,A	MOV T,A
START	STRT T	STRT CNT
STOP	STOP TCNT or RESET	STOP TCNT or RESET
TEST	JTF/JNTF	JTF/JNTF
READ**	MOV A,T	MOV A,T

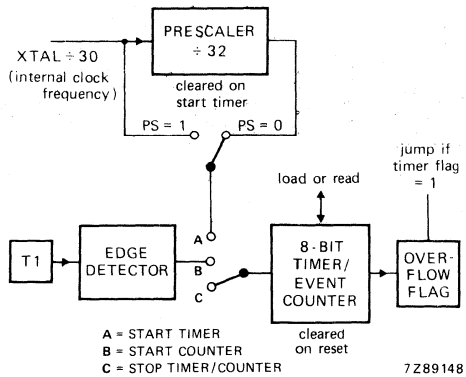


Fig. 18 Timer/event counter.

Program status word (see Fig. 19)

The program status word (PSW) is an 8-bit word (1 byte) in the CPU which stores information about the current status of the microcontroller.
The PSW bits are:

- Bits 0 to 2 — stack pointer bits (SP_0, SP_1, SP_2)
- Bit 3 — prescaler select (PS); 0 = modulo-32; 1 = modulo-1 (no prescaling)
- Bit 4 — working register bank select (RBS); 0 = register bank 0; 1 = register bank 1
- Bit 5 — not used (1)
- Bit 6 — auxiliary carry (AC); half-carry bit generated by an ADD instruction and used by the decimal adjust instruction DA A
- Bit 7 — carry (CY); the carry flag indicates that previous operation has resulted in an overflow of the accumulator.

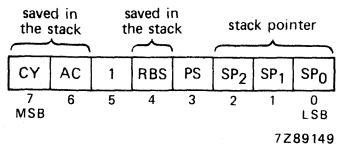


Fig. 19 Program status word.

* With prescaler select, PS = 0, the timer counts modulo-32 machine cycles, with PS = 1 it counts modulo-1 cycles (prescaler not used); prescaler cleared with STRT T, prescaler not readable.

** READ does not disturb the counting process.

FUNCTIONAL DESCRIPTION (continued)

Program status word (continued)

All bits can be read using the MOV A, PSW instruction. Bits 7 and 6 are set and cleared by CPU operation. Bit 4 can be changed by a SEL RB instruction, bit 3 by the MOV PSW, A instruction, and bits 0, 1 and 2 by the CALL, RET or RETR instructions in the event of an interrupt. Bits 7, 6 and 4 are stored in the program counter stack during subroutine and interrupt calls. These bits are restored in the PSW with a RETR (return and restore) instruction which must be used at the end of an interrupt and can be used at the end of a normal subroutine. The RET instruction has no restore feature and cannot be used at the end of an interrupt.

Program counter (see Fig. 20)

The 13-bit program counter is able to address 8 K bytes of ROM. The arrangement of the bits is shown in figure 20. During an interrupt subroutine PC_{11} and PC_{12} are forced to logic 0. All 13 bits are saved in the stack during CALL and interrupt routines.

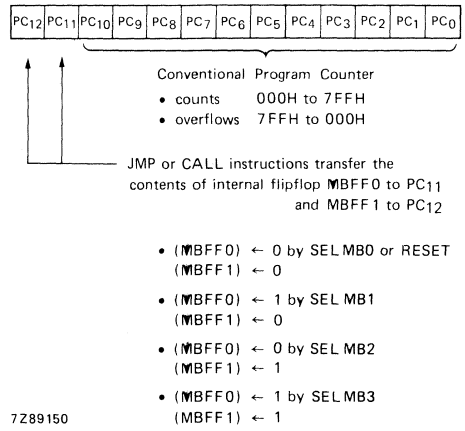


Fig. 20 Program counter.

Central processing unit

The PCF84C85 has arithmetic, logical and branching capabilities. The DA A, SWAP A and XCHD instructions simplify BCD arithmetic and the handling of nibbles. The MOVP A,@A instruction permits efficient table look-up from the current ROM page.

Conditional branch logic

The conditional branch logic within the processor enables several conditions, internal and external to the processor, to be tested by the user's program. Table 4 lists the conditional jump instructions used to change the program sequence. The DJNZ instruction decrements a designated register or data memory location and branches if the contents are not zero. This instruction is useful for looping control. The JMPP@A instruction allows multiway branches to destinations determined by the contents of the accumulator.

Table 4 Conditional branches

test	jump condition	jump instruction
accumulator	all bits zero	JZ
	any bit non-zero	JNZ
accumulator bit test	1	JB0 to JB7
carry flag	1	JC
	0	JNC
timer overflow flag	1	JTF
	0	JNTF
test input T0	1	JT0
	0	JNT0
test input T1	1	JT1
	0	JNT1
register	non-zero	DJNZ

Test input T1 (pin 39)

The T1 input line can be used as:

- A test input for branch instructions JT1 and JNT1
- An external input to the event counter

When used as a test input:

- JT1 instruction tests for logic 1 level
- JNT1 instruction tests for logic 0 level

When used as an input to the event counter, T1 must be LOW for > 4 CP, followed by a HIGH for > 4 CP. The transition can be recognized with a repetition rate of once per 30 oscillator clock periods (1 machine cycle).

There is no internal pull-up or pull-down resistor connected to the T1 input. If required it must be externally connected to a resistor ($R = \leqslant 100$ kΩ). When T1 is not used pin 39 must be connected to V_{DD} or V_{SS}.

Reset (pin 21)

A positive-going signal on the RESET input

- Sets the program counter to zero
- Selects location 0 of memory bank 0 and register bank 0
- Sets the stack pointer to zero (000); pointing to RAM address 8
- Disables the interrupts (external, timer and serial I/O)
- Stops the timer/event counter, then sets it to zero
- Sets the timer prescaler to modulo-32
- Resets the timer flag
- Sets all ports to input mode
- Sets the serial I/O to slave receiver mode and disables the serial I/O
- Cancels IDLE and STOP mode

FUNCTIONAL DESCRIPTION (continued)

Power-on-reset

The internal power-on reset circuit monitors the PCF84C85 supply voltage V_{DD}. For as long as the supply voltage remains below the internal reference level V_{ref} (typically 1,5 V) the oscillator is inhibited and RESET (pin 21) has an undefined level. When V_{DD} rises above the internal reference level, the oscillator is released and RESET is pulled high to V_{DD} by TR1 for a period t_D (typically 50 μs).

N.B. Because of the narrow bandwidth of the crystal, the start-up time of the oscillator is typically 10 ms.

Three modes of power-on reset are possible:

1. If V_{DD} can be switched on with fast rise time i.e. V_{DD} reaches its minimum operating value (corresponding to the selected oscillator frequency) before the RESET signal (t_D) has finished, then no extra components are required (see Fig. 21 and 22). Note that the first instruction is executed after the oscillator start-up time plus 1866 clock periods have elapsed.

2. If V_{DD} has a slow rise time then the RESET signal should be stretched by an external RC circuit (see Fig. 23 and 24). In the event of a short drop in the supply voltage, the diode path rapidly discharges the capacitor to ensure a reliable power-on reset. To ensure a correct reset, the RESET signal should reach at least 70% of the final value of V_{DD}. Given that the RESET voltage and V_{DD} rise exponentially, the above requirement is satisfied when the time constant τ of the RESET pulse is >8 times the time constant of V_{DD}. If V_{DD} rises linearly, then a RESET time constant >2 times the rise time of V_{DD} is required.

   When a reset is completed (RESET goes LOW) before the oscillator has started up, program execution begins after the oscillator start-up time plus 1866 clock periods have elapsed (see Fig. 24). If the oscillator is started-up prior to the completion of RESET, then program execution begins 1866 clock periods after RESET goes LOW.

3. Figure 25 shows an external reset to the PCF84C85 during power-on. The external reset signal must remain HIGH until V_{DD} has reached its minimum operating value corresponding to the selected oscillator frequency. When a reset is completed (RESET goes LOW) before the oscillator has started up, program execution begins after the oscillator start-up time plus 1866 clock periods have elapsed (see Fig. 26). If the oscillator is started-up prior to the completion of RESET, then program execution begins 1866 clock periods after RESET goes LOW.

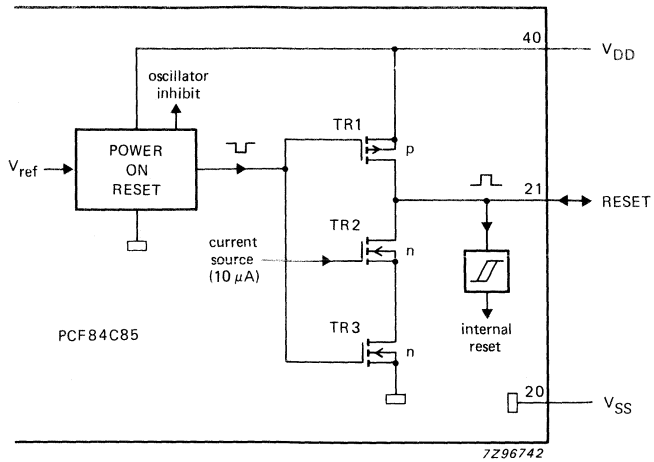


Fig. 21 Power-on-reset configuration.

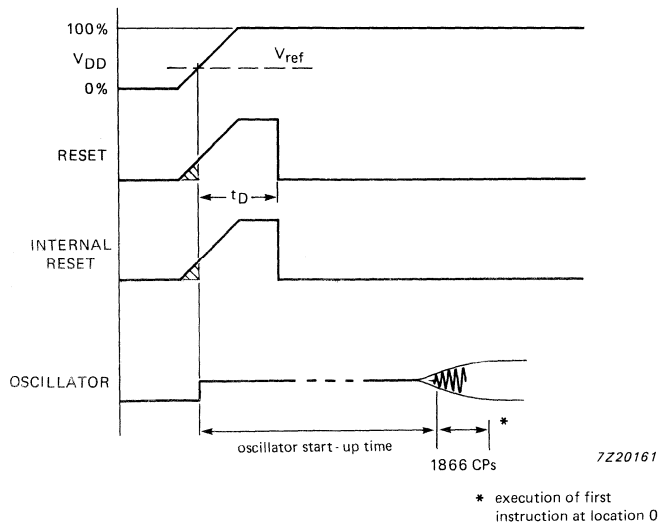


Fig. 22 Timing of power-on-reset with fast rise time.

FUNCTIONAL DESCRIPTION (continued)

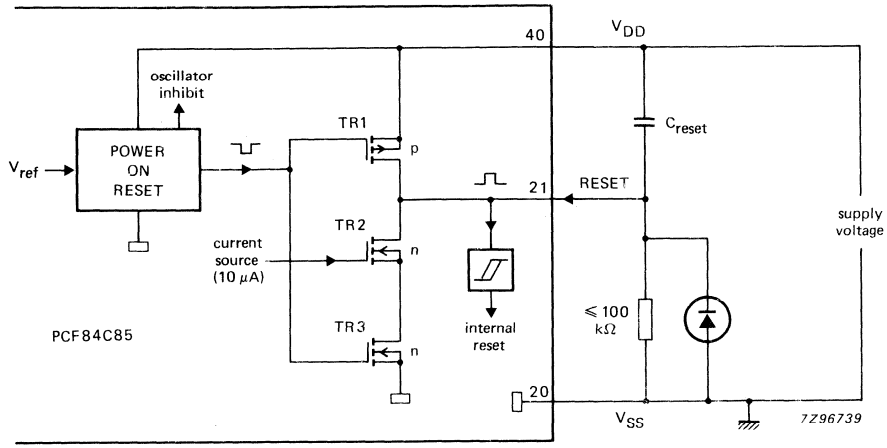


Fig. 23 Stretched power-on-reset with external components.

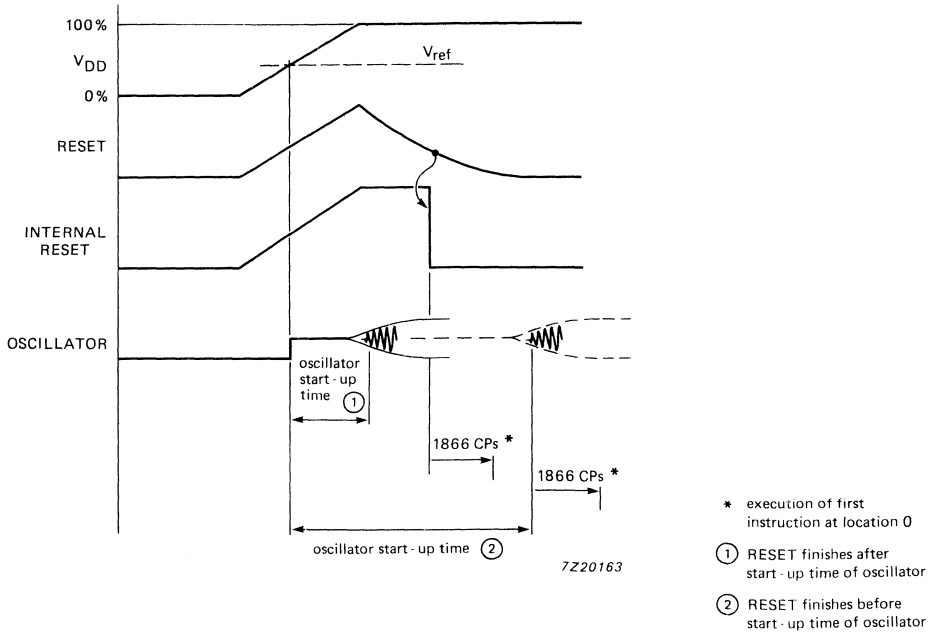


Fig. 24 Timing of power-on-reset with a slowly rising V_{DD} and a stretched RESET pulse.

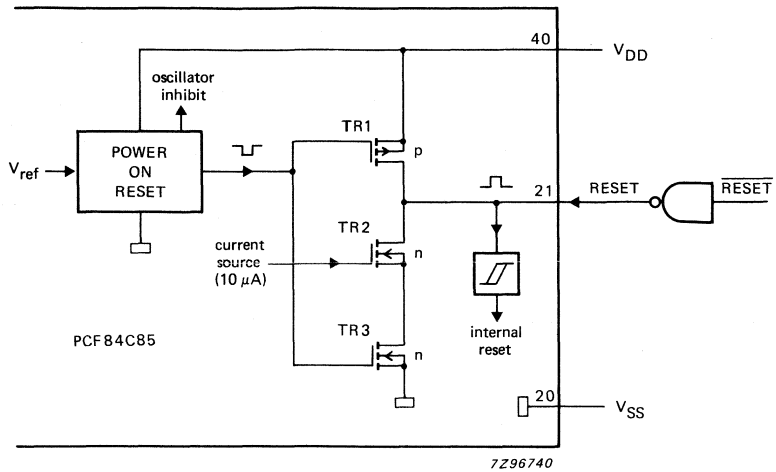


Fig. 25 External power-on-reset configuration.

DEVELOPMENT DATA

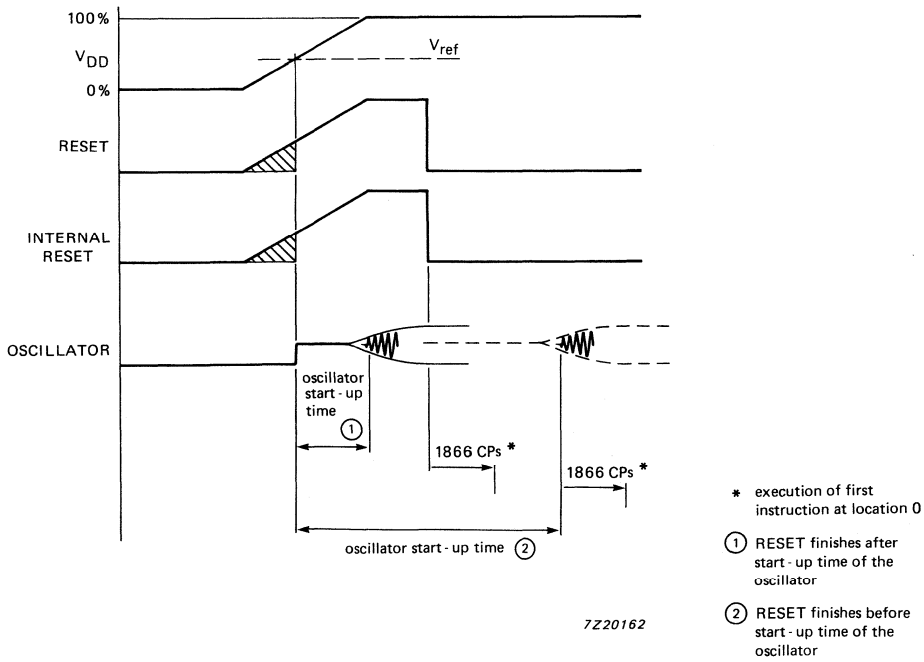


Fig. 26 Timing of external power-on-reset.

INSTRUCTION SET

The PCF84C85 instruction set consists of over 80 one and two byte instructions and is identical to the MAB8400 instruction set. New instructions are added for STOP and IDLE mode. Program code efficiency is high because all RAM locations and all ROM locations on a 256 byte page require only a single byte address.

Table 7 gives the instruction set of the PCF84C85. Table 6 shows the instruction map and Table 5 details the symbols and definition descriptions that are used.

Table 5 Symbols and definitions used in Table 7

symbol	definition description
A	accumulator
addr	program memory address
Bb	bit designation (b = 0-7)
RBS	register bank select
C	carry bit (bit CY)
CNT	event counter
Dx	Derivative register designation (x = 0,1,2 or 3)
data	8-bit number or expression
I	interrupt
MB	memory bank
MBFF	memory bank flip-flop
P	mnemonic for 'in-page' operation
PC	program counter
Pp	port designation (p = 0, 1 or 2)
PSW	program status word
RB	register bank
Rr	register designation (r = 0-7)
Sn	serial I/O register
SP	stack pointer
T	timer
TF	timer flag
T0, T1	test 0 and 1 inputs
#	immediate data prefix
@	indirect address prefix
(X)	contents of X
((X))	contents of location addressed by X
←	is replaced by
↔	is exchanged with

Table 6 PCF84C85 instruction map

first hexadecimal character of opcode ↓ / second hexadecimal character of opcode →	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	NOP	IDLE		ADD A,#data	JMP page 0	EN I	JNTF addr	DEC A	IN A,Pp				MOV A,Sn			
									0	1	2		0	1		
1	INC @Rr		JBO addr	ADDC A,#data	CALL page 0	DIS I	JTF addr	INC A	INC Rr							
	0	1							0	1	2	3	4	5	6	7
2	XCH A,@Rr		STOP	MOV A,#data	JMP page 1	EN TCNTI	JNTO addr	CLR A	XCH A,Rr							
	0	1							0	1	2	3	4	5	6	7
3	XCHD A,@Rr		JB1 addr		CALL page 1	DIS TCNTI	JTO addr	CPL A	OUTL Pp,A				MOV Sn,A			
	0	1							0	1	2		0	1	2	
4	ORL A,@Rr		MOV A,T	ORL A,#data	JMP page 2	STRT CNT	JNT1 addr	SWAP A	ORL A,Rr							
	0	1							0	1	2	3	4	5	6	7
5	ANL A,@Rr		JB2 addr	ANL A,#data	CALL page 2	STRT T	JT1 addr	DA A	ANL A,Rr							
	0	1							0	1	2	3	4	5	6	7
6	ADD A,@Rr		MOV T,A		JMP page 3	STOP TCNT		RRC A	ADD A,Rr							
	0	1							0	1	2	3	4	5	6	7
7	ADDC A,@Rr		JB3 addr		CALL page 3			RR A	ADDC A,Rr							
	0	1							0	1	2	3	4	5	6	7
8				RET	JMP page 4	EN SI			ORL Pp,#data				MOV A,Dx	MOV Dx,A	ANL Dx,A	ORL Dx,A
									0	1	2					
9			JB4 addr	RETR	CALL page 4	DIS SI	JNZ addr	CLR C	ANL Pp,#data				MOV Sn,#data			
									0	1	2		0	1	2	
A	MOV @Rr,A			MOVP A,@A	JMP page 5	SEL MB2		CPL C	MOV Rr,A							
	0	1							0	1	2	3	4	5	6	7
B	MOV @Rr,#data		JB5 addr	JMPP @A	CALL page 5	SEL MB3			MOV Rr,#data							
	0	1							0	1	2	3	4	5	6	7
C	DEC @Rr				JMP page 6	SEL RB0	JZ addr	MOV A,PSW	DEC Rr							
	0	1							0	1	2	3	4	5	6	7
D	XRL A,@Rr		JB6 addr	XRL A,#data	CALL page 6	SEL RB1		MOV PSW,A	XRL A,Rr							
	0	1							0	1	2	3	4	5	6	7
E	DJNZ @Rr,addr				JMP page 7	SEL MB0	JNC addr	RL A	DJNZ Rr, addr							
	0	1							0	1	2	3	4	5	6	7
F	MOV A,@Rr		JB7 addr		CALL page 7	SEL MB1	JC addr	RLC A	MOV A,Rr							
	0	1							0	1	2	3	4	5	6	7

INSTRUCTION SET (continued)

Table 7 Instruction set

	mnemonic	opcode (hex.)	bytes/ cycles	description	function		notes
ACCUMULATOR	ADD A, Rr	6*	1/1	Add register contents to A	(A)←(A) + (Rr)	r = 0–7	1
	ADD A, @Rr	60 61	1/1	Add RAM data, addressed by Rr, to A	(A)←(A) + ((R0)) (A)←(A) + ((R1))		1
	ADD A, #data	03 data	2/2	Add immediate data to A	(A)←(A) + data		1
	ADDC A, Rr	7*	1/1	Add carry and register contents to A	(A)←(A) + (Rr) + (C)	r = 0–7	1
	ADDC A, @Rr	70 71	1/1	Add carry and RAM data, addressed by Rr, to A	(A)←(A) + ((R0)) + (C) (A)←(A) + ((R1)) + (C)		1
	ADDC A, #data	13 data	2/2	Add carry and immediate data to A	(A)←(A) + data + (C)		1
	ANL A, Rr	5*	1/1	'AND' Rr with A	(A)←(A) AND (Rr)	r = 0–7	
	ANL A, @Rr	50 51	1/1	'AND' RAM data, addressed by Rr, with A	(A)←(A) AND ((R0)) (A)←(A) AND ((R1))		
	ANL A, #data	53 data	2/2	'AND' immediate data with A	(A)←(A) AND data		
	ORL A, Rr	4*	1/1	'OR' Rr with A	(A)←(A) OR (Rr)	r = 0–7	
	ORL A, @Rr	40 41	1/1	'OR' RAM data, addressed by Rr, with A	(A)←(A) OR ((R0)) (A)←(A) OR ((R1))		
	ORL A, #data	43 data	2/2	'OR' immediate data with A	(A)←(A) OR data		
	XRL A, Rr	D*	1/1	'XOR' Rr with A	(A)←(A) XOR (Rr)	r = 0–7	
	XRL A, @Rr	D0 D1	1/1	'XOR' RAM, addressed by Rr, with A	(A)←(A) XOR ((R0)) (A)←(A) XOR ((R1))		
	XRL A, #data	D3 data	2/2	'XOR' immediate data with A	(A)←(A) XOR data		
	INC A	17	1/1	increment A by 1	(A)←(A) + 1		
	DEC A	07	1/1	decrement A by 1	(A)←(A) −1		
	CLR A	27	1/1	clear A to zero	(A)←0		
	CPL A	37	1/1	one's complement A	(A)←NOT(A)		
	RL A	E7	1/1	rotate A left	$(A_{n+1})\leftarrow(A_n)$ $(A_0)\leftarrow(A_7)$	n = 0–6	

ACCUMULATOR (cont.)	RLC A	F7	1/1	rotate A left through carry	$(A_{n+1}) \leftarrow A_n$ $(A_0) \leftarrow (C), (C) \leftarrow (A_7)$	n = 0–6	2
	RR A	77	1/1	rotate A right	$(A_n) \leftarrow (A_{n+1})$ $(A_7) \leftarrow (A_0)$	n = 0–6	
	RRC A	67	1/1	rotate A right through carry	$(A_n) \leftarrow (A_{n+1})$ $(A_7) \leftarrow (C), (C) \leftarrow (A_0)$	n = 0–6	2
	DA A	57	1/1	decimal adjust A			2
	SWAP A	47	1/1	swap nibbles of A	$(A_{4-7}) \leftrightarrow (A_{0-3})$		
DATA MOVES	MOV A, Rr	F*	1/1	move register contents to A	(A)←(Rr)	r = 0–7	
	MOV A, @Rr	F0 F1	1/1	move RAM data, addressed by Rr, to A	(A)←((R0)) (A)←((R1))		
	MOV A, #data	23 data	2/2	move immediate data to A	(A)←data		
	MOV Rr, A	A*	1/1	move accumulator contents to register	(Rr)←(A)	r = 0–7	
	MOV @Rr, A	A0 A1	1/1	move accumulator contents to RAM location addressed by Rr	((R0))←(A) ((R1))←(A)		
	MOV Rr, #data	B* data	2/2	move immediate data to Rr	(Rr)←data		
	MOV @Rr, #data	B0 data B1 data	2/2	move immediate data to RAM location addressed by Rr	((R0))←data ((R1))←data		
	XCH A, Rr	2*	1/1	exchange accumulator contents with Rr	(A)↔(Rr)	r = 0–7	
	XCH A, @Rr	20 21	1/1	exchange accumulator contents with RAM data addressed by Rr	(A)↔((R0)) (A)↔((R1))		
	XCHD A, @Rr	30 31	1/1	exchange lower nibbles of A and RAM data addressed by Rr	$(A_{0-3}) \leftrightarrow ((R0_{0-3}))$ $(A_{0-3}) \leftrightarrow ((R1_{0-3}))$		
	MOV A, PSW	C7	1/1	move PSW contents to accumulator	(A)←(PSW)		
	MOV PSW, A	D7	1/1	move accumulator bit 3 to PSW_3	$(PSW_3) \leftarrow (A_3)$		3
	MOVP A, @A	A3	1/2	move indirectly addressed data in current page to A	$(PC_{0-7}) \leftarrow (A), (A) \leftarrow ((PC))$		
FLAGS	CLR C	97	1/1	clear carry bit	(C)←0		2
	CPL C	A7	1/1	complement carry bit	(C)←NOT(C)		2

INSTRUCTION SET (continued)

	mnemonic	opcode (hex.)	bytes/ cycles	description	function		notes
REGISTER	INC Rr	1*	1/1	increment register by 1	(Rr)←(Rr) + 1	r = 0–7	
	INC @Rr	10 11	1/1	increment RAM data, addressed by Rr, by 1	((R0))←((R0)) + 1 ((R1))←((R1)) + 1		
	DEC Rr	C*	1/1	decrement register by 1	(Rr)←(Rr) – 1	r = 0–7	
	DEC @Rr	C0 C1	1/1	decrement RAM data, addressed by Rr, by 1	((R0))←((R0)) – 1 ((R1))←((R1)) – 1		
BRANCH	JMP addr	● 4 address	2/2	unconditional jump within a 2 K bank	(PC_{8-10})←$addr_{8-10}$ (PC_{0-7})←$addr_{0-7}$ (PC_{11-12})←MBFF 0–1		
	JMPP @A	B3	1/2	indirect jump within a page	(PC_{0-7})←((A))		
	DJNZ Rr, addr	E* address	2/2	decrement Rr by 1 and jump if not zero to addr	(Rr)←(Rr) – 1 if (Rr) not zero (PC_{0-7})←addr	r = 0–7	
	DJNZ @Rr, addr	E0 address	2/2	decrement RAM data, addressed by Rr by 1 and jump if not zero to addr	((R0))←((R0)) – 1 if ((R0)) not zero (PC_{0-7})←addr		
		E1 address			((R1))←((R1)) – 1 if ((R1)) not zero (PC_{0-7})←addr		
	JBb addr	▲ 2 address	2/2	jump to addr if Acc. bit b = 1	if b = 1 : (PC_{0-7})←addr	b = 0–7	
	JC addr	F6 address	2/2	jump to addr if C = 1	if C = 1 : (PC_{0-7})←addr		
	JNC addr	E6 address	2/2	jump to addr if C = 0	if C = 0 : (PC_{0-7})←addr		
	JZ addr	C6 address	2/2	jump to addr if A = 0	if A = 0 : (PC_{0-7})←addr		
	JNZ addr	96 address	2/2	jump to addr if A is NOT zero	if A≠0 : (PC_{0-7})←addr		
	JT0 addr	36 address	2/2	jump to addr if T0 = 1	if T0 = 1: (PC_{0-7})←addr		
	JNT0 addr	26 address	2/2	jump to addr if T0 = 0	if T0 = 0: (PC_{0-7})←addr		
	JT1 addr	56 address	2/2	jump to addr if T1 = 1	if T1 = 1: (PC_{0-7})←addr		
	JNT1 addr	46 address	2/2	jump to addr if T1 = 0	if T1 = 0: (PC_{0-7})←addr		
	JTF addr	16 address	2/2	jump to addr if Timer Flag = 1	if TF = 1: (PC_{0-7})←addr		4
	JNTF addr	06 address	2/2	jump to addr if Timer Flag = 0	if TF = 0: (PC_{0-7})←addr		

TIMER/EVENT COUNTER	MOV A, T	42	1/1	move timer/event counter contents to accumulator	(A)←(T)	
	MOV T, A	62	1/1	move accumulator contents to timer/event counter	(T)←(A)	
	STRT CNT	45	1/1	start event counter		
	STRT T	55	1/1	start timer		
	STOP TCNT	65	1/1	stop timer/event counter		
	EN TCNTI	25	1/1	enable timer/event counter interrupt		
	DIS TCNTI	35	1/1	disable timer/event counter interrupt		
CONTROL	EN I	05	1/1	enable external interrupt		
	DIS I	15	1/1	disable external interrupt		
	SEL RB0	C5	1/1	select register bank 0	(RBS)←0	5
	SEL RB1	D5	1/1	select register bank 1	(RBS)←1	5
	SEL MB0	E5	1/1	select program memory bank 0	(MBFF0)←0, (MBFF1)←0	
	SEL MB1	F5	1/1	select program memory bank 1	(MBFF0)←1, (MBFF1)←0	
	SEL MB2	A5	1/1	select program memory bank 2	(MBFF0)←0, (MBFF1)←1	
	SEL MB3	B5	1/1	select program memory bank 3	(MBFF0)←1, (MBFF1)←1	
	STOP	22	1/1	enter STOP mode		
	IDLE	01	1/1	enter IDLE mode		
SUBROUTINE	CALL addr	▲ 4 address	2/2	jump to subroutine	((SP))←(PC), ($PSW_{4,6,7}$) 6 (SP)←(SP) + 1 (PC_{8-10})←$addr_{8-10}$ (PC_{0-7})←$addr_{0-7}$ (PC_{11-12})←MBFF 0–1	6
	RET	83	1/2	return from subroutine	(SP)←(SP) – 1 (PC)←((SP))	6
	RETR	93	1/2	return from interrupt and restore bits 4, 6, 7 of PSW	(SP)←(SP) – 1 ($PSW_{4,6,7}$) + (PC)←((SP))	6

INSTRUCTION SET (continued)

	mnemonic	opcode (hex.)	bytes/ cycles	description	function	notes
PARALLEL INPUT/OUTPUT	IN A, Pp	08 09 0A	1/2	input port p data to accumulator	(A)←(P0) (A)←(P1) (A)←(P2)	 7
	OUTL Pp, A	38 39 3A	1/2	output accumulator data to port p	(P0)←(A) (P1)←(A) (P2)←(A)	
	ANL Pp, #data	98 data 99 data 9A data	2/2	AND port p data with immediate data	(P0)←(P0) AND data (P1)←(P1) AND data (P2)←(P2) AND data	
	ORL Pp, #data	88 data 89 data 8A data	2/2	OR port p data with immediate data	(P0)←(P0) OR data (P1)←(P1) OR data (P2)←(P2) OR data	
DERIVATIVE INPUT/OUTPUT	MOV A, Dx	8C 00 8C 01	2/2 2/2	input pin data of port DP0, DP1 to accumulator	(A)←(D0) (A)←(D1)	 8
	MOV Dx, A	8D 02 8D 03	2/2 2/2	move contents of accumulator to latch of port DP0, DP1	(D2)←(A) (D3)←(A)	
	ANL Dx, A	8E 02 8E 03	2/2 2/2	AND contents of DP0, DP1 latch with accumulator	(D2)←(D2) AND (A) (D3)←(D3) AND (A)	
	ORL Dx, A	8F 02 8F 03	2/2 2/2	OR contents of DP0, DP1 latch with accumulator	(D2)←(D2) OR (A) (D3)←(D3) OR (A)	
	MOV A, Dx	8C 02 8C 03	2/2 2/2	move contents of DP0, DP1 latch to accumulator	(A)←(D2) (A)←(D3)	 8

	mnemonic	opcode (hex.)	bytes/ cycles	description	function	notes
SERIAL INPUT/OUTPUT	MOV A, S_n	0C 0D	1/2	move serial I/O register contents to accumulator	(A)←(S0) (A)←(S1)	9
	MOV S_n, A	3C 3D 3E	1/2	move accumulator contents to serial I/O register	(S0)←(A) (S1)←(A) (S2)←(A)	
	MOV S_n, #data	9C data 9D data 9E data	2/2	move immediate data to serial I/O register	(S0)←data (S1)←data (S2)←data	
	EN SI	85	1/1	enable serial I/O interrupt		
	DIS SI	95	1/1	disable serial I/O interrupt		
	NOP	00	1/1	no operation		

Notes to Table 8

1. PSW CY, AC affected
2. PSW CY affected
3 PSW PS affected
4. Execution of JTF and JNTF instructions resets the Timer Flag (TF).

* : 8,9,A,B,C,D,E,F
● : 0,2,4,6,8,A,C,E
▲ : 0,3,5,7,9,B,D,F

5. PSW RBS affected
6. PSW SP_0, SP_1, SP_2 affected
7. (A) = 0000 (P23) 111
8. The MSB of A becomes a logic 0
9. (S1) has a different function in read and write operations, see serial I/O interface.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 40)	V_{DD}	−0,8 to +8	V
All input voltages	V_I	−0,8 to V_{DD} +0,8	V
D.C. current into any input or output	$\pm I_I$, $\pm I_O$ max.	10	mA
Total power dissipation			
Power dissipation per output			
except P23, SCLK	P_O max.	50	mW
P23, SCLK	P_O max.	180	mW
Storage temperature range	T_{stg}	−65 to +150	°C
Operating ambient temperature range	T_{amb}	−40 to +85	°C
Operating junction temperature	T_j max.	125	°C

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see 'Handling MOS devices').

DEVELOPMENT DATA

D.C. CHARACTERISTICS

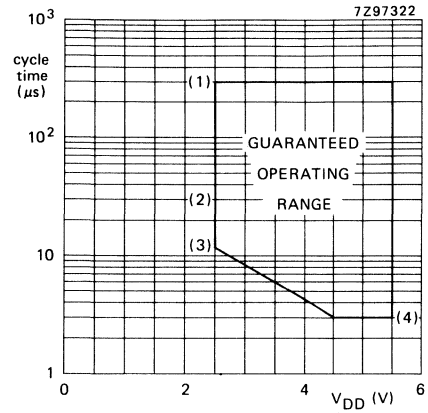
V_{DD} = 2,5 to 5,5 V; V_{SS} = 0 V; T_{amb} = −40 to + 85 °C; all voltages with respect to V_{SS}; unless otherwise specified.

parameter	symbol	min.	typ.	max.	unit
Supply voltage					
operating (see Fig. 27)	V_{DD}	2,5	–	5,5	V
Supply current					
operating (see Fig. 28)					
at V_{DD} = 5 V; f_{XTAL} = 10 MHz	I_{DD}	–	1,6	3,2	mA
at V_{DD} = 5 V; f_{XTAL} = 6 MHz	I_{DD}	–	1	2	mA
at V_{DD} = 3 V; f_{XTAL} = 3,58 MHz	I_{DD}	–	0,5	0,6	mA
IDLE mode (see Fig. 29)					
at V_{DD} = 5 V; f_{XTAL} = 10 MHz	I_{DD}	–	0,8	1,6	mA
at V_{DD} = 5 V; f_{XTAL} = 6 MHz	I_{DD}	–	1	1	mA
at V_{DD} = 3 V; f_{XTAL} = 3,58 MHz	I_{DD}	–	0,25	0,4	mA
STOP mode (see Fig. 35 and note 1)					
at V_{DD} = 2,5 V; T_{amb} = 25 °C	I_{DD}	–	1,2	2,5	μA
at V_{DD} = 2,5 V; T_{amb} = 70 °C	I_{DD}	–	–	10	μA
Inputs					
Input voltage LOW	V_{IL}	0	–	$0,3V_{DD}$	V
Input voltage HIGH	V_{IH}	$0,7V_{DD}$	–	V_{DD}	V
Input leakage current					
as $V_{SS} < V_I < V_{DD}$	$\pm I_{IL}$	–	–	1	μA
Outputs					
Output voltage LOW					
at V_I = V_{SS} or V_{DD}; $\|I_O\| < 1$ μA	V_{OL}	–	–	0,05	V
Output sink current LOW					
at V_{DD} = 5 V ± 10%; V_O = 0,4 V					
except P23/SDA, SCLK (see Fig. 31)	I_{OL}	1,6	3	–	mA
P23/SDA, SCLK (see Fig. 32)	I_{OL}	3	–	–	mA
Pull-up output source current HIGH (see Fig. 33)					
at V_{DD} = 5 V ± 10%; V_O = $0,7V_{DD}$	$-I_{OH}$	40	–	–	μA
at V_{DD} = 5 V ± 10%; V_O = V_{SS}	$-I_{OH}$	–	–	400	μA
Push-pull output source current HIGH					
at V_{DD} = 5 V ± 10%; V_O = V_{DD}−0,4 V	$-I_{OH}$	1,6	3	–	mA

Note 1

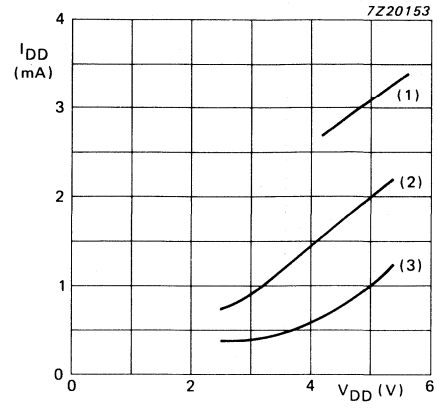
Crystal connected between XTAL1 and XTAL2; SCL and SDA pulled to V_{DD} via 5,6 kΩ resistor; T1 at V_{SS}, $\overline{INT}$ at V_{DD}.

A.C. CHARACTERISTICS (continued)



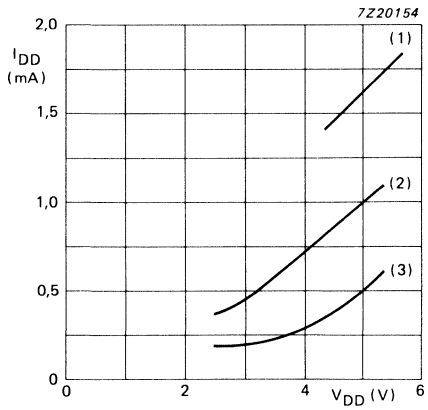
(1) clock frequency = 100 kHz
(2) clock frequency = 1 MHz
(3) clock frequency = 3 MHz
(4) clock frequency = 10 MHz

Fig. 27 Maximum clock frequency (f_{XTAL}) as a function of the supply voltage (V_{DD}).



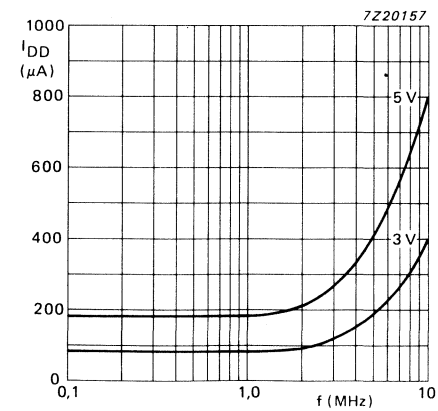
(1) clock frequency = 10 MHz
(2) clock frequency = 6 MHz
(3) clock frequency = 3,58 MHz

Fig. 28 Maximum supply current (I_{DD}) in operating mode as a function of the supply voltage.



(1) clock frequency = 10 MHz
(2) clock frequency = 6 MHz
(3) clock frequency = 3,58 MHz

Fig. 29 Maximum supply current (I_{DD}) in IDLE mode as a function of the supply voltage (V_{DD}).



(1) V_{DD} = 3 V
(2) V_{DD} = 5 V

Fig. 30 Typical supply current during IDLE mode as a function of frequency.

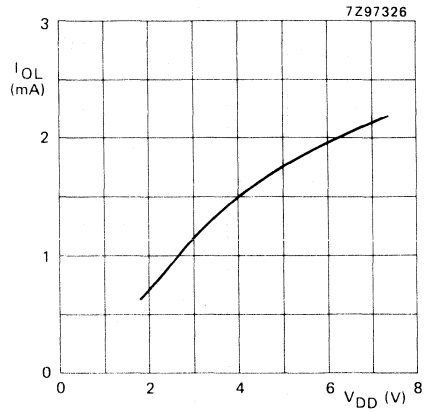


Fig. 31 Output sink current LOW (I_{OL}), except outputs P23/SDA and SCLK, as a function of supply voltage (V_{DD}); V_O = 0,4 V.

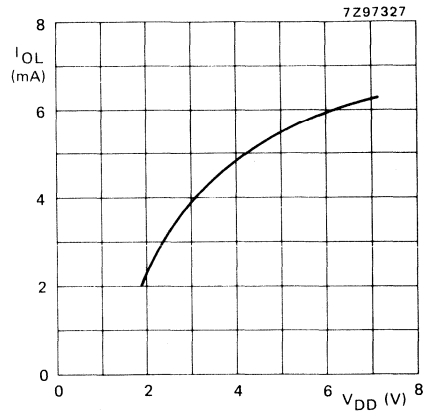
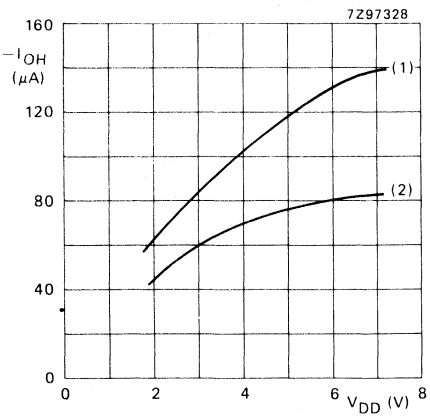


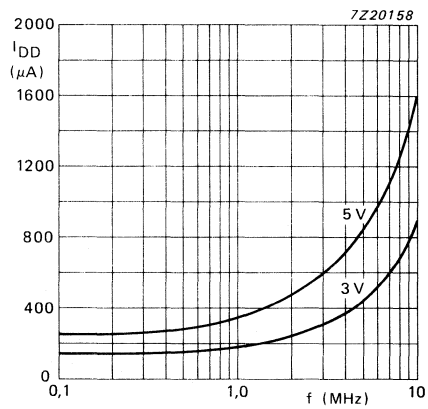
Fig. 32 Output current LOW (I_{OL}), outputs P23/SDA and SCLK, as a function of supply voltage (V_{DD}); V_O = 0,4 V.

DEVELOPMENT DATA



(1) $V_O = V_{SS}$
(2) $V_O = 0,7\ V_{DD}$

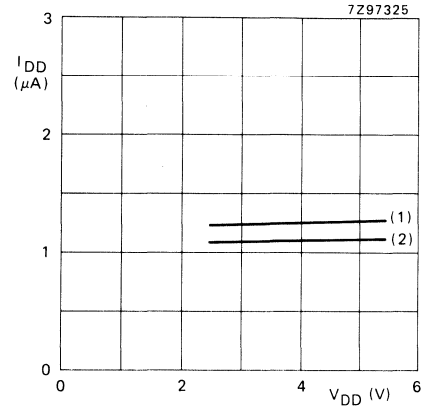
Fig. 33 Output source current HIGH ($-I_{OH}$) as a function of supply voltage (V_{DD}).



(1) V_{DD} = 3 V
(2) V_{DD} = 5 V

Fig. 34 Typical supply current during operating mode as a function of frequency.

A.C. CHARACTERISTICS (continued)



(1) T_{amb} = 85 °C
(2) T_{amb} = 25 °C

Fig. 35 Typical supply current (I_{DD}) in STOP mode as a function of the supply voltage (V_{DD}).

Table 8 Input timing shown in figure 36.

symbol	timing
t_{BUF}	$\geqslant 14t_{XTAL}$
$t_{HD;STA}$	$\geqslant 14t_{XTAL}$
t_{HIGH}	$\geqslant 17t_{XTAL}$
t_{LOW}	$\geqslant 17t_{XTAL}$
$t_{SU;STO}$	$\geqslant 14t_{XTAL}$
$t_{HD;DAT}$	> 0
$t_{SU;DAT}$	$\geqslant 250$ ns
t_{RD}	$\leqslant 1$ μs
t_{RC}	$\leqslant 1$ μs
t_{FD}	$\leqslant 1$ μs
t_{FC}	$\leqslant 0{,}3$ μs

Notes to Table 8

t_{XTAL} = one period of the XTAL input frequency (f_{XTAL})
= 167 ns for f_{XTAL} = 6 MHz.
These figures apply to all modes.

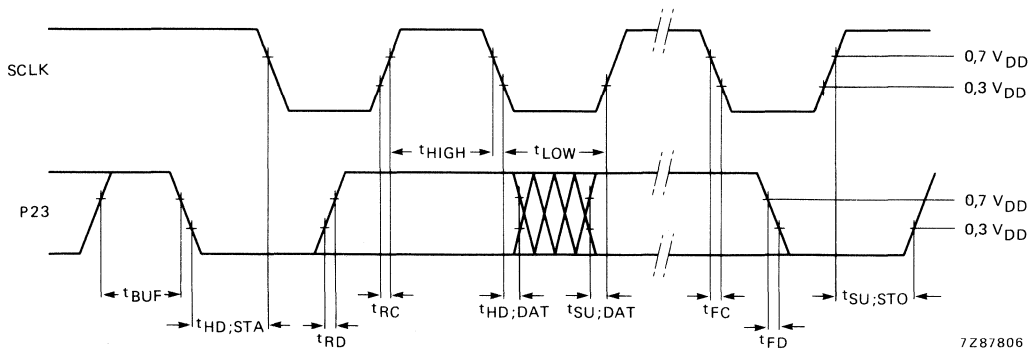


Fig. 36 PCF84C85 timing requirements for the P23 and SCLK *input* signals.

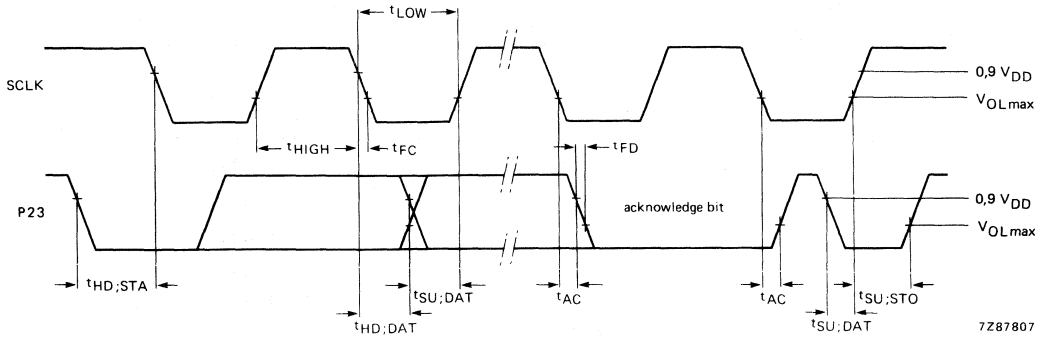


Fig. 37 PCF84C85 timing requirements for the P23 and SCLK *output* signals.

Table 9 Output timing shown in Figure 37

symbol	timing	
	normal mode (ASC in S2 = 0)	low-speed mode (ASC in S2 = 1)
$t_{HD;STA}$	½ (DF + 9) t_{XTAL}	¾ (DF + 9) t_{XTAL}
t_{HIGH}	½ (DF) t_{XTAL}	¾ (DF) t_{XTAL}
t_{LOW}	½ (DF) t_{XTAL}	¼ (DF) t_{XTAL}
$t_{SU;STO}$	½ (DF − 3) t_{XTAL}	¼ (DF − 3) t_{XTAL}
$t_{HD;DAT}$ (slave transmitter)		
any DF	$\geqslant 9t_{XTAL}$ $\leqslant 12t_{XTAL}$	$\geqslant 9t_{XTAL}$ $\leqslant 12t_{XTAL}$
$t_{HD;DAT}$ (master transmitter)		
for DF $\leqslant$ 51	$\geqslant 9t_{XTAL}$ $\leqslant 12t_{XTAL}$	– –
for DF $\leqslant$ 99	– –	$\geqslant 9t_{XTAL}$ $\leqslant 12t_{XTAL}$
$t_{SU;DAT}$ (master transmitter)		
for DF > 51	$\geqslant 15t_{XTAL}$ $\leqslant 24t_{XTAL}$	– –
for DF > 99	– –	$\geqslant 15t_{XTAL}$ $\leqslant 24t_{XTAL}$
t_{AC}	$\geqslant 9t_{XTAL}$ $\leqslant 12t_{XTAL}$	$\geqslant 9t_{XTAL}$ $\leqslant 12t_{XTAL}$
t_{FD}, t_{FC}	$\leqslant$ 100 ns at C_b = 400 pF	$\leqslant$ 100 ns at C_b = 400 pF

Notes to Table 9

t_{XTAL} = one period of the XTAL input frequency (f_{XTAL})
= 167 ns for f_{XTAL} = 6 MHz.
DF = divisor (see Table 2 Serial I/O section).
C_b = the maximum bus capacitance for each line.

DEVELOPMENT DATA

16/32-BIT MICROPROCESSOR

GENERAL DESCRIPTION

The 68070 is a highly integrated 16/32-bit central processing unit for use in a large variety of applications and is fully software compatible with the 68000. Integrating standard as well as advanced peripheral functions on the 68070 (housed in an 84-pin package), dramatically reduces system cost.

This document gives an overview of the basic functions, internal structure, and d.c. and a.c. characteristics. For further detail on the features and operation of 68070, refer to "User manual SCC68070" (Hardware and Software).

FEATURES

- **CHMOS technology**
- **32-bit internal structure**
- **Enhanced bus error handling**
- **84-pin package**
- **4 decoded interrupt inputs**
- **2 programmable interrupt inputs**
- **Decoded interrupt acknowledge**
- **Built-in clock generator: max. 20 MHz crystal**
- **On-chip MMU, supporting virtual memory**
- **2-channel DMA controller**
- **I^2C serial bus interface**
- **UART serial interface**
- **16-bit timer/counter**
- **Two 16-bit match/count/capture registers**

- **Full 68000 software compatibility**
- **68000-compatible bus interface (10 MHz)**
- **56 powerful instruction types**
- **5 basic data types**
- **16 Mbyte addressing range**
- **14 addressing modes**
- **Memory mapped I/O**
- **Vectored and auto-vectored interrupts**
- **7 interrupt levels**
- **Maximum internal clock frequency: 10 MHz**

The internal architecture of the 68070 is built around a bus interconnecting the CPU and the various on-chip peripheral functions. Each function has several dedicated connections to the external circuitry. The 68070 includes powerful programmable interrupt processing circuitry for interrupts generated by internal and external sources. An on-chip clock generator provides a 10 MHz clock signal for CPU and peripheral interfaces.

If enabled, the on-chip MMU takes care of address translation and memory protection. Two DMA channels increase data throughput and the I^2C-bus interface allows easy and low-cost addition of peripherals (master and slave devices). The 68070 also includes a UART interface. A built-in Timer/counter with two independently programmable MATCH/COUNT/CAPTURE registers means that the 68070 can be programmed with two of the following options simultaneously:

- pulse generator;
- external event counter;
- reference timer.

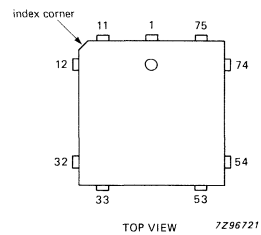


Fig.1 Pin configuration.

ORDERING INFORMATION

type number	temperature range	clock frequency	package
SCC68070CAA84	0 to 70°C	10 MHz	84-pin PLCC

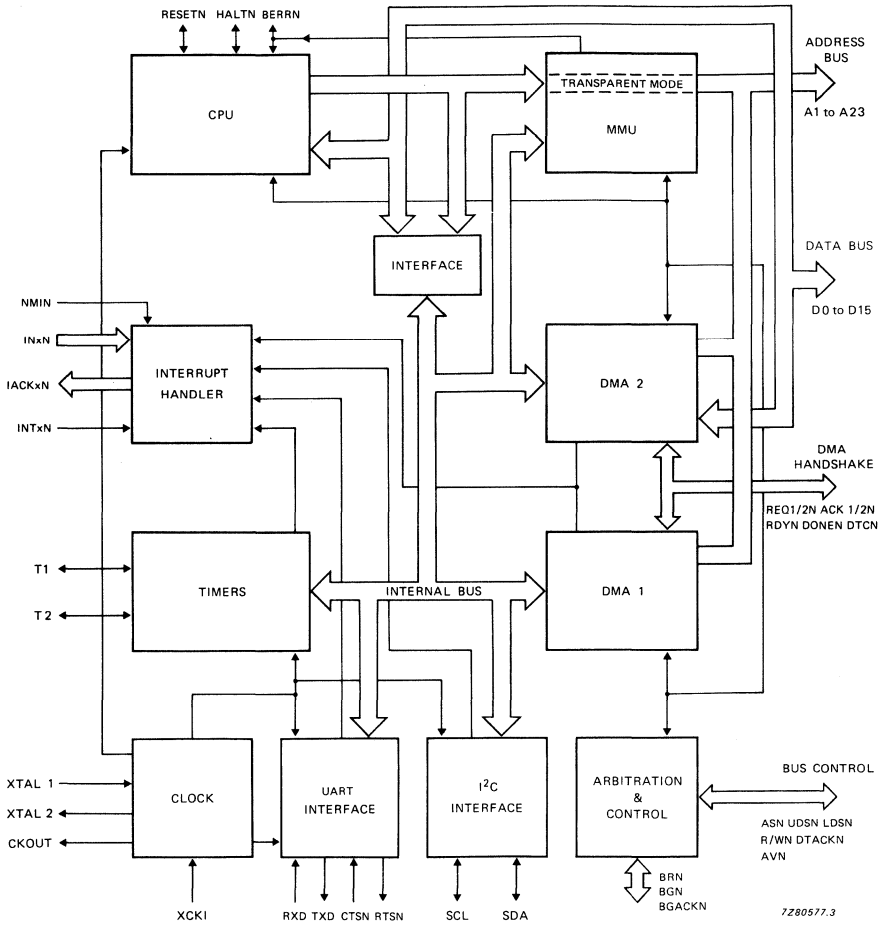


Fig.2 Block diagram.

DEVELOPMENT DATA

SIGNAL DESCRIPTION

MNEMONIC	TYPE	PIN NO.	FUNCTION
A1 to A23	O	32–42, 44–55	**(Active HIGH, three-state) Address bus** for direct addressing of 16 Mbytes of memory.
DO to D15	I/O	8–2, 84–76	**(Active HIGH, three-state) Data-bus,** 16-bit wide bidirectional.
ASN	O	19	**(Active-LOW, three-state) Address Strobe** – indicates a valid address on the bus.
LDSN	O	21	**(Active-LOW, three-state) Lower Data Strobe** – indicates that: – For a WRITE cycle, the data is valid on the lower half of the data bus (D0 to D7). – For a READ cycle, the data is to be placed on the lower half of the bus (D0 to D7).
UDSN	O	20	**(Active-LOW, three-state) Upper Data Strobe** – indicates that: – For a WRITE cycle, the data is valid on the upper half of the data bus (D8 to D15). – For a READ cycle, the data is to be placed on the upper half of the bus (D8 to D15).
R/WN	O	23	**Read (active-HIGH)/Write (active-LOW)** – this controls the direction of data flow.
DTACKN	I	24	**(Active-LOW) Data Transfer Acknowledge** – Asserted by the peripheral during CPU or DMA bus cycles when data is either received from or placed on the bus. If not asserted punctually, it causes the CPU or DMA controller to insert wait states.
BRN	I	11	**(Active-LOW) Bus Request** – Asserted by wire-ORed external DMA devices that request bus ownership.
BGN	O	9	**(Active-LOW) Bus Grant Output** – A daisy chain output that is asserted by the 68070 when the bus is granted by the CPU and the DMA does not have a bus request pending.
BGACKN	I/O	10	**(Active-LOW, Open Drain) Bus Grant Acknowledge** – Asserted by any DMA device (internal or external) that has control of the bus. As long as this line is held LOW externally, the 68070 will hold the bus signals in the high impedance state. When BGACKN is released, the 68070 will have access to the bus. Note that interrupts cannot be serviced while BGACKN is held LOW.
RESETN	I/O	28	**(Active-LOW, Open Drain) Bidirectional Reset** – If asserted externally together with the HALTN line, it will cause the processor to enter the Reset state. It is driven LOW by the processor when the RESET instruction resets external hardware.
HALTN	I/O	27	**(Active-LOW, Open Drain) Bidirectional Halt** – If asserted externally together with RESETN, it causes the 68070 to enter the Reset state. If asserted alone, it will cause the CPU or DMA controller to stop after completion of the current bus cycle. If HALTN and BERRN are asserted together, the 68070 will complete the current bus cycle, stop operation, and place all 3-state lines in the high-impedance state until HALTN and BERRN have been released, and then it will rerun the same bus cycle. BERRN should be released before HALTN. As long as HALTN is held LOW, all control signals are inactive and all 3-state lines are placed in the high-impedance state. When the processor has stopped executing instructions (e.g. after a double bus fault), the processor drives this line LOW.

SIGNAL DESCRIPTION (continued)

MNEMONIC	TYPE	PIN NO.	FUNCTION
BERRN	I/O	26	**(Active–LOW, Open Drain) Bus Error** – If this line is asserted during a bus cycle, it indicates that there was a fault in the bus cycle access. If asserted together with HALTN, the same bus cycle will be rerun after both HALTN and BERRN have been released. If BERRN is asserted alone, the 68070 will start bus-error exception processing. BERRN is driven LOW by the 68070 when the on-chip MMU indicates a bus error.
INT1N, INT2N	I	61, 60	**(Active-LOW) Latched interrupt inputs** – A LOW level of $\geqslant$ 1 clock pulse will be stored as a pending interrupt request. Priority levels are programmable.
IN2N, IN4N, IN5N	I	66, 63, 59	**(Active-LOW) Decoded interrupt priority inputs** – IN2N has the lower and IN5N has the higher priority.
NMIN	I	57	**(Active-LOW) Non-maskable interrupt (level 7)** – While the other interrupts may be masked (disabled), this interrupt is always enabled.
IACK2N, IACK4N IACK5N, IACK7N	O	65, 62, 58, 56	**(Active-LOW) Decoded interrupt acknowledge** – Asserted during an interrupt acknowledge sequence to indicate to a peripheral that its interrupt request is being serviced.
AVN	I	25	**(Active-LOW) Auto vectored interrupts** – If held LOW during the interrupt acknowledge sequence, the processor calculates the appropriate vector from a fixed vector table. If kept HIGH, the peripheral must provide an 8-bit vector number.
V_{DD}		1, 43	Supply voltage +5.0V nominal.
V_{SS}		22, 64	Ground.
XTAL1, XTAL2	I	30, 31	**External crystal inputs** – XTAL1 can be used as a clock-input if an external clock generator is used. The crystal or external clock frequency is divided by 2 to obtain the internal clock and CKOUT signals.
CKOUT	O	29	**Clock out** – This is the reference from the internal system clock.
REQ1N, REQ2N	I	12, 14	**(Active-LOW) DMA Request** – These are inputs from I/O devices requesting service from the DMA controller and causes it to request control of the bus. In burst mode, the inputs are level sensitive and the DMA controller releases the bus after REQxN is negated and the current DMA cycle is completed. In cycle-stealing mode, REQxN inputs are triggered by a negative pulse. This pulse must occur at least one clock cycle before DTCN is asserted to ensure continuous transfer.
ACK1N, ACK2N	O	13, 15	**(Active-LOW) DMA Request Acknowledge** – ACKxN is asserted by the DMA controller to indicate that it has acquired the bus and the requested device bus cycle is now beginning. It is asserted at the beginning of every device cycle together with ASN, and is negated at the end of every device bus cycle.
RDYN	I	18	**(Active-LOW) Device Ready** – The requesting device asserts RDYN to indicate to the DMA controller that valid data has either been stored or put on the bus. If RDYN is negated, it indicates that the data has neither been stored nor put on the bus, causing the DMA controller to insert wait states. RDYN can be held LOW permanently if the device is fast enough, indicating that the device is always ready and so no wait states are required. RDYN is not monitored by channel 2 in the dual-address mode.

SIGNAL DESCRIPTION (continued)

MNEMONIC	TYPE	PIN NO.	FUNCTION
DTCN	O	17	**(Active-LOW, Open Drain) Device Transfer Complete** – In DMA mode, DTCN is asserted by the DMA controller to indicate to the device that the requested data transfer is complete. On a write-to-memory operation, it indicates that the data provided by the device has been stored successfully. On a read-from-memory operation, it indicates to the device that the data from memory is present on the data bus and should be latched.
DONEN	I/O	16	**(Active-LOW, Open Drain) Done** – With DONEN as an output, the DMA controller asserts it simultaneously with the ACKxN output to indicate to the device that the transfer count is zero and therefore, the DMA controller's operation is complete. If, as an input, DONEN is asserted by the device before the transfer count reaches zero, it causes the DMA controller to abort operation and generate an interrupt request (if the interrupts are enabled).
SCL	I/O	75	**(Open Drain) Serial clock** – SCL is the clock signal for I^2C-bus operation. It is either driven by the 68070 when the I^2C interface is in the master mode, or is the clock input if the I^2C interface is in the slave mode.
SDA	I/O	74	**(Open Drain) Serial data** – SDA is the data signal for the I^2C-bus.
T1, T2	I/O	68, 67	**(Three-state) Timers 1 and 2** – These are I/O signals for the capture timers of channels 1 and 2 respectively. They can be programmed as either outputs for pulses or inputs for count cycles and events.
RXD	I	72	**Receive Data** – RXD is the data input for the UART serial interface.
TXD	O	73	**Transmit Data** – TXD is data output for the UART serial interface.
RTSN	O	71	**(Active-LOW) Request To Send** – This output of the UART serial interface indicates that the receiver is ready to accept data on the RXD line.
CTSN	I	70	**(Active-LOW) Clear To Send** – This input to the UART serial interface indicates that the remote receiving device is ready. RTSN and CTSN can be connected together if no control lines are needed.
XCKI	I	69	**External clock** – When selected, XCKI is the clock input for the UART serial interface. This signal can be used either: – to generate special baud rates or, – when a crystal frequency other than 19,6608 MHz is used by the 68070, an external clock of 4,9152 MHz can be connected to this input to generate the standard baud rates.

DEVELOPMENT DATA

ON-CHIP ADDRESSES

All memory locations on the peripheral side of the on-chip interface can only be accessed in SUPERVISOR mode; i.e. the S-bit in the Processor Status Word (PSW) is set to 1. All registers on the peripheral side of the interface are memory mapped separately from the 68070s external 16 Mbyte memory map. The on-chip address space which is decoded by the two MSBs (A31 and A30) of the 32-bit internal address and the S-bit of the processor status word is shown in Table 1.

Table 1 A31, A30 and S–bit decoding

S	A31	A30	
X	0	0	external
X	0	1	external
1	1	0	internal only
0	1	0	external
X	1	1	external

The address map of all on-chip peripherals is given in Table 2.

Table 2 On-Chip Addresses, (hexadecimal).

Address range			Description
00000000	to	7FFFFFFF	off-chip
80000000	to	80000FFF	on-chip, reserved
80001000			LIR priority level
80001001	to	80002000	on-chip, reserved
80002001	to	80002009	I^2C interface
8000200A	to	80002010	on-chip, reserved
80002011	to	8000201F	UART interface
80002020	to	80002029	TIMER
8000202A	to	80002044	on-chip, reserved
80002045			PICR1
80002046			on-chip, reserved
80002047			PICR2
80002048	to	80003FFF	on-chip, reserved
80004000	to	80007FFF	DMA Controller
80008000	to	8000807F	MMU
80008080	to	BFFFFFFF	on-chip, reserved
C0000000	to	FFFFFFFF	off-chip

BUS TIMING

Bus cycles in the 68070 are similar to those of a 68000 running on a 10 MHz clock frequency. However, if the DTACKN signal is not asserted by the time the 68070 is ready to transmit or receive data, it will insert wait cycles. Upper and lower data strobes (UDSN and LDSN) are asserted independently with respect to the type of transfer (low byte – LDSN asserted, high byte – UDSN asserted, and word – both strobes asserted).

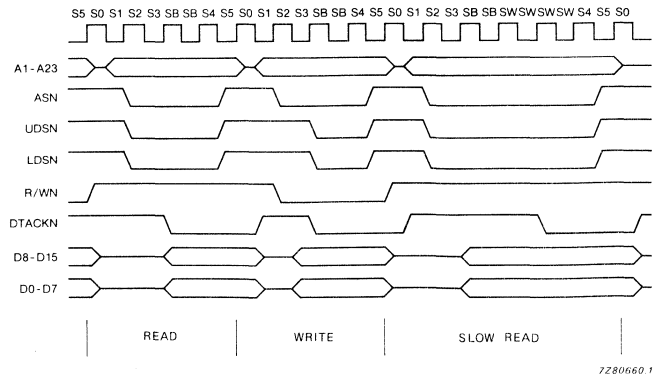


Fig.3 Read, write and slow read cycle timing.

CPU FUNCTIONAL DESCRIPTION

GENERAL

The CPU of the 68070 is software compatible with the 68000, so all programs written for the 68000 will run on the 68070 unchanged. However, for certain applications the following differences between the processors should be noted:

- Differences exist in the bus-error exception processing since the 68070 can provide full bus-error recovery.
- The timing is different because of the 68070's new architecture and technology. Although the bus timing is similar to a 10 MHz 68000, instruction execution timing is completely different (For execution timing, see the end of this section, Tables 7 to 19).

PROGRAMMING MODEL AND DATA ORGANIZATION

The programming model is identical to that of the 68000 as shown in Fig. 4 with seventeen 32-bit registers, a 32-bit Program Counter and a 16-bit Status Register. The first eight registers (D0 – D7) are used as data registers for byte, word and long-word operations. The second group of registers (A0 – A6) and the system stack pointer (A7) can be used as software stack pointers and base address registers. In addition, these registers can be used for word and long-word address operations.

All seventeen registers can be used as index registers.

Figure 4 shows the programming model and Figure 5 illustrates the status register.

The 68070 supports bit, 8, 16 and 32-bit integers, and BCD data, together with 32-bit addresses. Each data type is arranged in the memory as shown in Figure 6.

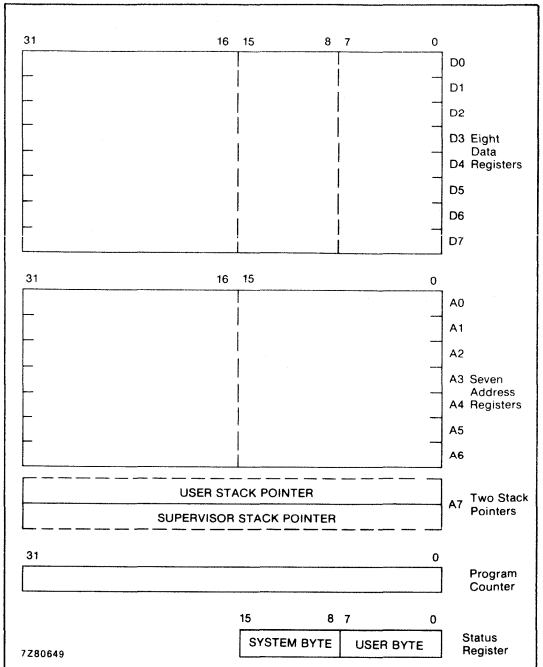


Fig.4 Programming model.

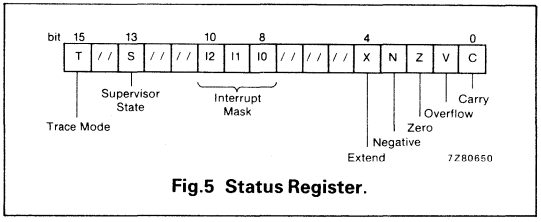
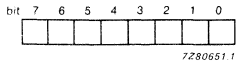
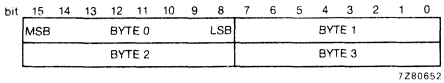


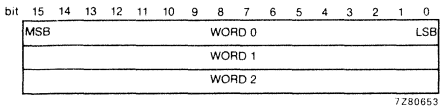
Fig.5 Status Register.



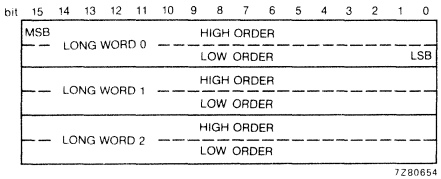
(a) Bit data (1 byte = 8 bits).



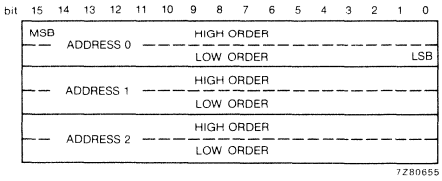
(b) Integer data(1byte = 8 bits).



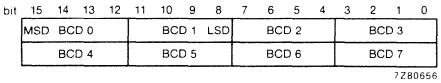
(c) Word data (16 bits).



(d) Long-word data (32 bits).



(e) Addresses (1 address = 32 bits).



(f) BCD data (2 BCD digits = 1 byte).

Fig.6 Memory data organization.

INTERNAL AND EXTERNAL OPERATION

The 68070 operates with a maximum internal clock frequency of 10 MHz and a minimum of 4 MHz. Each clock cycle is divided into 2 states. A non-access machine cycle has 3 clock cycles or 6 states (S0 to S5) and a bus cycle (SB) normally consists of 3 clock cycles plus 1 bus cycle (8 states). When DTACKN is not asserted, indicating that data has not been received or not put on the bus, wait states (SW) are inserted in multiples of 2.

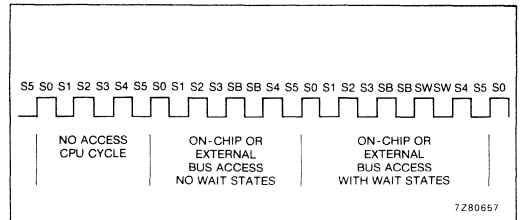


Fig.7 Machine cycles.

BUS ARBITRATION

Because a DMA controller is integrated on the 68070 as a possible bus master, the bus arbitration needs a priority protocol. This is done by a daisy-chain using the BGN of the CPU such that channel 1 of the DMA controller has highest priority, followed by channel 2 and then the external devices. The CPU grants bus acquisition and therefore has the lowest priority. Once the DMA controller has submitted the internal bus grant to an outside master, it will not interrupt the line until BUS GRANT ACKNOWLEDGE (BGACKN) has been negated. If the DMA controller has a DMA request pending, it will acquire the bus as soon as the external device has negated BGACKN. In this case, it will not submit BGN to an outside master even if the prospective master's BRN signal had been asserted before the DMA controller's pending request.

The 68070 bus arbitration also works like the 68008's two-signal mode, using BGN and BRN only. BGN will be asserted in response to BRN after either the processor has finished the bus cycle or the DMA controller has completed its task. BGN will stay asserted until either BGACKN is asserted or BRN is negated.

PROCESSING STATES AND EXCEPTION PROCESSING

The CPU is always in one of three processing states: normal, exception, or halted. The normal processing state is that associated with instruction execution; the memory references are to fetch instructions and operands, and to store results. A special case of the normal state is the stopped state which the processor enters when a STOP instruction is executed. In this state, no further memory references are made by the CPU.

The exception processing state is associated with interrupts, trap instructions, tracing and other exceptional conditions. The exception may be generated internally by an instruction or by an unusual condition arising during the execution of an instruction. Externally, exception processing can be forced by an interrupt, by bus error, or by a reset.

The processor can work in the 'user' or 'supervisor' state determined by the state of the S-bit in the status register. Accesses to the on-chip peripherals must be in the supervisor state.

All exception processing is performed in the supervisor state once the current content of the Status Register has been copied. The exception vector number is then determined, and a copy of the Status Register, the PC value and the Format + vector number are saved on the supervisor stack using the SSP. Finally, the contents of the exception vector location is fetched and loaded into the PC.

Exception vectors

Exception vectors are memory locations from which the CPU fetches the address of a routine that will handle that exception. All exception vectors are 2 words in length (see Fig. 8) except for the reset vector which is made up of 4 words. All exception vectors are contained in the supervisor data space. When the reset vector is fetched after a RESETN, the MMU is disabled and the reset vector is located at physical address 0.

A vector number is an 8-bit number that, when multiplied by 4, gives the address of an exception vector. Vector numbers are generated internally or externally depending on the cause of the exception. In the case of interrupts, during the interrupt acknowledge bus cycle, an external peripheral may send the CPU an 8-bit vector number (see Fig. 9) on the data bus lines D0 to D7. The CPU translates the vector number into the full 24-bit address as shown in Fig. 10. The memory layout for the exception vectors is given in Table 3.

Multiple exceptions

Because more than one exception could occur simultaneously, exceptions are grouped in order of priority (group 0, 1 and 2). Within each group the priority is as shown in Table 4, uppermost with the highest priority.

Table 3 Exception vector assignment

Vector Nos.	DEC	HEX	Assignment
0	0	000	Reset: initial SSP
1	4	004	Reset: initial PC
2	8	008	Bus error
3	12	00C	Address error
4	16	010	Illegal instruction
5	20	014	Zero divide
6	24	018	CHK instruction
7	28	01C	TRAPV instruction
8	32	020	Privilege violation
9	36	024	Trace
10	40	028	Line 1010 emulator
11	44	02C	Line 1111 emulator
12*	48	030	(Unassigned, reserved)
13*	52	034	(Unassigned, reserved)
14	56	038	Format error
15	60	03C	Uninitialized interrupt vector
16–23*	64	040	(Unassigned, reserved)
	95	05F	–
24	96	060	Spurious interrupt
25	100	064	Level 1 interrupt autovector
26	104	068	Level 2 interrupt autovector
27	108	06C	Level 3 interrupt autovector
28	112	070	Level 4 interrupt autovector
29	116	074	Level 5 interrupt autovector
30	120	078	Level 6 interrupt autovector
31	124	07C	Level 7 interrupt autovector
32–47	128	080	TRAP instruction vectors
	191	0BF	
48–56*	192	0C0	(Unassigned, reserved)
	227	0E3	
57	228	0E4	Level 1 on-chip interrupt autovector
58	232	0E8	Level 2 on-chip interrupt autovector
59	236	0EC	Level 3 on-chip interrupt autovector
60	240	0F0	Level 4 on-chip interrupt autovector
61	244	0F4	Level 5 on-chip interrupt autovector
62	248	0F8	Level 6 on-chip interrupt autovector
63	252	0FC	Level 7 on-chip interrupt autovector
64–255	256	100	User interrupt vectors

* Vectors 12, 13, 16 to 23, and 48 to 56 are reserved for future enhancements.
No user peripheral devices should be assigned to these numbers.

Table 4 Exception grouping and priority

Group	Exception	Processing
0	RESET ADDRESS ERROR BUS ERROR	Exception processing begins at the next machine cycle.
1	TRACE INTERRUPT ILLEGAL PRIVILEGE	Exception processing begins before the next instruction.
2	TRAP, TRAPV, CHK ZERO DIVIDE FORMAT ERROR	Exception processing is started through normal instruction execution.

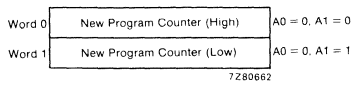


Fig.8 Exception vector format.

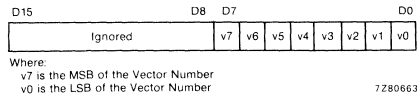


Fig.9 External peripheral vector format.

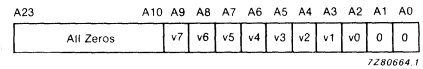


Fig.10 Address translated from 8-bit vector number.

RESET OPERATION

When the CPU executes a RESET instruction, the RESETN signal is driven LOW for 146 clock cycles to reset internal and external peripherals. In this case the CPU itself is not affected, but all on-chip peripherals are reset. When both the RESETN and HALTN signals are driven LOW by an external device, the CPU and on-chip peripherals are reset. The CPU responds by reading the reset vector table entry (vector number zero, address 000000 HEX) and loads it into the Supervisor Stack Pointer (SSP). Vector table entry number one (at address 000004 HEX) is read next and loaded into the Program Counter (PC). The CPU then initializes the Status Register (SR) to an interrupt level of seven and instruction execution is started (see Fig. 11).

All 3-state output signals are placed in the high-impedance state for as long as the RESETN and HALTN signals are externally driven. When the RESETN and HALTN signals are released, after start-up time the CPU will execute 4 read cycles to load the SSP High, SSP Low, PC High, and PC Low. Then the first instruction is fetched and executed. The HALTN signal must be driven LOW at the same time as the RESETN signal. The 68070 will only start to read the stack pointer and the initial Program Counter after both signals have been released. RESETN should not be released after HALTN.

When the V_{DD} is initially applied to the 68070, an external RESET must be applied to the RESETN and HALTN pins for at least 100 ms.

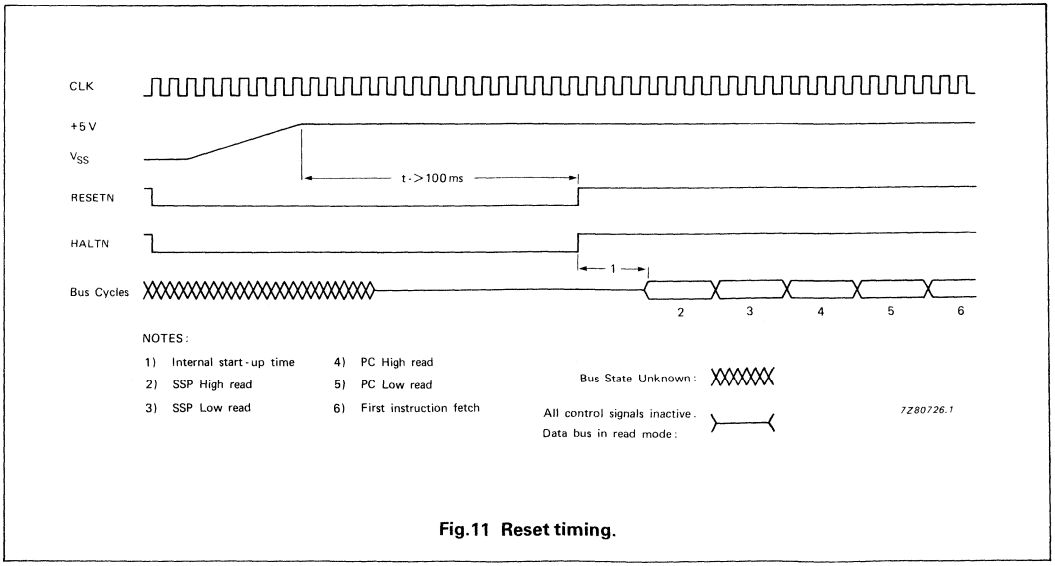


Fig.11 Reset timing.

BUS ERROR PROCESSING

Like the 68000, the 68070 uses the BUS ERROR (BERRN) and the HALTN signals to distinguish between two bus-error handling routines. If both the BERRN and the HALTN signals are asserted, the 68070 will rerun the last bus cycle as soon as both the HALTN and BERRN lines are released. This is valid for both the CPU and the DMA controller. The BERRN should be negated before HALTN (see Fig. 12).

If just the BERRN signal is asserted, bus error exception processing is entered.

If the DMA controller is the affected master, it will:

- stop the service after the current bus cycle is terminated,
- release the bus,
- set the BERRN bit in its status word, and
- send an interrupt if the INTERRUPT ENABLE bit in its status word was set.

The address counter reflects the address of the faulty bus cycle, while the transfer counter indicates the number of successful transfers.

If the CPU is the bus master, it will enter the bus error exception processing after the current bus cycle is terminated and BERRN has been released. Since the architecture of the 68070 differs from the 68000, it handles bus errors in a different manner. Unlike the 68000, the 68070 allows full recovery from bus errors.

The procedure follows the usual sequence of steps:

- the status register is copied.
- the supervisor state is entered.
- the trace state is turned off, and
- the vector number is generated to refer to the bus error vector.

To save more of the context, additional information is saved in the supervisor stack as follows:

- The program counter and a copy of the status register are saved.
- A format word containing a special bit configuration for the 68070 long stack format, and the vector number of the exception, in this case the bus error exception vector, is stacked.
- Besides other internal information, the processor saves the address which was being accessed by the aborted bus cycle.
- Specific information about the access is either saved or is retrievable from stacked information.
- A special status word is saved to determine the state of the (internal) function codes, the source of the bus error (MMU or External), and whether the error occurred during a read or write cycle, or in the first or second access of a long word operation. A RERUN bit in this special status word has to be set to suppress a retry of the faulty bus cycle on Return from Exception (RTE).
- The instruction register as well as the temporary registers is saved.

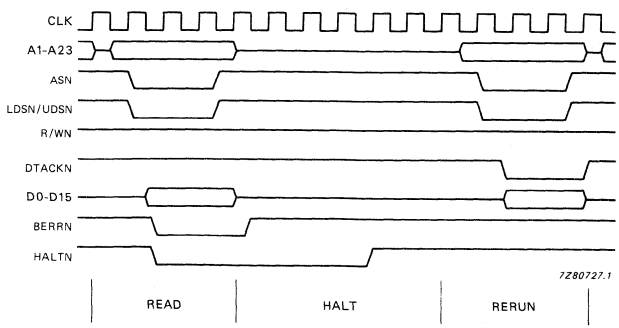


Fig.12 Rerun bus cycle timing.

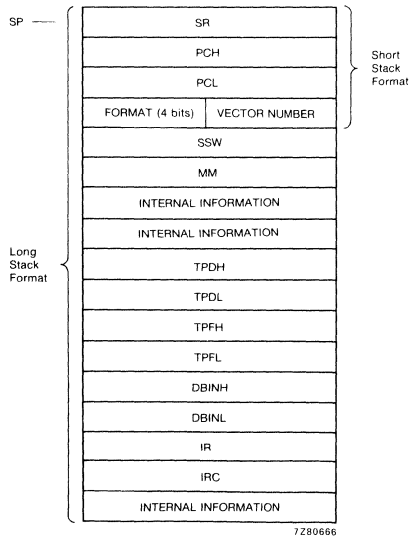
68070 STACK FORMAT

The stack format for exception processing is similar to the 68010 (rather than the 68000) although the information stored is not the same, due to the different architecture.

To handle this format, the 68070 differs from the 68000 in that:

- the stack format is changed
- the minimum number of words put into or restored from the stack is 4 (68010 compatible; not 3 as for the 68000)
- the RTE instruction decides (with aid of the 4 format bits) whether more information has to be restored, as follows:
  The 68070 long format is used for bus error and address error exceptions, all other exceptions use the short format
- if another format code other than one of the two listed above is detected during the restore action, a FORMAT ERROR occurs.

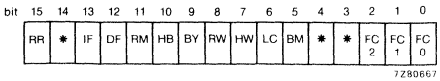
If the user wants to finish the instruction in which the bus or address error occurred, the 68070 format must be used on RTE. If no changes to the stack are required during exception processing, the stack format is transparent to the user.



SR	–	Status Register.
PCH/PCL	–	Program Counter High/Low Word.
Format	–	Indicating either a short stack format (only the first four words, or the long 68070 format for bus and address error exceptions.
Vector Number	–	The vector number of the exception in the vector table; e.g. 2 for a bus error, and 3 for an address error.
SSW	–	Special Status Word.
MM	–	Current Move Multiple Mask.
TPDH/TPDL	–	Data of a faulty write cycle, the data can be found here.
TPFH/TPFL	–	Address used during the faulty bus cycle.
DBINH/DBINL	–	Data that has been read prior to the faulty cycle can in some cases be found here.
IR	–	Holds the present instruction executed.
IRC	–	Holds either the present instruction executed or the prefetched instruction.

Fig.13 Stack format.

DEVELOPMENT DATA



RR – Rerun. By default, this bit is set to 0. If set 1, the CPU will not rerun the faulty bus cycle on return from exception (RTE).

* – Undefined (reserved).

IF – The faulty cycle was an instruction fetch.

DF – The faulty cycle was a data fetch.

RM – The error occurred during a read-modify-write cycle.

HB – High Byte.

BY – The faulty cycle was a byte transfer.

RW – Read/Write cycle.

HW – High Word.

LC – The faulty cycle was during a long-word access.

BM – The bus error was caused by the on-chip MMU.

FC 2, 1, 0 – These bits hold the internal function codes during the faulty bus cycle. The function codes are the same as for the 68000 and affect the status of the CPU during the faulty bus cycle as follows:

FC2	FC1	FC0	
0	0	0	reserved
0	0	1	user data
0	1	0	user program
0	1	1	reserved
1	0	0	reserved
1	0	1	supervisor program
1	1	0	supervisor program
1	1	1	interrupt acknowledge

Fig.14 Special status word.

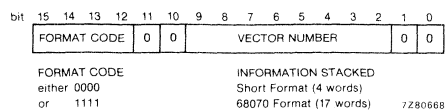


Fig.15 Vector number and format code.

INTERRUPT PROCESSING

The 68070 interrupt handling follows the same basic rules as the 68000. However, the following changes have been made to simplify system development:

- the IPL signals have been replaced by decoded interrupt signals IN2N, IN4N, IN5N, and NMIN (interrupt level 7)
- each of the interrupt inputs has a separate acknowledge signal IACK2N, IACK4N, IACK5N and IACK7N
- two latched interrupt inputs (INT1N and INT2N) have programmable priority levels. They have no interrupt acknowledge signal and are always served by autovectoring (see Table 3)
- interrupt priority levels IPL1, IPL3 and IPL6 are not available externally, unless programmed into INT1N or INT2N
- if autovectoring is desired, the AUTOVECTOR request signal (AVN) must be asserted during the interrupt acknowledge routine
- to ensure being recognized, an interrupt signal IN2N, IN4N, IN5N, and NMIN must stay asserted until it is acknowledged by its IACKxN signal.

If the priority of the interrupt pending is greater than the current processor priority, then:

- the exception processing sequence is started
- a copy of the status register is saved
- the privilege level is set to supervisor state
- tracing is supressed
- the priority level of the processor is set to that of the interrupt being acknowledged.

The processor then gets the vector number from the interrupting device, classifies it as an interrupt acknowledge and displays the interrupt level number being acknowledged on the address bus.

During the interrupt acknowledge cycle, LDSN is not asserted (as is the case with the 68000). This is done to simplify the address decoding circuitry of the memory. Acknowledge cycle decoding (by the interrupting device) is done using the IACKxN signal instead.

If autovectoring is requested by the external logic, the processor generates a vector number internally that corresponds to the interrupt level number. Then, if a bus error is indicated by the external logic, the interrupt is treated as spurious and the vector number that was generated will refer to the spurious interrupt vector.

Priority level 7 cannot be inhibited by the interrupt priority mask (Non-maskable interrupt – NMI).

If external and on-chip peripherals are programmed to the same interrupt priority level, an on-chip daisy-chain defines the priority as follows:

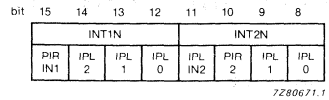
external interrupts	INxN	highest priority
	INT1N	
	INT2N	
	TIMER	
	UART RX	
	UART TX	
	I^2C	
	DMA CH1	
	DMA CH2	lowest priority

The two latched interrupt inputs INT1N and INT2N have a common Latched Interrupt priority level Register (LIR) as shown in Fig. 16.

CLOCK CIRCUITRY

The clock signals required by each part of the 68070 are generated from the same Master Oscillator. Dividing this frequency by two gives the clock signals for the CPU, MMU and DMA. Dividing the Master Oscillator signal by four provides the clock signals for the UART and I^2C interfaces, and dividing the Master Oscillator by 192 gives the clock for the Timer.

When the Master Oscillator frequency differs from 19,6608 MHz, and standard baud rates are required from the UART, it is possible to clock the UART separately by supplying externally a 4,9152 MHz signal on the XCKI pin. Only the UART operates from the XCKI pin. The Timer will still have a period of 192 times the Master Oscillator period. The speed of the I^2C interface is programmable and may have to be programmed with a different division factor.



INT1N and INT2N refer to the external pins.

IPL — Interrupt priority level of interrupts connected externally to pins INT1N or INT2N. IPL2 is the MSB and IPL0 is the LSB. All values are positive true; IPL = 111 represents priority level 7 and IPL = 000 will inhibit the interrupts.

PIR — Pending Interrupt Reset, when set to 1 any pending interrupts of the respective interrupt input will be reset and the inputs must be toggled again to create another interrupt. Note that this does not reset the interrupting status of a connected peripheral and further, if the IPL bits are changed without setting the PIR bit then spurious interrupts may occur. Reading the PIR bits will return a 0.

note: Initially and after RESET, all LIR bits are cleared to zero.

Fig.16 Latched Interrupt priority level Register (LIR).

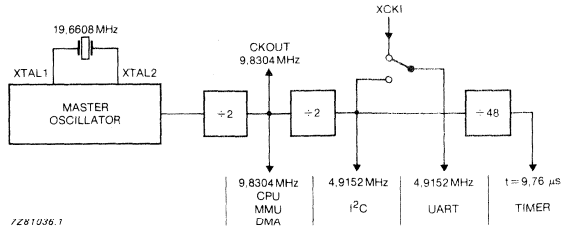


Fig.17 Clock circuitry.

INSTRUCTION SET AND ADDRESSING MODES

The 68070 is completely code compatible with the 68000, which means that programs developed for the 68000 will run on the 68070. This applies to both source and object code.

The instruction set was designed to minimize the number of mnemonics that the programmer has to remember. Tables 5 and 6 give an overview of the instruction set and of the different addressing modes.

Table 5 Instruction set

Mnemonic	Description	Operation	Condition Codes				
			X	N	Z	V	C
ABCD	Add Decimal with Extend	$(Destination)_{10}+(Source)_{10}\rightarrow Destination$	*	U	*	U	*
ADD	Add Binary	(Destination)+(Source)→Destination	*	*	*	*	*
ADDA	Add Address	(Destination)+(Source)→Destination	–	–	–	–	–
ADDI	Add Immediate	(Destination)+Immediate Data → Destination	*	*	*	*	*
ADDQ	Add Quick	(Destination)+Immediate Data → Destination	*	*	*	*	*
ADDX	Add Extended	(Destination)+(Source)+X→Destination	*	*	*	*	*
AND	AND Logical	(Destination) Λ (Source)→Destination	–	*	*	0	0
ANDI	AND Immediate	(Destination) Λ Immediate Data → Destination	–	*	*	0	0
ASL, ASR	Arithmetic Shift	(Destination) Shifted by <count> → Destination	*	*	*	*	*
B_{cc}	Branch Conditionally	If CC then PC+d→PC	–	–	–	–	–
BCHG	Test a Bit and Change	~(<bit number>) OF Destination→Z	–	–	*	–	–
		~(<bit number>) OF Destination→	–	–	*	–	–
		<bit number> OF Destination	–	–	*	–	–
BCLR	Test a Bit and Clear	~(<bit number>) OF Destination→Z	–	–	*	–	–
		0→<bit number>→OF Destination	–	–	*	–	–
BRA	Branch Always	PC+d→PC	–	–	–	–	–
BSET	Test a Bit and Set	~(<bit number>) OF Destination→Z	–	–	*	–	–
		1→<bit number> OF Destination	–	–	*	–	–
BSR	Branch to Subroutine	PC→SP@–;PC+d→PC	–	–	–	–	–
BTST	Test a Bit	~(<bit number>) OF Destination→Z	–	–	*	–	–
CHK	Check Register against Bounds	If Dn<0 or Dn> (<ea>) then TRAP	–	*	U	U	U
CLR	Clear an Operand	0→Destination	–	0	1	0	0
CMP	Compare	(Destination)–(Source)	–	*	*	*	*
CMPA	Compare Address	(Destination)–(Source)	–	*	*	*	*
CMPI	Compare Immediate	(Destination)–Immediate Data	–	*	*	*	*
CMPM	Compare Memory	(Destination)–(Source)	–	*	*	*	*
DB_{cc}	Test Condition, Decrement and Branch	If CC then Dn–1→Dn; if Dn ≠ –1 then PC+d → PC	–	–	–	–	–
DIVS	Signed Divide	(Destination)/(Source) →Destination	–	*	*	*	0
DIVU	Unsigned Divide	(Destination)/(Source) → Destination	–	*	*	*	0
EOR	Exclusive OR Logical	(Destination) ⊕ (Source) → Destination	–	*	*	0	0
EORI	Exclusive OR Immediate	(Destination) ⊕ Immediate Data → Destination	–	*	*	0	0
EXG	Exchange Register	Rx↔Ry	–	–	–	–	–
EXT	Sign Extend	(Destination) Sign–extended → Destination	–	*	*	0	0
JMP	Jump	Destination→PC	–	–	–	–	–
JSR	Jump to Subroutine	PC→SP@–; Destination→PC	–	–	–	–	–
LEA	Load Effective Address	Destination→An	–	–	–	–	–
LINK	Link and Allocate	AN→SP@–; SP→An; SP+d→SP	–	–	–	–	–
LSL, LSR	Logical Shift	(Destination) Shifted by <count> → Destination	*	*	*	0	*
MOVE	Move Data from Source to Destination	(Source)→Destination	–	*	*	0	0
MOVE to CCR	Move to Condition Code	(Source)→CCR	*	*	*	*	*

Table 5 Instruction set (continued)

Mnemonic	Description	Operation	Condition Codes				
			X	N	Z	V	C
MOVE to SR	Move to the Status Register	(Source)→SR	*	*	*	*	*
MOVE from SR	Move from the Status Register	SR→Destination	–	–	–	–	–
MOVE USP	Move User Stack Pointer	USP→An; An→USP	–	–	–	–	–
MOVEA	Move Address	(Source)→Destination	–	–	–	–	–
MOVEM	Move Multiple Registers	Registers→Destination	–	–	–	–	–
		(Source)→Registers	–	–	–	–	–
MOVEP	Move Peripheral Data	(Source)→Destination	–	–	–	–	–
MOVEQ	Move Quick	Immediate Data→Destination	–	*	*	0	0
MULS	Signed Multiply	(Destination)*(Source) → Destination	–	*	*	0	0
MULU	Unsigned Multiply	(Destination)*(Source) → Destination	–	*	*	0	0
NBCD	Negate Decimal with Extend	$0-(\text{Destination})_{10}-X \rightarrow$ Destination	*	U	*	U	*
NEG	Negate	0−(Destination)→Destination	*	*	*	*	*
NEGX	Negate with Extend	0−(Destination)−X→Destination	*	*	*	*	*
NOP	No Operation	–	–	–	–	–	–
NOT	Logical Complement	~(Destination)→Destination	–	*	*	0	0
OR	Inclusive OR Logical	(Destination) v (Source)→Destination	–	*	*	0	0
ORI	Inclusive OR Immediate	(Destination) v Immediate Data→Destination	–	*	*	0	0
PEA	Push Effective Address	Destination→SP@−	–	–	–	–	–
RESET	Reset External Devices	–	–	–	–	–	–
ROL, ROR	Rotate (Without Extend)	(Destination) Rotated by <count>→Destination	–	*	*	0	*
ROXL, ROXR	Rotate with Extend	(Destination) Rotated by <count>→Destination	*	*	*	0	*
RTE	Return from Exception	SP@+→SR; SP@+→PC	*	*	*	*	*
RTR	Return and Restore Condition Codes	SP@+→CC; SP@+→PC	*	*	*	*	*
RTS	Return from Subroutine	SP@+→PC	–	–	–	–	–
SBCD	Subract Decimal with Extend	$(\text{Destination})_{10}-(\text{Source})_{10}-X \rightarrow$Destination	*	U	*	U	*
S_{CC}	Set According to Condition	If CC then 1's→Destination else 0's→Destination	–	–	–	–	–
STOP	Load Status Register and Stop	Immediate Data→SR; STOP	*	*	*	*	*
SUB	Subtract Binary	(Destination)−(Source)→Destination	*	*	*	*	*
SUBA	Subtract Address	(Destination)−(Source) →Destination	–	–	–	–	–
SUBI	Subtract Immediate	(Destination)−Immediate Data→Destination	*	*	*	*	*
SUBQ	Subtract Quick	(Destination)−Immediate Data→Destination	*	*	*	*	*
SUBX	Subtract with Extend	(Destination)−(Source)−X→Destination	*	*	*	*	*
SWAP	Swap Register Halves	Register [31:16]↔Register [15:0]	–	*	*	0	0
TAS	Test and Set an Operand	(Destination) Tested→CC; 1→[7] OF Destination	–	*	*	0	0
TRAP	Trap	PC→SSP@−; SR→SSP@−; (Vector)→PC	–	–	–	–	–
TRAPV	Trap on Overflow	If V then TRAP	–	–	–	–	–
TST	Test an Operand	(Destination) Tested→CC	–	*	*	0	0
UNLK	Unlink	An →SP; SP@+→An	–	–	–	–	–

[ ] = bit number 0 cleared U defined
* affected 1 set @ location addressed by
– unaffected

DEVELOPMENT DATA

INSTRUCTION TIMING

Table 6 Data addressing modes

Mode	Generation
Register Direct Addressing	
Data Register Direct	EA=Dn
Address Register Direct	EA=An
Absolute Data Addressing	
Absolute Short	EA=(Next Words)
Absolute Long	EA=(Next Two Words)
Program Counter Relative Addressing	
Relative with Offset	EA=(PC)+d_{16}
Relative with Index and Offset	EA=(PC)+(Xn)+d_8
Register Indirect Addressing	
Register Indirect	EA=(An)
Postincrement Register Indirect	EA=(An), An←An+N
Predecrement Register Indirect	An←An−N, EA=(An)
Register Indirect with Offset	EA=(An)+d_{16}
Indexed Register Indirect with Offset	EA=(An)+(Xn)+d_8
Immediate Data Addressing	
Immediate	DATA = Next Word(s)
Quick Immediate	Inherent Data
Implied Addressing	
Implied Register	EA=SR, USP, SSP, PC, SP

Notes

EA = Effective Address
An = Address register
Dn = Data Register
Xn = Address or Data register used as index register
N = 1 for bytes, 2 for words, and 4 for long words
← = Replaces
SR = Status register
PC = Program counter
( ) = Contents of
d_8 = 8-bit offset (displacement)
d_{16} = 16-bit offset (displacement)
SP = Stack pointer
SSP = System stack pointer
USP = User stack pointer

Table 7 Effective address calculation times

	Addressing Mode	.B	.W	.L
Rn	Data or Address Register Direct	0 (0/0)	0 (0/0)	
(An)	Address Register Indirect	4 (1/0)	8 (2/0)	
(An)+	Address Register Indirect postincrem.	4 (1/0)	8 (2/0)	
−(An)	Address Register Indirect predecrem.	7 (1/0)	11 (2/0)	
d(An)	Address Register Indirect Displacem.	11 (2/0)	15 (3/0)	
d(An,Xi)	Address Register Indirect with Index	14 (2/0)	18 (3/0)	
xxx.S	Absolute Short	8 (2/0)	12 (3/0)	
xxx.L	Absolute Long	12 (3/0)	16 (4/0)	
d(PC)	Program Counter with Displacement	11 (2/0)	15 (3/0)	
d(PC,Xi)	Program Counter with Index	14 (2/0)	18 (3/0)	
#xxx	Immediate	4 (1/0)	8 (2/0)	

The number of bus read and write cycles are shown in parenthesis as (R/W).

Table 8 MOVE byte and Move Word instruction clock periods

	Rn	(An)	(An)+	−(An)	d(An)	d(An,iX)	xxx.S	xxx.L
Rn	7 (1/0)	11 (1/1)	11 (1/1)	14 (1/1)	18 (2/1)	21 (2/1)	15 (2/1)	19 (3/1)
(An)	11 (2/0)	15 (2/1)	15 (2/1)	18 (2/1)	22 (3/1)	25 (3/1)	19 (3/1)	23 (4/1)
(An)+	11 (2/0)	15 (2/1)	15 (2/1)	18 (2/1)	22 (3/1)	25 (3/1)	19 (3/1)	23 (4/1)
−(An)	14 (2/0)	18 (2/1)	18 (2/1)	21 (2/1)	25 (3/1)	28 (3/1)	22 (3/1)	26 (4/1)
d(An)	18 (3/0)	22 (3/1)	22 (3/1)	25 (3/1)	29 (4/1)	32 (4/1)	26 (4/1)	30 (5/1)
d(An,Xi)	21 (3/0)	25 (3/1)	25 (3/1)	28 (3/1)	32 (4/1)	35 (4/1)	29 (4/1)	33 (5/1)
xxx.S	15 (3/0)	19 (3/1)	19 (3/1)	22 (3/1)	26 (4/1)	29 (4/1)	23 (4/1)	27 (5/1)
xxx.L	19 (4/1)	23 (4/1)	23 (4/1)	26 (4/1)	30 (5/1)	33 (5/1)	27 (5/1)	31 (6/1)
d(PC)	18 (3/1)	22 (3/1)	22 (3/1)	25 (3/1)	29 (4/1)	32 (4/1)	26 (4/1)	30 (5/1)
d(PC,Xi)	21 (3/0)	25 (3/1)	25 (3/1)	28 (3/1)	32 (4/1)	35 (4/1)	29 (4/1)	33 (5/1)
#xxx	11 (2/0)	15 (2/1)	15 (2/1)	18 (2/1)	22 (3/1)	25 (3/1)	19 (3/1)	23 (4/1)

Table 9 MOVE long instruction clock periods

	Rn	(An)	(An)+	−(An)	d(An)	d(An,iX)	xxx.S	xxx.L
Rn	7 (1/0)	15 (1/2)	15 (1/2)	18 (1/2)	22 (2/2)	25 (2/2)	19 (2/2)	23 (3/2)
(An)	15 (1/0)	23 (3/2)	23 (3/2)	26 (3/2)	30 (4/2)	33 (4/2)	27 (4/2)	31 (5/2)
(An)+	15 (3/0)	23 (3/2)	23 (3/2)	26 (3/2)	30 (4/2)	33 (4/2)	27 (4/2)	31 (5/2)
−(An)	18 (3/0)	26 (3/2)	26 (3/2)	29 (3/2)	33 (4/2)	36 (4/2)	30 (4/2)	34 (5/2)
d(An)	22 (4/0)	30 (4/2)	30 (4/2)	33 (4/2)	37 (5/2)	40 (5/2)	34 (5/2)	38 (6/2)
d(An,Xi)	25 (4/0)	33 (4/2)	33 (4/2)	36 (4/2)	40 (5/2)	43 (5/2)	37 (5/2)	41 (6/2)
xxx.S	19 (4/0)	27 (4/2)	27 (4/2)	30 (4/2)	34 (5/2)	37 (5/2)	31 (5/2)	35 (6/2)
xxx.L	23 (5/0)	31 (5/2)	31 (5/2)	34 (5/2)	38 (6/2)	41 (6/2)	35 (6/2)	39 (7/2)
d(PC)	22 (4/0)	30 (4/2)	30 (4/2)	33 (4/2)	37 (5/2)	40 (5/2)	34 (5/2)	38 (6/2)
d(PC,Xi)	25 (4/0)	33 (4/2)	33 (4/2)	36 (4/2)	40 (5/2)	43 (5/2)	37 (5/2)	41 (6/2)
#xxx	15 (3/0)	23 (3/2)	23 (3/2)	26 (3/2)	30 (4/2)	33 (4/2)	27 (4/2)	31 (5/2)

Table 10 Standard instruction clock periods

	Size	op<ea>, An	op<ea>, Dn	op<ea>,<M>
ADD	.B .W	7+ (1/0)	7+ (1/0)	11+ (1/1)
	.L	7+ (1/0)	7+ (1/0)	15+ (1/2)
AND	.B .W	–	7+ (1/0)	11+ (1/1)
	.L	–	7+ (1/0)	15+ (1/2)
CMP	.B .W	7+ (1/0)	7+ (1/0)	–
	.L	7+ (1/0)	7+ (1/0)	–
DIVS	–	–	169+** (1/0)	–
DIVU	–	–	130+* (1/0)	–
EOR	.B .W	–	7+ (1/0)	11+ 1/1)
	.L	–	7+ (1/0)	15+ (1/2)
MULS	–	–	76+* (1/0)	–
MULU	–	–	76+* (1/0)	–
OR	.B .W	–	7+ (1/0)	11+ (1/1)
	.L	–	7+ (1/0)	15+ (1/2)
SUB	.B .W	7+ (1/0)	7+ (1/0)	11+ (1/1)
	.L	7+ (1/0)	7+ (1/0)	15+ (1/2)

\+ add effective address calculation time

* the duration of the instruction is constant

** indicates maximum value

Table 11 Immediate instruction clock periods

	Size	op<im>,Dn	op<im>,An	op<im>,<M>
ADDI	.B .W	14 (2/0)	–	18+ (2/1)
	.L	18 (3/0)	–	26+ (3/2)
ADDQ	.B .W	7 (1/0)	7 (1/0)	11+ (1/1)
	.L	7 (1/0)	7 (1/0)	15+ (1/2)
ANDI	.B .W	14 (2/0)	–	18+ (2/1)
	.L	18 (3/0)	–	24+ (3/2)
CMPI	.B .W	14 (2/0)	–	14+ (2/0)
	.L	18 (3/0)	–	18+ (3/0)
EORI	.B .W	14 (2/0)	–	18+ (2/1)
	.L	18 (3/0)	–	26+ (3/2)
MOVEQ	.L	7 (1/0)	–	–
ORI	.B .W	14 (2/0)	–	18+ (2/1)
	.L	18 (3/0)	–	26+ (3/2)
SUBI	.B .W	14 (2/0)	–	18+ (2/1)
	.L	18 (3/0)	–	26+ (3/2)
SUBQ	.B .W	7 (1/0)	7 (1/0)	11+ (1/1)
	.L	7 (1/0)	7 (1/0)	15+ (1/2)

\+ add effective address calculation time

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Table 12 Single operand instruction clock periods

Instruction	Size	Register	Memory
CLR	Byte, Word	7 (1/0)	11 (1/1)+*
	Long	7 (1/0)	15 (1/2)+**
NBCD	Byte	10 (1/0)	14 (1/1)+
NEG	Byte, Word	7 (1/0)	11 (1/1)+
	Long	7 (1/0)	15 (1/2)+
NEGX	Byte, Word	7 (1/0)	11 (1/1)+
	Long	7 (1/0)	15 (1/2)+
NOT	Byte, Word	7 (1/0)	11 (1/1)+
	Long	7 (1/0)	15 (1/2)+
S_{CC}	Byte, Word	13 (1/0)	17 (1/1)+
	Long	13 (1/0)	14 (1/1)+
TAS	Byte	10 (1/0)	15 (1/1)+*
TST	Byte, Word	7 (1/0)	7 (1/0)+
	Long	7 (1/0)	7 (1/0)+

\+ add effective address calculation time

* subtract one read cycle (−4(1/0)) from effective address calculation

** subtract two read cycles (−8(2/0)) from effective address calculation

Table 13 Shift/rotate instruction clock periods

Instruction	Size	Register	Memory
ASR, ASL	Byte, Word	13+3n (1/0)	14 (1/1)+
	Long	13+3n (1/0)	–
LSR, LSL	Byte, Word	13+3n (1/0)	14 (1/1)+
	Long	13+3n (1/0)	–
ROR, ROL	Byte, Word	13+3n (1/0)	14 (1/1)+
	Long	13+3n (1/0)	–
ROXR, ROXL	Byte, Word	13+3n (1/0)	14 (1/1)+
	Long	13+3n (1/0)	–

\+ add effective address calculation time

Table 14 Bit manipulation instruction clock periods

Instruction	Size	Dynamic		Static	
		Register	Memory	Register	Memory
BCHG	Byte	–	14 (1/1)+	–	21 (2/1)+
	Long	10 (1/0)	–	17 (2/0)	–
BCLR	Byte	–	14 (1/1)+	–	21 (2/1)+
	Long	10 (1/0)	–	17 (2/0)	–
BSET	Byte	–	14 (1/1)+	–	21 (2/1)+
	Long	10 (1/0)	–	17 (2/0)	–
BTST	Byte	–	7 (1/0)+	–	14 (2/0)+
	Long	7 (1/0)	–	14 (2/0)	–

\+ add effective address calculation time

Table 15 Conditional instruction clock periods

	Displ.	Trap or Branch Taken	Trap or Branch Not taken
Bcc	.B	13 (1/0)	13 (1/0)
	.W	14 (2/0)	14 (2/0)
BRA	.B	13 (1/0)	–
	.W	14 (2/0)	–
BSR	.B	17 (1/2)	–
	.W	22 (2/2)	–
DBcc	cc True	–	14 (2/0)
	cc False	17 (2/0)	17 (3/2)
CHK	–	64 (3/5)+	19 (1/0)+
TRAPV	–	55 (3/4)	10 (1/0)

\+ add effective address calculation time

Table 16 JMP, JSR, LEA, PEA, MOVEM instruction clock periods

	Size	(An)	(An)+	−(An)	d(An)	d(An,Xi)	xxx.S	xxx.L	d(PC)	d(PC,Xi)
JMP	–	7	–	–	14	17	14	18	14	17
	–	(1/0)	–	–	(2/0)	(2/0)	(2/0)	(3/0)	(2/0)	(2/0)
JSR	–	18	–	–	25	28	25	29	25	28
	–	(1/2)	–	–	(2/2)	(2/2)	(2/2)	(2/2)	(2/2)	(2/2)
LEA	–	7	–	–	14	17	14	18	14	17
	–	(1/0)	–	–	(2/0)	(2/0)	(2/0)	(3/0)	(2/0)	(2/0)
PEA	–	18	–	–	25	28	25	29	25	28
	–	(1/2)	–	–	(2/2)	(2/2)	(2/2)	(3/2)	(2/2)	(2/2)
MOVEM M→R	.W	26+7n	26+7n	–	30+7n	33+7n	30+7n	34+7n	30+7n	33+7n
		(2+n/0)	(2+n/0)	–	(3+n/0)	(3+n/0)	(3+n/0)	(4+n/0)	(3+n/0)	(3+n/0)
	.L	26+11n	26+11n	–	30+11n	33+11n	30+11n	34+11n	30+11n	33+11n
		(2+2n/0)	(2+2n/0)	–	(3+2n/0)	(3+2n/0)	(3+2n/0)	(4+2n/0)	(3+2n/0)	(3+2n/0)
MOVEM R→M	.W	23+7n	–	23+7n	27+7n	30+7n	27+7n	31+7n	–	–
		(2/n)	–	(2/n)	(3/n)	(3/n)	(3/n)	(4/n)	–	–
	.L	23+11n	–	23+11n	27+11n	30+11n	27+11n	31+11n	–	–
		(2/2n)	–	(2/2n)	(3/2n)	(3/2n)	(3/2n)	(4/2n)	–	–

n = number of registers to move

Table 17 Multi−precision instruction clock periods

Instruction	Size	op Dn, Dn	op M, M
ADDX	Byte, Word	7 (1/0)	28 (3/1)
	Long	7 (1/0)	40 (5/2)
CMPM	Byte, Word	–	18 (3/0)
	Long	–	26 (5/0)
SUBX	Byte, Word	7 (1/0)	28 (3/1)
	Long	7 (1/0)	40 (5/2)
ABCD	Byte	10 (1/0)	31 (3/1)
SBCD	Byte	10 (1/0)	31 (3/1)

Table 18 Miscellaneous clock periods

Instruction	Size	Register	Memory	Register to Memory	Memory to Register
ANDI to CCR	–	14 (2/0)	–	–	–
ANDI to SR	–	14 (2/0)	–	–	–
EORI to CCR	–	14 (2/0)	–	–	–
EORI to SR	–	14 (2/0)	–	–	–
EXG	–	13 (1/0)	–	–	–
EXT	Word	7 (1/0)	–	–	–
	Long	7 (1/0)	–	–	–
LINK	–	25 (2/2)	–	–	–
MOVE from SR	–	7 (1/0)	11 (1/1)+	–	–
MOVE to CCR	–	10 (2/0)	10 (2/0)+	–	–
MOVE to SR	–	10 (2/0)	10 (2/0)+	–	–
MOVE from USP	–	7 (1/0)	–	–	–
MOVE to USP	–	7 (1/0)	–	–	–
MOVEP	Word	–	–	25 (2/2)	22 (4/0)
	Long	–	–	39 (2/4)	36 (6/0)
NOP	–	7 (1/0)	–	–	–
ORI to CCR	–	14 (2/0)	–	–	–
ORI to SR	–	14 (2/0)	–	–	–
RESET	–	154 (1/0)	–	–	–
RTE	–	–	–	–	–
short format		39 (5/0)			
long format:					
no rerun		140 (18/0)			
with rerun		146 (18/0)			
rerun of TAS		151 (19/1)			
RTR	–	22 (4/0)	–	–	–
RTS	–	15 (3/0)	–	–	–
STOP	–	13 (0/0)	–	–	–
SWAP	–	7 (1/0)	–	–	–
UNLK	–	15 (3/0)	–	–	–

+ add effective address calculation time

Table 19 Exception processing clock periods

Exception	Number of clock periods
Address error	158 (3/17)
Bus error	158 (3/17)
Interrupt	65 (4/4) *
Illegal instruction	55 (3/4)
Privilege violation	55 (3/4)
Trace	55 (3/4)
Trap	52 (3/4)
Divide by Zero	64 (3/4)+
RESET **	43 (4/0)

* The interrupt acknowledge bus cycle is assumed to take four external clock periods.

** Indicates the maximum time from when RESETN and HALTN are first sampled as negated to first instruction fetch.

68070 ON-CHIP MMU

The 68070 contains a Memory Management Unit (MMU) that, if enabled, supports virtual memory, multitasking, task protection and dynamic stack allocation. The 68070's MMU is a subset of the Memory Access Controllers in the 68000 family (68910 and 68920) and is software compatible with the contiguous segment mode of these devices.

SEGMENTATION

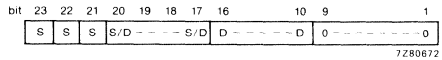
The MMU divides the memory into segments of multiples of 1 Kbyte (blocks). Two modes are possible:

Mode	Number of segments	Maximum segment length
1	8	2048 blocks = 2 Mbytes
2	128	128 blocks = 128 Kbytes

Memory protection is assigned on a segment to segment basis.

For address translation, the logical addresses can be split into 3 parts (see Fig. 18):

- segment number,
- displacement and
- offset.

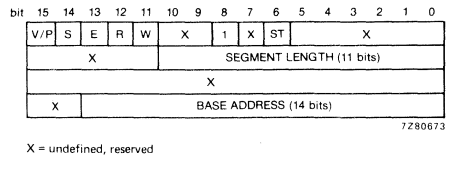


S = the segment number
S/D = either the segment number or a displacement, as defined by the MMU Control Register (MCR)
D = displacement
O = offset

Fig.18 Logical address format.

SEGMENT DESCRIPTORS

Every segment is described by a segment descriptor stored in the segment descriptor table in main memory. Each descriptor contains a segment address field, a segment protection field (with protection attributes) and the segment length. However, for ease of access, up to 8 descriptors can be stored in the on-chip descriptor RAM. The format of the descriptors in main memory is shown in Fig. 19.



X = undefined, reserved

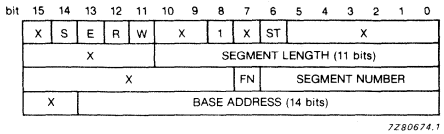
- Base Address: the 14 MSBs of the start address of this segment.
- V/P (Valid/Present) – may be used by the loading software to determine whether the segment is valid and present.
- S (Supervisor) – supervisor permission is required to access this segment.
- E (Execute) – instruction fetches may be performed with this segment.
- R (Read) – read operations may be performed with this segment.
- W (Write) – write operation may be performed with this segment.
- ST (Stack) – stack segments grow from high to low addresses.

Segment Length: the 11 bits define the length of a segment by the number of 1 Kbyte blocks. (If the SN bit of the MMU Control Register (MCR) is set, placing the MMU in mode 2, only 7 MSBs define the length of the segment.)

Note: All bits indicated as "undefined, reserved" must be programmed to zeros, except bit 8 of the first word which must be set to 1 to be compatible with the MACs in the 68000 family (68910 and 68920).

Fig.19 Format of descriptors in main memory.

The format of the descriptor in the on-chip descriptor RAM is shown in Fig. 20 (four consecutive words for each descriptor).



FN = FLUSH If this bit is equal to zero it invalidates the descriptor. Therefore, it must be reset to zero when writing a new valid segment number. The FN bit should be set to one after the remainder of the segment descriptor has been loaded into the MMU.

X = undefined, reserved; will return zeros when ready by the CPU.

Fig.20 Descriptor format in MMU.

The low-order byte of the third word contains the segment number that is loaded into the fully associative CAM. The Most Significant Bit of the Segment Number is in bit 6 of this word, i.e. it is left justified for either mode of the Segment Number.

MMU CONTROL AND STATUS REGISTERS

The format of the MMU's control (MCR) and the status (MSR) registers are shown in Fig. 21. The mnemonics used in Fig. 21 are defined in Table 20.

The registers can be accessed as either one word or two separate bytes. MCR is a read/write register, while MSR is read–only and a write to MSR will result in a normal bus cycle with no effect.

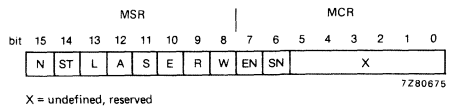


Fig. 21 MMU Status and Control Registers (MSR and MCR).

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Table 20 Control and status register bits

	bit number	symbol	description		
MSR	15	FN	Not–present	:	'1' addressed segment has no descriptor in the MMU (or FN = '0')
	14	ST	Stack segment	:	if set the segment grows from the highest to the lowest address
	13	L	Length violation	:	if set, a length violation has occurred
	12	A	Access error	:	if set, an attribute violation has occurred
	11	S	Supervisor bit	}	Reflects the descriptor attributes when an access error occurred
	10	E	Execute bit		
	9	R	Read bit		
	8	W	Write bit		
MCR	7	EN	Enable bit	:	'1' enables the MMU (address translation and protection)
	6	SN	Number of segments	:	'0' = mode 1; '1' = mode 2

ADDRESS MAP OF THE MMU

The internal addresses of the MMU's Control Register (MCR), Status Register (MSR), and Descriptor RAM are as follows:

Base address = 80008000 (HEX)

A6	A5	A4	A3	A2	A1	A0	
0	0	0	0	0	0	0	MSR
0	0	0	0	0	0	1	MCR
1	C	C	C	0	0	0/1	ATTR
1	C	C	C	0	1	0/1	SEG LENGTH
1	C	C	C	1	0	0	UNDEFINED, RESERVED
1	C	C	C	1	0	1	SEG NUMBER
1	C	C	C	1	1	0/1	BASE ADDR

Notation:
MSR = MMU Status Register
MCR = MMU Control Register
SEG = Segment
ATTR = Attributes
CCC = 000 to 111 (i.e. Segment Descriptors 0 to 7)

All internal MMU addesses are mapped in the 68070's on-chip address space (also see Tables 1 and 2) and are only accessible in supervisor mode. On-chip addresses are not processed by the MMU.

OPERATION

The MMU provides protection and virtual memory support. When the MMU is enabled, it only influences addresses sent by the CPU and adds two states (or one clock cycle) at the beginning of each external bus cycle of the CPU. However, during the vector acquisition of an interrupt acknowledge cycle, the MMU does not process the address coming from the CPU; i.e. logical address equals physical address.
If an error occurs within the enabled MMU (length or attribute violation, or segment not-present), the MMU inhibits data strobes (UDSN, LDSN) and asserts a bus error signal to both the CPU and the external world (BERRN). The address strobe (ASN) will still be asserted to indicate bus occupation to other possible bus masters. Then, the CPU will start bus error exception processing with the stack operation.

The address translation is processed as follows:

1) The segment number 'S' of the logical address is used to address the segment descriptor stored in the MMU on-chip descriptor RAM. If this segment descriptor is not valid or not present, a BERRN will be generated and corrective action must be taken to load the indicated segment descriptor and continue the interrupted instruction.

2) The displacement 'D' of the logical address is compared to the length attribute in the segment descriptor. If the displacement is outside the indicated length then a BERRN will be generated.

3) The internal function codes are used to check for access violations, using the attributes of the segment descriptor. In the case of violation a BERRN will be generated.

4) If no violations have been detected, a physical address will be generated. This address is constructed by adding the segment base address, the displacement 'D' and the offset 'O' bits, see figure 21(a).

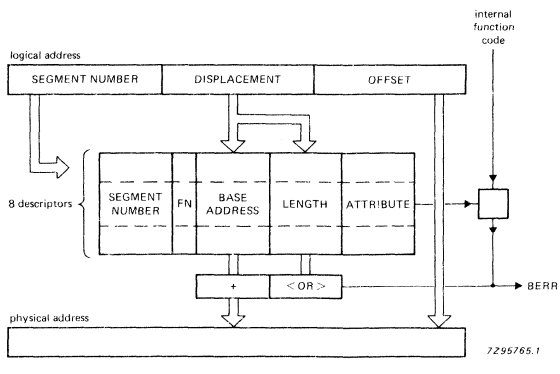


Fig.21(a) Principle of the MMU.

DMA CONTROLLER

GENERAL

The 68070 has on-chip, a two-channel DMA controller that handles byte or word operands and devices with port sizes of 8 or 16-bits. The channels can be programmed to transfer data in cycle-stealing (single cycle) or burst (a block of successive cycles) mode. Channel 1 always uses single addressing, while channel 2 can operate with single or dual addresses (memory to memory).

Typical system latency times are less than 2,5 µs and the maximum transfer rate (using single addressing) is 1,6 million transfers/s.

The 68070's DMA controller is a subset of the existing DMA controllers in the 68000 family (68430, 68440, and 68450) and is therefore software compatible with these devices.

BUS ARBITRATION AND PRIORITY RESOLUTION

The 68070 contains three possible bus masters, the DMA channels 1 and 2 and the CPU, where channel 1 has the highest priority, and the CPU the lowest. There can also be external bus masters which have a priority lower than channel 2 but higher than the CPU (which has the lowest priority in the system). The priority is defined by connecting a daisy-chain to the internal bus grant signal of the CPU, through the internal bus grant signals of channel 1 and channel 2, and then to the external devices.

When a valid transfer request is received from a device, the DMA controller will arbitrate for and acquire the bus. The DMA controller indicates to the CPU that it wants to become bus master by generating an internal bus request signal, and the CPU responds by sending an internal bus grant signal, daisy-chained through the DMA controller. In this case, it is not offered to the external devices because the DMA controller has a request pending. If BGN has already been offered to the external devices when a DMA request arrives, the DMA controller waits for BGACKN to be negated.

If the CPU is the current bus master, it will finish its current bus cycle and then give the bus to the DMA controller. When the DMA controller has received the internal bus grant signal, it waits for the external signals, Address Strobe (ASN) and Data Transfer Acknowledge (DTACKN), to become inactive before assuming bus ownership.

If the BRN signal is asserted by an external device when the CPU is not the bus master (i.e. BGACKN is asserted) no BGN signal will be sent until the CPU has regained the bus (i.e. BGACKN is negated).

DEVICE/DMA CONTROLLER COMMUNICATION

The following five signal lines let the peripheral devices and the DMA controller communicate (see the pin description for further details):

- Request (REQxN). The device makes a request for service by asserting the REQxN line. Either burst or cycle-stealing mode can be used.
- Acknowledge (ACKxN). The channel asserts the acknowledge line (which implicitly addresses the device making the request) during transfers to and from the device.
- Ready (RDYN). RDYN is an active-LOW input which is asserted by the requesting device in single-address mode.
- Device Transfer Complete. (DTCN). DTCN is an active-LOW output asserted by the DMA controller during device bus-cycles to indicate that the cycle has been completed successfully.
- Done (DONEN). DONEN is a bidirectional active-LOW signal. As an output, it indicates to the device that the memory transfer count is exhausted.
  As an input, it indicates that the operation will terminate after current operand has been transfered (also see Termination phase).

DMA CONTROL AND STATUS REGISTERS

Table 21 DMA controller address map

Base Address 80004000 (HEX)

Address bits [1), 2)]								Acronym	Register Name	Mode	Affected by RESET
7	6	5	4	3	2	1	0				
c	0	0	0	0	0	0	0	CSR	Channel Status Register	R/W[3)]	Yes
c	c	0	0	0	0	0	1	CER	Channel Error Register	R	Yes
c	c	0	0	0	0	1	0		Reserved		
c	c	0	0	0	0	1	1		Reserved		
c	c	0	0	0	1	0	0	DCR	Device Control Register	R/W	Yes
c	c	0	0	0	1	0	1	OCR	Operation Control Register	R/W	Yes
c	c	0	0	0	1	1	0	SCR	Sequence Control Register	R/W[4)]	Yes
c	c	0	0	0	1	1	1	CCR	Channel Control Register	R/W	Yes
c	c	0	0	1	0	0	0		Reserved		
c	c	0	0	1	0	0	1		Reserved		
c	c	0	0	1	0	1	0	MTCH	Memory Transfer Counter High	R/W	No
c	c	0	0	1	0	1	1	MTCL	Memory Transfer Counter Low	R/W	No
c	c	0	0	1	1	0	0	MACH	Memory Address Counter High	R/W[4)]	No
c	c	0	0	1	1	0	1	MACMH	Memory Address Counter Middle High	R/W	No
c	c	0	0	1	1	1	0	MACML	Memory Address Counter Middle Low	R/W	No
c	c	0	0	1	1	1	1	MACL	Memory Address Counter Low	R/W	No
c	c	0	1	0	0	d	d		Reserved		
c	c	0	1	0	1	0	0	DACH	Device Address Counter High	R/W[4), 5)]	No
c	c	0	1	0	1	0	1	DACMH	Device Address Counter Middle High	R/W[5)]	No
c	c	0	1	0	1	1	0	DACML	Device Address Counter Middle Low	R/W[5)]	No
c	c	0	1	0	1	1	1	DACL	Device Address Counter Low	R/W[5)]	No
c	c	0	1	1	d	d	d		Reserved		
c	c	1	0	0	d	d	d		Reserved		
c	c	1	0	1	0	d	d		Reserved		
c	c	1	0	1	1	0	1		Reserved		
c	c	1	0	1	1	0	1	CPR	Channel Priority Register	R/W[4)]	No
c	c	1	0	1	1	1	0		Reserved		
c	c	1	0	1	1	1	1		Reserved		
c	c	1	1	d	d	d	d		Reserved		

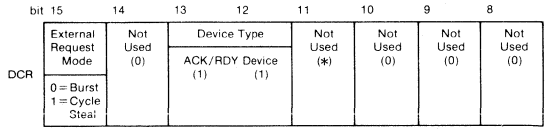
Notes: 1) 'cc' = 00 for channel 1, 'cc' = 01 for channel 2, 'cc' = 10 or 11 reserved.
2) 'd' designates don't care.
3) A write to this register may perform a status reset operation.
4) This is a dummy register present only to provide compatibility with other 68000 family DMA controllers. A write to this register has no effect on the DMA controller.
5) Channel 2 only.

To be compatible with other 68000 family DMA controllers, the control and status bits are mapped into bit positions equivalent to the register map of the other devices. Bits which are used in the other devices but not in the DMA controller are assigned default values. If upward compatibility with the other devices is required, the programmer should use these default values when writing control words into the registers although they have no effect in the DMA controller. When a register is read, the default value is returned regardless of the value used when the register was programmed. The default value is indicated by '(x)' in unused bit positions in the register formats that follow.

REGISTER FORMATS

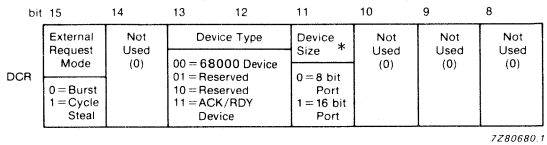
Device Control Register (DCR)

CHANNEL 1



* Must be 0 if OCR 5:4 = 00 (SIZE), otherwise 1. When read, the value of this bit is (OCR 5.OR.OCR 4).

CHANNEL 2



* This bit is programmable only when DCR 13:12 = 00 (68000 device). For DCR 13:12 = 11 (ACKx/RDY Device) the function is identical to channel 1.

Fig. 22 Device Control Registers (DCR).

External Request Mode (DCR 15)

This bit selects the Channel operation to either burst or cycle steal mode, as follows:

0 Burst Mode: This mode allows a device to request the transfer of multiple operands using consecutive bus cycles.

1 Cycle Stealing Mode: This mode allows a device to transfer operands on a per cycle basis.

Device Type (DCR 13:12)

These bits determine how the device is addressed, as follows:

CHANNEL 1

11 The device connected is implicitly addressed by the 5 device control signals with handshaking using ACKxN and RDYN.

CHANNEL 2.

00 The device is explicitly addressed by the Device Address Counter (DAC) via the 68070 bus interface. Transfers are made in two bus cycles and the data is stored in the CPU between bus cycles.

11 The connected device is implicitly addressed by the 5 device control signals with handshaking using ACKxN and RDYN.

Device Size (DCR 11, Channel 2 only)

This bit functions only with explicitly addressed devices, DCR 13:12 = 00.

0 The device port size is 8-bit, and the device reads/writes only using the low-order half of the bus (D0-D7) or the high-order (D8-D15) half depending on bit A0 of the Device Address Counter (DAC). Depending on which part of the bus is used either LDSN for the lower-order part or UDSN for the upper-order part is asserted. During byte size transfers (OCR 5:4 = 00) the half of the data bus used for read/write to the memory depends on the state of A0 of the Memory Address Counter (MAC).

During word size transfers (OCR 5:4 = 01), read/write operations to the device take place in two successive bytes; the DAC will either be unchanged or incremented by two per byte, depending on SCR 9:8 (see Fig. 24).

1 The device port size is 16-bit, and the device is accessed as a normal memory location.

Operation Control Register (OCR)

CHANNEL 1

	bit 7	6	5 4	3	2	1	0
OCR	Direction 0 = Mem. to Dev. 1 = Dev. to Mem.	Not Used (0)	Operand Size 00 = Byte 01 = Word (16-bit) 10 = Reserved 11 = Reserved	Not Used (0)	Not Used (0)	Not Used (1)	Not Used (0)

CHANNEL 2

	bit 7	6	5 4	3	2	1	0
OCR	Direction 0 = Mem. to Dev. 1 = Dev. to Mem.	Not Used (0)	Operand Size 00 = Byte 01 = Word (16-bit) 10 = Reserved 11 = Reserved	Not Used (0)	Not Used (0)	Not Used (1)	Not Used (0)

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Fig.23 Operation Control Registers (OCR).

Operand Size (OCR 5:4)

The value of these bits determines whether UDSN, LDSN or both are asserted during the transfer, and by what value the address counters MAC and DAC are incremented in each transfer cycle.

Sequence Control Register (SCR)

CHANNEL 1

	bit 15	14	13	12	11 10	9 8
SCR	Not Used (0)	Not Used (0)	Not Used (0)	Not Used (0)	MAC Count Up (0) (1)	DAC Not Used (0) (0)

CHANNEL 2

	bit 15	14	13	12	11 10	9 8
SCR	Not Used (0)	Not Used (0)	Not Used (0)	Not Used (0)	MAC 00 = No Change 01 = Count Up 10 = Reserved 11 = Reserved	DAC 00 = No Change 01 = Count Up 10 = Reserved 11 = Reserved

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Fig. 24 Sequence Control Registers (SCR).

Channel Control Register (CCR)

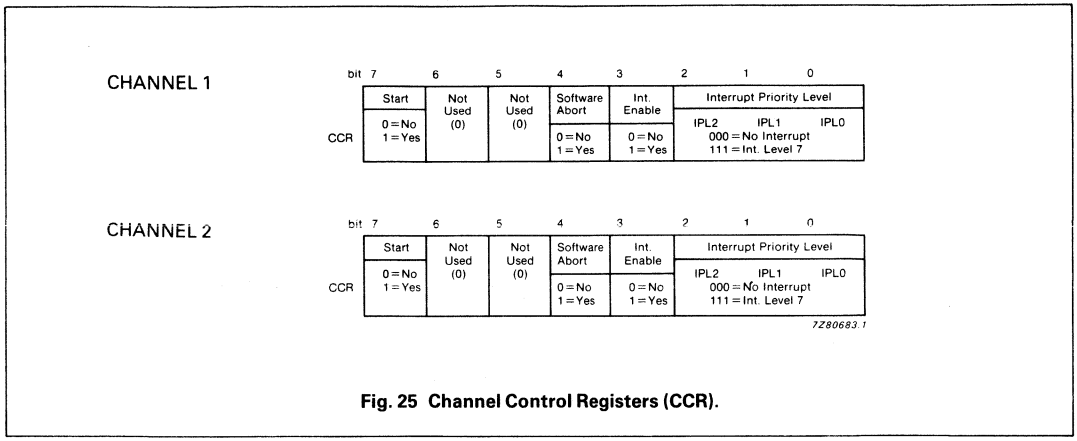

Fig. 25 Channel Control Registers (CCR).

Start Operation (CCR 7)

0 No Start pending.

1 Start Operation. The start bit is set to initiate channel operation.

Software Abort (CCR 4)

0 Do Not Abort.

1 Abort Operation. Setting this bit terminates the current operation and puts it into the idle state, then:

- The COC bit (CSR 15) and ERR bit (CSR 12) are set.
- The Channel Active bit (CSR 11) in the CSR is reset.
- An Abort Error condition is signalled in the CER.

Setting this bit causes a pending start to be reset. When reading CCR, this bit is always a zero.

Channel Status Register (CSR)

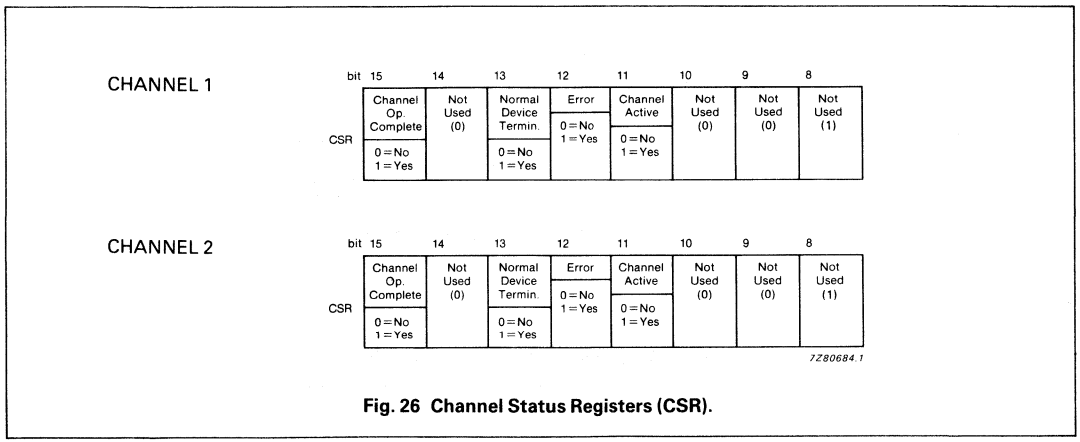

Fig. 26 Channel Status Registers (CSR).

Reading this register gives the status of the channel. The COC bit (CSR 15), NDT bit (CSR 13), and ERR bit (CSR 12) can be cleared by writing a '1' to the appropriate bit positions of the register. Writing a '0' to these bit positions has no effect.

Channel Error Register (CER)

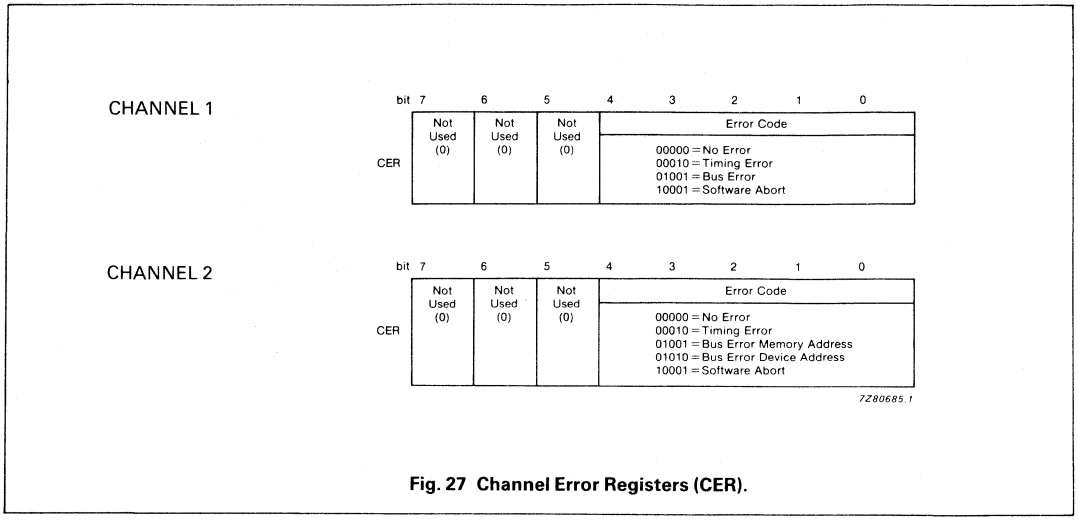

Fig. 27 Channel Error Registers (CER).

Error Code (CER 4:0)

This field indicates the source of the error when the ERR bit (CSR 12) is set. Clearing bit 12 of the CSR clears the contents of the Channel Error Register.
The error codes are:

00000 No Error.

00010 Timing Error. An attempt has been made to start the channel before all the bits of the CSR had been cleared.

01001 Bus Error memory side. A bus error (BERRN asserted without HALTN) occured during the cycle with MAC presenting the address.

01010 Bus Error device side. A bus error (BERRN asserted without HALTN) occurred during the cycle with DAC presenting the address (channel 2 only).

10001 Software Abort. The channel operation was terminated by a Software Abort command (CCR 4).

Channel Priority Register (CPR)

CHANNEL 1

	bit 7	6	5	4	3	2	1	0
CPR	Not Used (0)	Not Used (0)	Not Used (0)	Not Used (0)	Not Used (0)	Not Used (0)	Priority (0)	(0)

CHANNEL 2

	bit 7	6	5	4	3	2	1	0
CPR	Not Used (0)	Not Used (0)	Not Used (0)	Not Used (0)	Not Used (0)	Not Used (0)	Priority (0)	(1)

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Fig. 28 Channel Priority Registers (CPR).

Memory Address Counter (MACH, MACMH, MACML, MACL)

The 32-bit memory address counter defines a memory location as the first source operand to be transferred or its destination, depending on the direction of the transfer.

Only the least significant 24 bits of the counter (MACMH, MACML, and MACL) are implemented in the DMA controller.

Device Address Counter (DACH, DACMH, DACML, DACL) – Channel 2 only

The 32-bit device address counter defines a device location as the source of the first operand to be transferred or its destination, depending on the direction of the transfer.
Only the least significant 24 bits of the counter (DACMH, DACML, and DACL) are implemented in the DMA controller.

Memory Transfer Counter (MTCH, MTCL)

The 16-bit memory transfer counter defines the number of operands to be transferred by the channel.

OPERATION

The operation of the DMA channels can be divided into three phases:

- Initialization,
- Transfer, and
- Termination.

Initialization

After programming the Channel Control Registers (CCR), the memory and device address counters, and the memory transfer counter, the CPU sets the START bit (CCR 7). The channel initializes the operation by clearing any pending requests, clearing the START bit, and setting the Channel Active bit in the Channel Status Register (CSR). The channel is then ready to receive valid requests for an operation.

Transfer phase

The actual transfer of data between the device and the memory occurs during this phase in one of two ways. In single address mode, the transfers occur during a single bus cycle, while in double address mode, each transfer is performed with a read and a write bus cycle.

Termination phase

The termination phase of the block transfer occurs under the following conditions.

Count Termination

As a part of operand transfer, the channel decrements the Memory Transfer Counter (MTC). When this counter has been decremented to zero, it indicates that this is the last operand transfer and that the channel operation is complete. DONEN is asserted, CSR 11 is cleared and CSR 15 is set.

Device Termination

The channel monitors the state of the DONEN line while acknowledging a device transfer request. If the device asserts DONEN, the channel will terminate the operation after transferring the current operand. CSR 11 is cleared, and CSR 13 and CSR 15 are set.

Software Abort

The Software Abort bit (CCR 4) allows the CPU to abort the current channel operation (see description of CCR 4).

Bus error treatment

If both the BERRN and HALTN signals are asserted during a DMA controller cycle, the DMA controller will enter the RERUN state.

If only the BERRN signal is asserted during a DMA controller cycle, the channel stops DMA controller operation, releases the bus, sets the ERR (CSR 12) and COC (CSR 15) bits in the CSR, clears the Channel Active bit (CSR 11) in the CSR, and sets the error code in the CER to indicate a bus error.

Reset

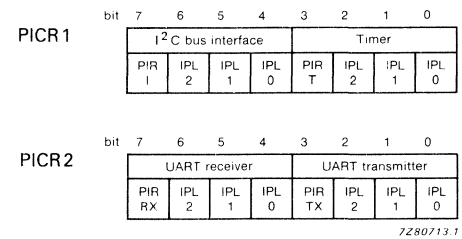
Via RESET, external sources and CPU programs can reset and initialize the DMA controller. If the DMA controller is the bus master when reset is detected, it releases the bus and resets all the bits of the status registers (except CSR 8) to zero.

Interrupts

If the Interrupt Enable bit (CCR 3) is set, the channel will send an interrupt when it terminates an operation (COC bit set – CSR 15). The priority level of the interrupt is given by the IPL bits in the CCR. During the interrupt acknowledge cycle, the channel requests an autovector and thus the IPL bits correspond directly to the vector used.

PERIPHERAL INTERRUPT CONTROL

The I^2C and UART serial interfaces, and the Timer, use a common set of Peripheral Interrupt Control Registers PICR. These registers are memory mapped on the on-chip bus and communicate with the CPU of the 68070.



I^2C I^2C serial bus interface.
UART UART serial interface.
RX UART receiver.
TX UART transmitter.
TIMER Timer functions.

IPL Interrupt priority level of interrupts requested by the I^2C, UART or Timer. IPL2 is the MSB and IPL0 is the LSB. All values are positive true; IPL = 111 represents priority level 7 and IPL = 000 will inhibit the interrupts.

PIR Pending Interrupt Reset, when set to 1 any pending interrupts of the respective peripheral will be reset. Note that this does not reset the interrupting status of a peripheral and further, if the IPL bits are changed without setting the PIR bit then spurious interrupts may occur. Reading the PIR bits will return a 0.

note: Initially and after RESET, all PICRx bits are cleared to zero.

Fig.29 Peripheral Interrupt Control Registers (PICR).

THE I²C SERIAL BUS INTERFACE

The 68070 contains an inter-IC (I²C) serial interface bus. The I²C-bus can be used in a master or slave mode, and can be connected to up to 128 different peripheral ICs, each with a unique device address. Maximum transmission speed is 100 kbits/s.

Communication with the bus is via two dedicated pins, SCL, serial clock and SDA, serial data. The interface can generate interrupts with priority programmed to one of 7 levels. A complete data transfer on the I²C-bus is shown in Fig. 30.

I²C Data Register (IDR)

The data register IDR performs the conversion between the serial and parallel data formats. Data to be transmitted is loaded into IDR by the CPU and is shifted out serially (MSB first), and data received on the serial bus is shifted into IDR (MSB first).

I²C Address Register (IAR)

The address register holds the slave address allocated to the device in its 7 MSB's. It is only written to by the CPU and remains unchanged until rewritten. The LSB is the Always Selected bit (ALS) which when set to 1 will disable the address recognition so the I²C-bus interface will respond to all addresses.

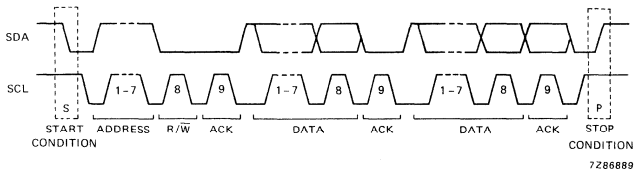


Fig. 30 A complete data transfer on the 1²C bus.

OPERATING MODES

The CPU can operate in the following modes with the serial I²C-bus.

- master transmitter (MTX).
- master receiver (MRX).
- slave transmitter (STX).
- slave receiver (SRX).

THE 68070'S I²C-BUS I/O REGISTERS

The communication between the 68070's CPU and I²C-bus interface is via a set of registers and an interrupt request facility. All I²C registers are accessible by read or write operations. The data and information controlling the operation of the interface is stored in the following five registers (that are fully transparent and memory mapped to the CPU):

Base address: 8000 2001 (HEX)

A3	A2	A1	A0*	
0	0	0	1	I²C Data Register (IDR)
0	0	1	1	I²C Address Register (IAR)
0	1	0	1	I²C Status Register (ISR)
0	1	1	1	I²C Control Register (ICR)
1	0	0	1	I²C Clock Control register (ICC)

* Note: All location with A0 = 0 are undefined/reserved.

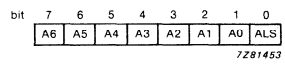


Fig. 31 I²C Address Register (IAR).

I²C Status Register (ISR)

Status register ISR contains all the information concerning the status of the I²C-bus interface, and all its bits can be written and read by the CPU. The functions of the status bits illustrated in Fig. 32 are given below.

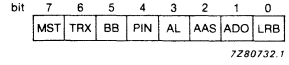


Fig. 32 I²C Status Register (ISR).

DEVELOPMENT DATA

MST = Master

If this bit is 1, the I²C-bus interface is in the master mode and it generates clock pulses on SCL for transmission or reception timing of serial data. If the MST bit is 0, the I²C-bus interface is in the slave mode and the clock pulses are received from the master on SCL.

TRX = Transmitter

If this bit is 1, the I²C–bus interface is in the transmitter mode and data in the IDR register is shifted out onto the data line SDA, synchronized with the clock pulses on SCL. If this bit is 0, the I²C-bus interface is in the receiver mode and data on the data line SDA is shifted into the IDR synchronized with the clock pulses on SCL.

BB = Bus Busy

This bit indicates the state of the serial bus; if 0, the bus is free and if 1, the bus is busy.

PIN = Pending Interrupt Not

The PIN bit is set to 0 every time an I²C-bus interrupt is requested. Any access to IDR will reset PIN bit to 1.

AL = Arbitration Lost

The AL bit indicates that, as a master transmitter, the arbitration procedure on the bus was lost.

AAS = Addressed As Slave

AAS is set to 1 when the address comparator recognizes either its own slave address, the general call address (8 zeros) or any address if ALS = 1. It is reset to 0 by any access to IDR.

AD0 = Address Zero

AD0 is set to 1 if the address comparator detects the general call address (8 zeros). It is reset to 0 when a STOP condition is detected.

LRB = Last Received Bit

The LRB position in ISR of a transmission contains the receiver acknowledge bit. When it is 0, the reception of the transmission has been acknowledged.

I²C Control Register (ICR)

Some additional functions of the interface can be controlled with the flags in the control register ICR as shown in Fig. 33.

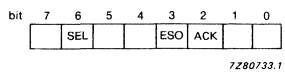


Fig.33 I²C Control Register (ICR).

SEL = Selected

The SEL bit is set automatically in the slave mode, together with the AAS bit in ISR and remains at 1 during the whole transfer. It is reset when a STOP or repeated START condition is detected.

ESO = Enable I²C-bus

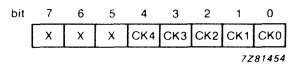
If the ESO bit is set, the I²C-bus interface is enabled and when it is reset the I²C-bus is disabled. Only the CPU can alter the ESO bit.

ACK = Acknowledge

- ACK = 1 Reception will be acknowledged by a '0' bit.
- ACK = 0 Reception will not be acknowledged, a '1' bit is sent.

I²C Clock Control register (ICC)

By programming the 5 LSBs of the clock control register, the frequency of SCL and SDA can be adapted to the needs of the I²C-bus or the 68070's system clock. After initialization or RESET, bits CK4 to CK0 are cleared to zero and must be programmed to a non-zero value before the I²C interface is enabled.



X = undefined, reserved. Reading these bits will return a 1.

Fig.34 I²C Clock Control register (ICC).

Table 22 I^2C-bus interface divisors

CK4 - CK0 (HEX)	divisor	approximate SCL** frequency (kHz)
0	illegal	–
1	78	126,025*
2	90	109,222*
3	102	96,372
4	126	78,015
5	150	65,533
6	174	56,494
7	198	49,464
8	246	39,959
9	294	33,435
A	342	28,742
B	390	25,205
C	486	20,266
D	582	16,890
E	678	14,498
F	774	12,700
10	996	10,175
11	1158	8,488
12	1350	7,281
13	1542	6,374
14	1926	5,103
15	2310	4,255
16	2694	3,648
17	3078	3,193
18	3846	2,555
19	4614	2,130
1A	5382	1,826
1B	6150	1,598
1C	7686	1,278
1D	9222	1,065
1E	10758	0,913
1F	12294	0,799

* Maximum bus clock frequency in I^2C systems is 100 kbits/s.

** crystal or clock input frequency = 19,6608 MHz

DEVELOPMENT DATA

UART SERIAL INTERFACE

The UART serial interface is a universal asynchronous data communication controller that interfaces directly with the CPU and can be used in either polled or interrupt driven modes. It accepts programmed instructions from the CPU while supporting asynchronous serial data communication in either full or half-duplex mode. The interface then converts data received from the CPU into a serial form for transmission, and simultaneously, it can receive serial data and convert it to parallel data as input to the CPU. The baud rate generator can be programmed to generate independant transmit/receive baud rates by either using the 68070's system clock, or accepting an external clock via the XCKI input.

FUNCTIONAL BLOCKS

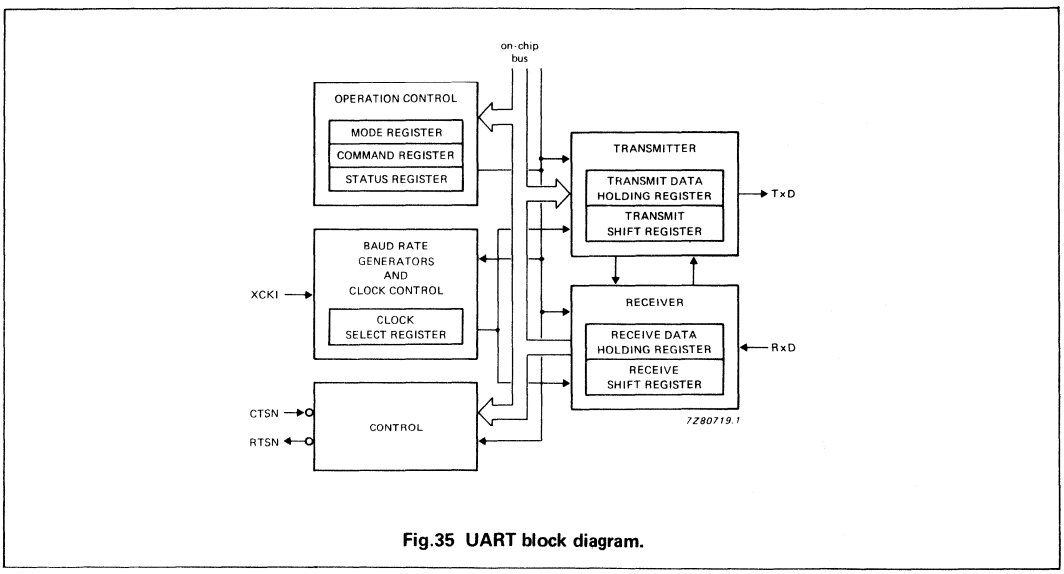


Fig.35 UART block diagram.

PROGRAMMING

Before initiating data communication, the UART operation mode must be programmed by writing to the mode, clock select and command registers. The UART interface can be re-configured at any time during program execution, but when writing to the mode and clock select registers the transmitter and receiver should be disabled.

Table 23 UART register addressing

Base Address = 8000 2011

A3	A2	A1	A0*	Function
0	0	0	1	UART Mode Register (UMR)
0	0	1	1	UART Status Register (USR)
0	1	0	1	UART Clock Select (UCS)
0	1	1	1	UART Command Register (UCR)
1	0	0	1	UART Transmit Holding Register (UTH)
1	0	1	1	UART Receive Holding Register (URH)
1	1	0	1	undefined, reserved
1	1	1	1	undefined, reserved

* Note, all locations with A0 = 0 are undefined, reserved.

DEVELOPMENT DATA

UART Mode Register (UMR)

bit 7	6	5	4	3	2	1	0
Channel mode		Not used	CTSN enable TxD	Parity control	Parity type	Stop bit length	Character length
00 = normal 01 = auto echo 10 = local loopback 11 = remote loopback		(1)	0 = no CSTN control 1 = CSTN control TxD	0 = inhibited 1 = enabled	0 = odd 1 = even	0 = one stop bit 1 = two stop bits	0 = seven bits 1 = eight bits

7Z81455

UMR 0 selects the character length (7 or 8 bits). This does not include the parity bit (if programmed) or the START/STOP bits.

UMR 1 selects the number of STOP bits; either 1 or 2.

UMR 2 selects either odd or even parity when parity has been enabled by UMR 3.

UMR 3 controls the parity generation and when enabled, a parity bit is added to the transmitted character and the receiver performs a parity check on the incoming data.

UMR 4 determines if the CTSN line controls the operation of the transmitter.

UMR 7:6 = 00 is the normal mode, with transmitter and receiver operating independently.

UMR 7:6 = 01 places the UART in auto echo mode, which automatically retransmits the received data.

UMR 7:6 = 10 selects local loopback mode.

UMR 7:6 = 11 selects the remote loopback mode.

Fig.36 UART Mode Register (UMR).

All bits of the mode register UMR 7:0 are cleared by a RESETN signal or a RESET instruction issued by the CPU, with the exception of the UMR 5 which always returns a 1 when read.

UART Clock Select register (UCS)

bit 7	6 5 4	3	2 1 0
Clock source	Receiver clock select	Not used	Transmitter clock select
	bit rate divisor		bit rate divisor
0 = internal (default after RESETN)	000 = 75 baud 65536 001 = 150 32768 010 = 300 16384 011 = 1200 4096 100 = 2400 2048 101 = 4800 1024 110 = 9600 512 111 = 19200 256	(1)	000 = 75 baud 65536 001 = 150 32768 010 = 300 16384 011 = 1200 4096 100 = 2400 2048 101 = 4800 1024 110 = 9600 512 111 = 19200 256
1 = external			

7Z81456

Fig.37 UART Clock Select Register (UCS).

The UCS register allows selection of the clock source and the baud rate for receiver and transmitter; as shown above. The baud rates given above are generated when either a 19,6608 MHz clock is used as the 68070's XTAL1 clock (source = internal) or a 4,1952 MHz clock is applied to XCKI (source = external). Other frequencies will give a different set of baud rates. Note that when using the 68070's XTAL1 clock, it is pre-divided by 4.

UCS 7 selects the clock source for the receiver and transmitter baud rates. After RESET, the clock source is the on-chip clock and with a 19,6608 MHz crystal, the listed baud rates are available. An external clock source (XCKI) is selected if UCS 7 = 1. The maximum frequency that can be applied to XCKI is 5 MHz.

All bits of the clock select register are cleared by a RESETN signal, or by a RESET instruction issued by the CPU.

UART Command Register (UCR)

bit 7	6 5 4	3 2	1 0
Not used	Command field	TxD control	RxD control
(1)	see text for detail	01 = enable 10 = disable 00 = illegal 11 = illegal	01 = enable 10 = disable 00 = illegal 11 = illegal

7Z81457

Fig. 38 UART Command Register (UCR).

UCR is used to write commands to the UART.

UCR 6:4 = Miscellaneous commands.

The encoded value of this field may be used to specify a single command as follows:

000 No command
001 No command
010 Reset receiver - resets the receiver as if a hardware reset had been applied. The receiver is disabled.
011 Reset transmitter - resets the transmitter as if a hardware reset had been applied.
100 Reset error status - clears the received break, parity error, framing error, and overrun error bits in the status register USR 7:4.
101 No command
110 Start break - forces the TxD output LOW (spacing).
111 Stop break - The TxD line will go HIGH (marking) whithin two bit times. TxD will remain HIGH for one bit time before the next character, if any, is transmitted.

All bits of the command register UCR 7:0 are cleared by a RESETN signal, or by a RESET instruction issued by the CPU, with the exception of UCR 7 which is not used and always returns a 1 when read.

UART Status Register (USR)

bit	7	6	5	4	3	2	1	0
	Received break	Framing error	Parity error	Overrun error	TXEMT	TXRDY	Not used	RXRDY
	0 = no 1 = yes	0 = no 1 = yes	0 = no 1 = yes	0 = no 1 = yes	0 = no 1 = yes	0 = no 1 = yes	(1)	0 = no 1 = yes

7Z81458

TxEMT = Transmitter Empty
TxRDY = Transmitter Ready
RxRDY = Receiver Ready

Fig.39 UART Status Register (USR).

All status bits USR 7:0 are cleared by a RESETN signal, or a RESET instruction issued by the CPU, with the exception of USR 1 which is not used and always returns a 1 when read.

TIMER

The 68070's Timer comprises a 16-bit reference timer with an auto-reload register, and two identical (independently function-programmable) 16-bit registers. Clock period of the reference timer, and hence the maximum resolution, is 96/CKOUT(in MHz) μs. Two programmable I/O lines provide the necessary connection to external circuitry.

Three modes can be selected:

- match or pulse-generator mode which changes the output state when there is a match between the reference and register values.
- count mode which counts external events that occur at the T1 (T2) input.
- capture mode which stores the reference timer value in a capture register when an external event occurs at the T1 (T2) input.

Any transition on the inputs to T1 or T2 can be programmed as an external event.

TIMER PROGRAMMING

The address map of the Timer is shown below:

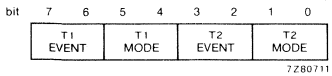
Base address = 80002020 (HEX)

A3	A2	A1	A0	REGISTER	
0	0	0	0	Timer Status Register	TSR
0	0	0	1	Timer Control Register	TCR
0	0	1	0	Reload Register HIGH	RRH
0	0	1	1	Reload Register LOW	RRL
0	1	0	0	Timer 0 HIGH	T0H
0	1	0	1	Timer 0 LOW	T0L
0	1	1	0	Timer 1 HIGH	T1H
0	1	1	1	Timer 1 LOW	T1L
1	0	0	0	Timer 2 HIGH	T2H
1	0	0	1	Timer 2 LOW	T2L

The CPU can read from and write to all the Timer registers and they can be accessed "on the fly".

DEVELOPMENT DATA

Timer Control Register (TCR)



EVENT - Control for external events monitored to trigger a function in Timer registers T1 or T2.

00 - Input inhibited.
01 - LOW-to-HIGH transitions will be monitored.
10 - HIGH-to-LOW transitions will be monitored.
11 - Any transition will be monitored.

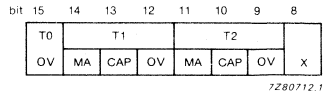
MODE - Control for the function of the Timer registers T1 or T2.

00 - Timer inhibited.
01 - Match Mode. A match between the reference timer T0 with the respective Timer register will reset output T1 or T2. Each overflow of T0 will set output T1 or T2. The I/O port of the Timer is automatically switched to output mode.
10 - Capture Mode. When an external event occurs (as described above), the contents of the reference timer T0 will be stored in the Timer register T1 or T2.
11 - Event Counter Mode. When an external event occurs the Timer register T1 or T2 will be incremented.

Fig.40 Timer Control Register (TCR).

Timer Status Register (TSR)

The Timer Status Register (TSR) indicates which timer and what specific event occured that caused an interrupt (if enabled) and can be read or written by the CPU. After being read, each bit of this register should be reset by software as an acknowledge of the read because the status bits are automatically set but are not reset by the Timer.



OV - Overflow. The Timer counts from FFFF (HEX) to 0000 (HEX). This bit will be set by timers T1 and T2 in event-counter mode only.
MA - Match. A match between the value stored in Timer registers T1 or T2 and the value of the continuous timer T0 occurred (in match mode).
CAP - Capture. When an external event occurs the current value of the continuous timer (T0) is stored into timer T1 or T2 (in capture mode).
X - *Undefined, reserved.*

Fig.41 Timer Status Register (TSR).

REFERENCE TIMER

The reference timer (T0) will increment by 1 (starting from the value initially loaded into T0H and T0L). Using a crystal frequency of 19,6608 MHz the 68070 will increment every 9,766 µs (or 96 CKOUT cycles). When T0 reaches FFFF, the OV flag in the status register is set and the reload register (RR) is loaded into T0. T0 will then start incrementing again until the next overflow occurs.

ELECTRICAL SPECIFICATION

ABSOLUTE MAXIMUM RATINGS[1,2,3]

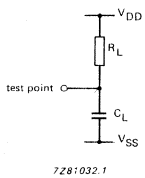
Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	range	unit
Input voltage on any pin with respect to ground (V_{SS})	V_I	−0,3 to +7,0	V
Input, output current	$\pm I_I, I_O$ max.	t.b.f.	mA
Total power dissipation	P_{tot} max.	2	W
Storage temperature range	T_{stg}	−55 to +150	°C
Operating ambient temperature range	T_{amb}	0 to +70	°C

Notes

1. Stresses above those listed in the Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and do not mean that the device will operate at these or other conditions above those given in the operation section.
2. For operating at elevated temperatures, the device must be derated based on a 150°C maximum junction temperature.
3. This product includes circuitry specifically designed to protect its internal devices from excessive static charge. Nevertheless, it is recommended that conventional precautions be taken to avoid applying any voltage above the rated maxima.
4. Parameters are valid over specific temperature range.
5. All voltages are measured with ground as reference (GND). For testing, all input signals swing between 0,4 and 2,4 V with a transition time of t.b.f.maximum. All time measurements are made with input voltages of 0,8 and 2,0 V and output voltages of 0,8 and 2,0 V as appropriate.
6. On clock input XTAL1 when an external clock is used.
7. All timing measurements have CKOUT as a reference for both internal oscillator and external clock input modes. The device has been designed to be used with a 19,6608 MHz crystal, but the minimum crystal frequency specified is 8 MHz. All timing measurements except number 1 are specified at 19,6608 MHz.
8. Actual value depends on clock period.
9. After V_{DD} has been applied for 100 ms.
10. If the asynchronous setup time (#41) requirements are met, the DTACKN LOW-to-data setup time (#31) requirements can be ignored. The data must only satisfy the data-in to clock-LOW setup time (#27) for the following cycle.
11. If the asynchronous setup time (#41) requirements are met, for both DTACKN and BERRN, then #42 may be 0 ns.
12. All timing diagrams should only be referred to in regard to the edge-to-edge measurements of the timing specifications. They are not intended as a functional description of the input and output signals. Refer to the functional description and related diagrams for device operation.

t.b.f. = to be fixed

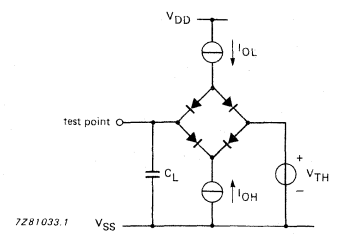


test point	R_L (kΩ)	C_L (pF)
RESETN	1	130
HALTN	1	130
SDA	2	400
SCL	2	400
BGACKN	1	130
DONEN	1	130
BERRN	1	130

Fig. 42 Open drain, bi-directional test loads.

DC CHARACTERISTICS V_{DD} = 5,0V ± 10%, V_{SS} = OV; T_{amb} = 0 to 70°C (see Figures 42, 43)[4,5]

parameter		test conditions	limits min.	limits max.	unit
V_{IH}	Input voltage HIGH, all inputs except XTAL1, XTAL2, SDA, SCL		2,0	V_{DD}	V
	XTAL1		$0,8V_{DD}$	V_{DD}	V
	SDA, SCL		3,0	V_{DD}	V
V_{IL}	Input voltage LOW, all inputs except SDA, SCL		V_{SS}–0,3	0,8	V
	SDA, SCL		V_{SS}–0,3	1,5	V
I_{in}	Input leakage current RTSN, CTSN, XCKI,BRN, DTACKN,INT1N, INT2N, REQ1N, REQ2N, RDYN, IN2N, IN4N, IN5N, NMIN, AVN, and XTAL1	V_{DD} = 5,25 V		20	µA
I_{TSI}	Three-state (off-state) input current A1-A23, D0-D15, ASN, LDSN, R/WN, UDSN, T1, and T2	Vin=2,4/0,4 V		20	µA
I_{ODI}	Open-drain (off-state) input current BGACKN, RESETN, HALTN, BERRN, DTCN, DONEN, SCL, and SDA			20	µA
V_{OH}	Output voltage HIGH CKOUT	I_{OH} = 400 µA	$0,8V_{DD}$		V
	A1–A23, D0–D15, ASN, BGN, LDSN, R/WN, UDSN, T1, T2, TXD, RTSN, ACKN1N, ACKN2N and IACKN2,4,5,7N		2,4		V
V_{OL}	Output voltage LOW HALTN, BERRN, IACKN2,4,5,7N,A1–A23, BGN, BGACKN, ACKN1N, ACKN2N, RESETN, T1, T2, TXD, RTSN, ASN, D0–D15, LDSN,R/WN, UDSN, DTCN, DONEN	I_{OL} = 3,2 mA		0,5	V
	CKOUT	I_{OL} = 3,2 mA		0,45	V
	SDA and SCL	I_{OL} = 5,0 mA		0,45	V
I_{DD}	Current consumption	CKOUT freq. = 10MHz		tbf	mA
C_{in}	Capacitance	V_{in} =0V, T_{amb} = 25°C frequency=1 MHz		20	pF



C_L = 130 pF (including all parasitics) exept CKOUT for which C_L = 50 pF

V_{TH} = 1,6 V system load threshold voltage at which dynamic loads (I_{OL} and I_{OH}) switch; see d.c. characteristics

Fig.43 Remaining test loads.

DEVELOPMENT DATA

AC CHARACTERISTICS

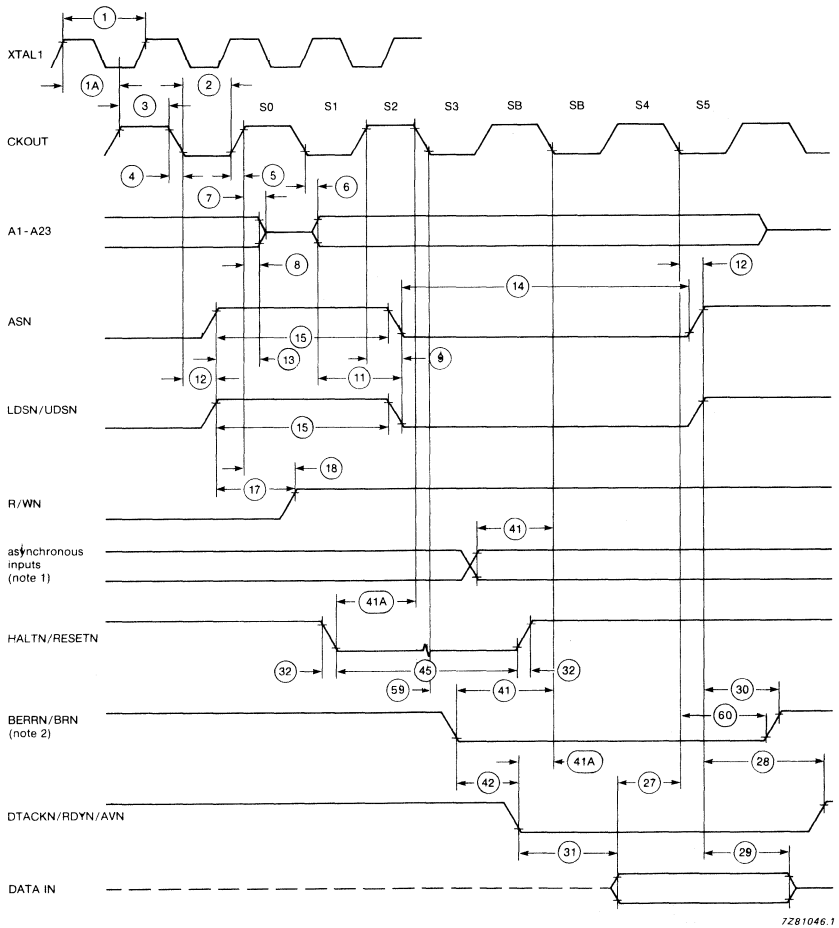
Crystal frequency = 19,6608 MHz, V_{DD} = 5V ± 10%, V_{SS} = 0V, T_{amb} = 0 to 70°C, C_{load} on CKOUT = 50 pF (see Fig. 44 to 47).

number	parameter	symbol	tentative limits min.	tentative limits max.	unit
1	Crystal or input (XTAL1) clock period	t_{CYC}	50	125	ns
1A	XTAL HIGH to CKOUT HIGH or LOW		8	96	ns
2	CKOUT, LOW level	t_{COL}	33		ns
3	CKOUT, HIGH level	t_{COH}	33		ns
4	CKOUT fall-time	t_{COf}		10	ns
5	CKOUT rise-time	t_{COr}		17	ns
6	CKOUT LOW to address valid	t_{CLAV}		60	ns
7	CKOUT HIGH to address/data, high-impedance(maximum)	t_{CHAZx}		15	ns
8	CKOUT HIGH to address invalid (minimum)	t_{CHAZn}	0		ns
9	CKOUT HIGH to ASN, DSN LOW	t_{CHSL}	0	45	ns
11[8]	Address to ASN/DSN (read), ASN (write) LOW	t_{AVSL}	8		ns
12	CKOUT LOW to ASN, DSN HIGH	t_{CLSH}	−5	45	ns
13[8]	ASN, DSN HIGH to address invalid	t_{SHAZ}	7		ns
14[8]	ASN/DSN (read), ASN (write) LOW level	t_{SL}	200		ns
14A[8]	DSN LOW level (write)	t_{DSL}	100		ns
15	ASN, DSN HIGH level	t_{SH}	100		ns
16	CKOUT HIGH to ASN, DSN high-impedance	t_{CHSZ}		32	ns
17[8]	ASN, DSN HIGH to R/WN HIGH (read)	t_{SHRH}	9		ns
18	CKOUT HIGH to R/WN HIGH	t_{CHRH}	0	55	ns
20	CKOUT HIGH to R/WN LOW (write)	t_{CHRL}		55	ns
21[8]	Address valid to R/WN LOW (write)	t_{AVRL}	0		ns
22[8]	R/WN LOW to DSN LOW (write)	t_{CLSL}	55		ns
23	CKOUT LOW to data-out valid (write)	t_{CLDO}		50	ns
25[8]	ASN, DSN HIGH to data-out invalid (write)	t_{SHDO}	20		ns
26[8]	Data-out valid to DSN LOW (write)	t_{DOSL}	8		ns
27[10]	Data-in to clock LOW (setup time, read)	t_{DICL}	41		ns
28[8]	ASN, DSN HIGH to DTACKN, RDYN, AVN HIGH	t_{SHDAH}	0	150	ns
29	ASN, DSN HIGH to data invalid (hold time, read)	t_{SHDI}	15		ns
30	ASN, DSN HIGH to BERRN HIGH	t_{SHBEH}	0		ns
31[8]	DTACKN LOW to data in (setup time, read)	t_{DCLDI}		62	ns
32	HALTN and RESETN input transition time	t_{RHrf}	0	200	ns
33	CKOUT HIGH to BGN LOW	t_{CHGL}		45	ns
34	CKOUT HIGH to BGN HIGH	t_{CHGH}		55	ns
35	BRN LOW to BGN LOW	t_{BRLGL}	1,5	3,5 +80 ns	c.p.

AC CHARACTERISTICS (cont).

number	parameter	symbol	tentative limits min.	tentative limits max.	unit
36	BRN HIGH to BGN HIGH	t_{BRHGH}	1,5	2,5 +80 ns	c.p.
37	BGACKN LOW to BGN HIGH	t_{GALGH}	1,5	3,5 +80 ns	c.p.
38	BGN LOW to bus high-impedance (ASN HIGH)	t_{GLZ}	15		ns
39	BGN HIGH level	t_{GH}	1,5		c.p.
40	BGACKN width	t_{BGL}	1,5		c.p.
41[10]	Asynchronous input setup time	t_{ASI}	35		ns
41A	Asynchronous input setup time for DTACKN, AVN, BERRN, HALTN, RDYN	t_{ASDT}	35		ns
42[11]	BERRN (input) LOW to DTACKN LOW	t_{BELDAL}	35		ns
43	CKOUT HIGH to Data Out invalid (write)	t_{CHDO}	0		ns
44	R/WN LOW to data bus driven	t_{RLDO}	3		ns
45	HALTN/RESETN pulse width	t_{HRPW}	10		c.p.
46	REQx setup before CKOUT LOW		35		ns
47	ACKxN LOW from CKOUT HIGH		0	45	ns
48	REQx hold after CKOUT LOW		10		ns
49	DTCN LOW from CKOUT HIGH			45	ns
50	ASN, LDSN, UDSN HIGH from DTCN LOW		−5		ns
51	ACKxN HIGH from CKOUT HIGH			55	ns
52	DTCN non-active from CKOUT HIGH			45	ns
53	DONEN (output) LOW from CKOUT HIGH			45	ns
54	DONEN (output) non-active from CKOUT HIGH			45	ns
56	DONEN (input) setup LOW before CKOUT LOW		35		ns
57	DONEN (input) hold LOW after CKOUT HIGH		10		ns
58	REQ LOW to BGACKN (output) LOW		2,5		c.p.
59	CKOUT LOW to BERRN (output) LOW			50	ns
60	CKOUT LOW to BERRN (output) non-active			45	ns
61	CKOUT HIGH to BGACKN (output) LOW			50	ns

DEVELOPMENT DATA



Notes

1. Setup time for the asynchronous inputs and AVN guarantees their recognition at the next falling edge of the clock.

2. BRN need fall at this time only to ensure being recognized at the end of this bus cycle.
   When BERRN is driven during a faulty MMU cycle, an additional error cycle (SE) is inserted in between SB and S4.

Fig.44 Read cycle timing.

DEVELOPMENT DATA

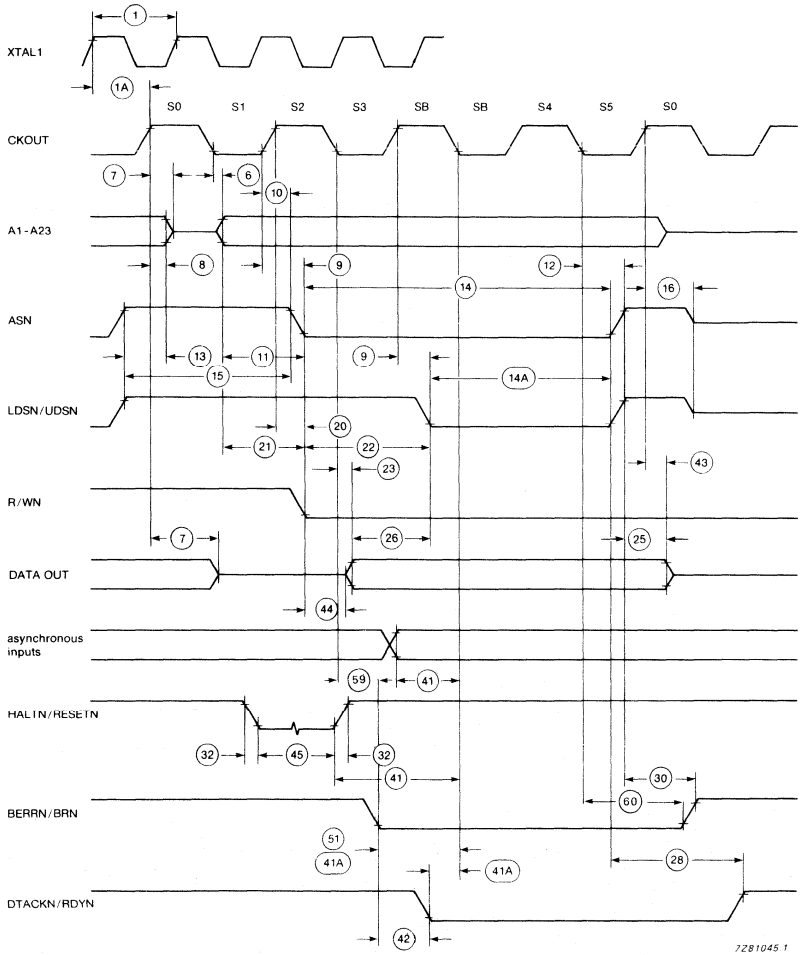


Fig.45 Write cycle timing.

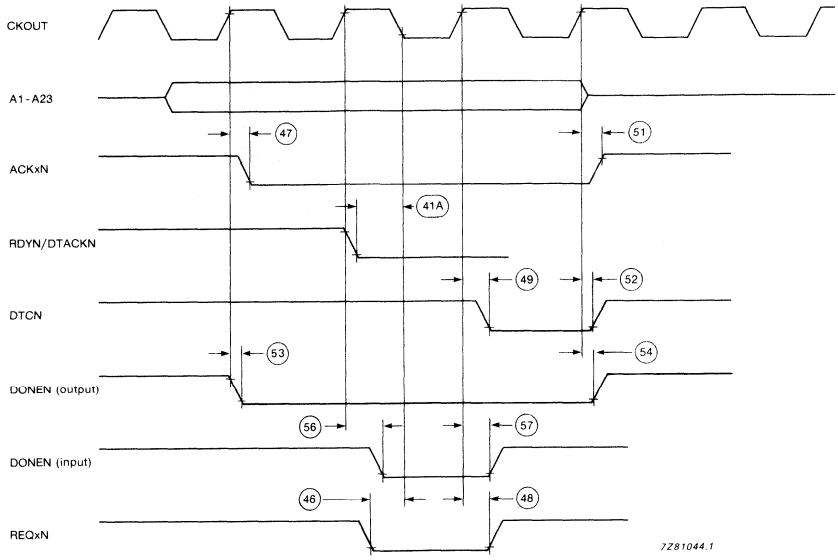
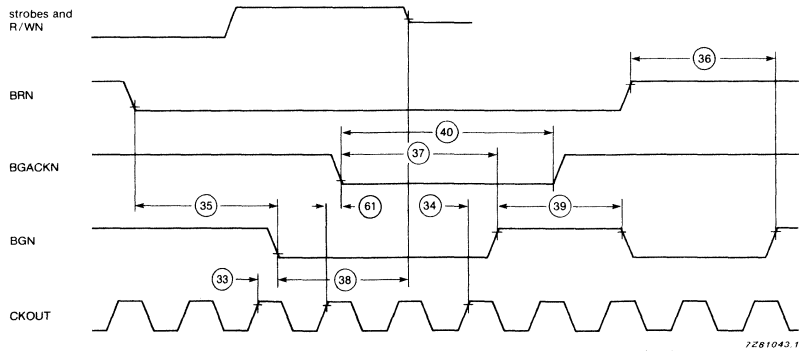


Fig.46 DMA timing.



Note

1. Setup time for the asynchronous inputs BERRN, BRN, BGACKN, DTACKN, IN2N, IN4N, IN5N, NMIN, INT1N, INT2N, AVN, REQ1N, REQ2N, DONEN, RDYN and DATA guarantees their recognition.

Fig.47 AC electrical timing—bus arbitration.

DEVELOPMENT DATA

CLOCK TIMING (see Fig. 48, 49)

parameter	symbol	min.	max.	unit
Crystal or Input Frequency	f	8	20	MHz
Cycle time	t_{cyc}	50	125	ns
Clock pulse width	t_{CL}	15	–	ns
	t_{CH}	15	–	ns
Rise and fall times	t_{Cr}	–	10	ns
	t_{Cf}	–	10	ns
XTAL1 HIGH to XTAL2 LOW	t_{C12}	–	10	ns
XTAL1 LOW to XTAL2 HIGH	t_{C21}	–	10	ns

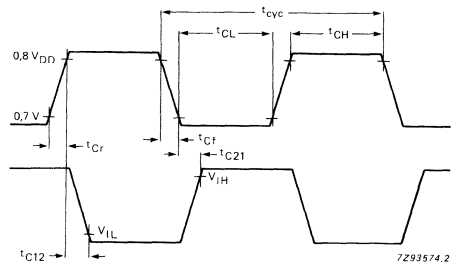


Fig.48 Input clock timing when external clock is used.

POWER CONSIDERATIONS

The average chip-junction temperature, T_j, in °C can be obtained from:

$$T_j = T_{amb} + (P_D \times R_{THJA}) \quad (1)$$

where:

T_{amb} = ambient temperature, °C
R_{THJA} = package thermal resistance, junction-to-ambient, °CW.
$P_D = P_{INT} + P_{I/O}$ (2)

$P_{INT} = I_{DD} \times V_{DD}$ = chip internal power W
$P_{I/0}$ = power dissipation on input and output pins (determined by the user)

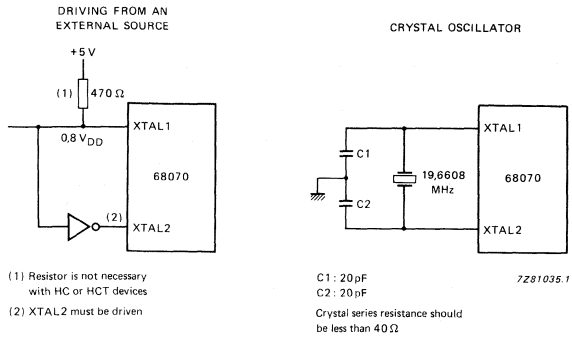
For most applications $P_{I/O} < P_{INT}$. An approximate relationship between P_D and T_j (if $P_{I/O}$ is neglected) is:

$$P_D = K \div (T_j + 273)$$

Solving equations (1) and (2) for K gives:

$$K = P_O(T_{amb} + 273) + R_{THJA} P_D^2 \quad (3)$$

Where K is a constant pertaining to a particular part. K can be determined from equation (3) by measuring P_D (at equilibrium) for a know T_{amb}. Using this value of K, the values of P_D and T_j can be obtained by solving equations (1) and (2) iteratively for any value of T_{amb}.



(1) Resistor is not necessary with HC or HCT devices

(2) XTAL2 must be driven

C1 : 20 pF
C2 : 20 pF

Crystal series resistance should be less than 40 Ω

Fig.49 clock circuitry.

I²C INTERFACE TIMING

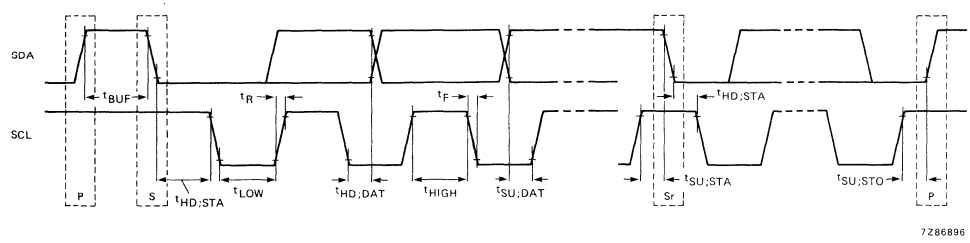


Fig. 50 I²C Interface Timing.

parameter	symbol	min.	max.	units
SCL clock frequency	f_{SCL}	0	128*	kHz
Time the bus must be free before a new transmission can start	t_{BUF}	4,7	–	µs
Hold time START condition. After this period the first clock pulse is generated	$t_{HD;STA}$	4,0	–	µs
The LOW period of the clock	t_{LOW}	4,7	–	µs
The HIGH period of the clock	t_{HIGH}	4,0	–	µs
Set-up time for START condition (only relevant for a repeated start condition)	$t_{SU;STA}$	4,7	–	µs
Hold time DATA for I²C devices	$t_{HD;DAT}$	0	–	µs
Set-up time DATA	$t_{SU;DAT}$	250	–	ns
Rise time of both SDA and SCL lines	t_R	–	1	µs
Fall time of both SDA and SCL lines	t_F	–	300	ns
Set-up time for STOP condition All values referred to V_{IH} and V_{IL} levels.	$t_{SU;STO}$	4,7	–	µs

* Note: Timings given above are for SCL = 100 kHz (max. I²C system frequency)

UART INTERFACE TIMING

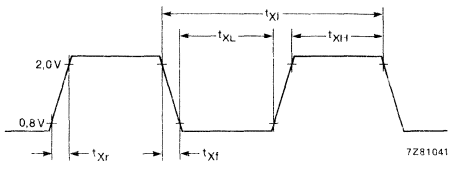


Fig.51 XCKI input timing.

DEVELOPMENT DATA

parameter	symbol	min.	typ.	max.	unit
XCKI frequency of operation	F_{XCKI}	2	4,9152*	5	MHz
XCKI cycle time	t_{XI}	200		500	ns
XCKI pulse width	t_{XH}	60		140	ns
	t_{XL}	60		140	ns
XCKI rise and fall times	t_{Xr}			t.b.f.	ns
	t_{Xf}			t.b.f.	ns

* This frequency gives accurate baud rate generation.

TIMER SPECIFICATION

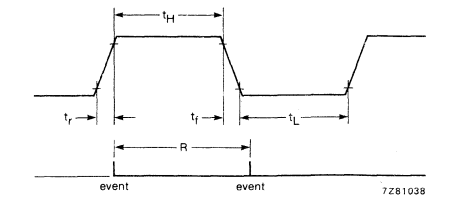


Fig.52 Input timing to T1 or T2.

parameter	symbol	min.	max.	unit
T1 or T2 pulse width	t_H	700		ns
	t_L	700		ns
T1 or T2 rise and fall times	t_r		50	ns
	t_f		50	ns
Resolution (the time between two events to be taken into account)	R	$\frac{96}{\text{CKOUT(MHz)}}$		µs

* T1 and T2 input signals must be held HIGH or LOW longer than t_H or t_L to be latched at the input to the Timer. Events must be separated by more than the resolution R of the Timer.

SUMMARY OF ON-CHIP ADDRESSES

HEX address			symbol	register
8000 0000	to	8000 OFFF	–	reserved
8000 1000			LIR	Latched interrupt priority Register
8000 1001	to	8000 2000	–	reserved
8000 2001			IDR	I^2C Data Register
8000 2002			–	reserved
8000 2003			IAR	I^2C Address Register
8000 2004			–	reserved
8000 2005			ISR	I^2C Status Register
8000 2006			–	reserved
8000 2007			ICR	I^2C Control Register
8000 2008			–	reserved
8000 2009			ICC	I^2C Clock Control Register
8000 200A	to	8000 2010	–	reserved
8000 2011			UMR	UART Mode Register
8000 2012			–	reserved
8000 2013			USR	UART Status Register
8000 2014			–	reserved
8000 2015			UCS	UART Clock Select Register
8000 2016			–	reserved
8000 2017			UCR	UART Command Register
8000 2018			–	reserved
8000 2019			UTH	UART Transmit Holding Register
8000 201A			–	reserved
8000 201B			URH	UART Receive Holding Register
8000 201C	to	8000 201F	–	reserved
8000 2020			TSR	Timer Status Register
8000 2021			TCR	Timer Control Register
8000 2022			RRH	Reload Register High
8000 2023			RRL	Reload Register Low
8000 2024			T0H	Timer 0 High
8000 2025			T0L	Timer 0 Low
8000 2026			T1H	Timer 1 High
8000 2027			T1L	Timer 1 Low
8000 2028			T2H	Timer 2 High
8000 2029			T2L	Timer 2 Low
8000 202A	to	8000 2044	–	reserved
8000 2045			PICR1	Peripheral Interrupt Control Register 1
8000 2046			–	reserved
8000 2047			PICR2	Peripheral Interrupt Control Register 2
8000 2048	to	8000 3FFF	–	reserved

HEX address			symbol	register
8000 4000			CSR	Channel Status Register Channel 1
8000 4001			CER	Channel Error Register Channel 1
8000 4002	to	8000 4003	–	reserved
8000 4004			DCR	Device Control Register Channel 1
8000 4005			OCR	Operation Control Register Channel 1
8000 4006			SCR	Sequence Control Register Channel 1
8000 4007			CCR	Channel Control Register Channel 1
8000 4008	to	8000 4009	–	reserved
8000 400A			MTCH	Memory Transfer Counter High Channel 1
8000 400B			MTCL	Memory Transfer Counter Low Channel 1
8000 400C			MACH	Memory Address Counter High Channel 1
8000 400D			MACMH	Memory Address Counter Middle High Channel
8000 400E			MACML	Memory Address Counter Middle Low Channel 1
8000 400F			MACL	Memory Address Counter Low Channel 1
8000 4010	to	8000 402C	–	reserved
8000 402D			CPR	Channel Priority Register Channel 1
8000 402E	to	8000 403F	–	reserved
8000 4040			CSR	Channel Status Register Channel 2
8000 4041			CER	Channel Error Register Channel 2
8000 4042	to	8000 4043	–	reserved
8000 4044			DCR	Device Control Register Channel 2
8000 4045			OCR	Operation Control Register Channel 2
8000 4046			SCR	Sequence Control Register Channel 2
8000 4047			CCR	Channel Control Register Channel 2
8000 4048	to	8000 4049	–	reserved
8000 404A			MTCH	Memory Transfer Counter High Channel 2
8000 404B			MTCH	Memory Transfer Counter Low Channel 2
8000 404C			MACH	Memory Address Counter HIgh Channel 2
8000 404D			MACMH	Memory Address Counter Middle High Channel 2
8000 404E			MACML	Memory Address Counter Middle Low Channel 2
8000 404F			MACL	Memory Address Counter Low Channel 2
8000 4050	to	8000 4053	–	reserved
8000 4054			DACH	Device Address Counter High Channel 2
8000 4055			DACMH	Device Address Counter Middle High Channel 2
8000 4056			DACML	Device Address Counter Middle Low Channel 2
8000 4057			DACL	Device Address Counter Low Channel 2
8000 4058	to	8000 406C	–	reserved
8000 406D			CPR	Channel Priority Register Channel 2
8000 406E	to	8000 7FFF	–	reserved

DEVELOPMENT DATA

SUMMARY OF ON-CHIP ADDRESSES (cont.)

HEX address			symbol	register
8000 8000			MSR	MMU Status Register
8000 8001			MCR	MMU Control Register
8000 8002	to	8000 803F	–	reserved
8000 8040			SAH	Segment Attributes High, Descriptor 0
8000 8041			SAL	Segment Attributes Low, Descriptor 0
8000 8042			SLH	Segment Length High, Descriptor 0
8000 8043			SLL	Segment Length Low, Descriptor 0
8000 8044			–	reserved
8000 8045			SNR	Segment Number, Descriptor 0
8000 8046			SBH	Segment Base Address High, Descriptor 0
8000 8047			SBL	Segment Base Address Low, Descriptor 0
8000 8048			SAH	Segment Attributes High, Descriptor 1
8000 8049			SAL	Segment Attributes Low, Descriptor 1
8000 804A			SLH	Segment Length High, Descriptor 1
8000 804B			SLL	Segment Length Low, Descriptor 1
8000 804C			–	reserved
8000 804D			SNR	Segment Number, Descriptor 1
8000 804E			SBH	Segment Base Address High, Descriptor 1
8000 804F			SBL	Segment Base Address Low, Descriptor 1
8000 8050			SAH	Segment Attributes High, Descriptor 2
8000 8051			SAL	Segment Attributes Low, Descriptor 2
8000 8052			SLH	Segment Length High, Descriptor 2
8000 8053			SLL	Segment Length Low, Descriptor 2
8000 8054			–	reserved
8000 8055			SNR	Segment Number, Descriptor 2
8000 8056			SBH	Segment Base Address High, Descriptor 2
8000 8057			SBL	Segment Base Address Low, Descriptor 2
8000 8058			SAH	Segment Attributes High, Descriptor 3
8000 8059			SAL	Segment Attributes Low, Descriptor 3
8000 805A			SLH	Segment Length High, Descriptor 3
8000 805B			SLL	Segment Length Low, Descriptor 3
8000 805C			–	reserved
8000 805D			SNR	Segment Number, Descriptor 3
8000 805E			SBH	Segment Base Address High, Descriptor 3
8000 805F			SBL	Segment Base Address Low, Descriptor 3
8000 8060			SAH	Segment Attributes High, Descriptor 4
8000 8061			SAL	Segment Attributes Low, Descriptor 4
8000 8062			SLH	Segment Length High, Descriptor 4
8000 8063			SLL	Segment Length Low, Descriptor 4
8000 8064			–	reserved
8000 8065			SNR	Segment Number, Descriptor 4
8000 8066			SBH	Segment Base Address High, Descriptor 4
8000 8067			SBL	Segment Base Address Low, Descriptor 4

HEX address			symbol	register
8000 8068			SAH	Segment Attributes High, Descriptor 5
8000 8069			SAL	Segment Attributes Low, Descriptor 5
8000 806A			SLH	Segment Length High, Descriptor 5
8000 806B			SLL	Segment Length Low, Descriptor 5
8000 806C			–	reserved
8000 806D			SNR	Segment Number, Descriptor 5
8000 806E			SBH	Segment Base Address High, Descriptor 5
8000 806F			SBL	Segment Base Address Low, Descriptor 5
8000 8070			SAH	Segment Attributes High, Descriptor 6
8000 8071			SAL	Segment Attributes Low, Descriptor 6
8000 8072			SLH	Segment Length HIgh, Descriptor 6
8000 8073			SLL	Segment Length Low, Descriptor 6
8000 8074			–	reserved
8000 8075			SNR	Segment Number, Descriptor 6
8000 8076			SBH	Segment Base Address High, Descriptor 6
8000 8077			SBL	Segment Base Address Low, Descriptor 6
8000 8078			SAH	Segment Attributes High, Descriptor 7
8000 8079			SAL	Segment Attributes Low, Descriptor 7
8000 807A			SLH	Segment Length High, Descriptor 7
8000 807B			SLL	Segment Length Low, Descriptor 7
8000 807C			–	reserved
8000 807D			SNR	Segment Number, Descriptor 7
8000 807E			SBH	Segment Base Address High, Descriptor 7
8000 807F			SBL	Segment Base Address Low, Descriptor 7
8000 8080	to	BFFF FFFF	–	reserved

DEVELOPMENT DATA

DTMF/MODEM/MUSICAL-TONE GENERATORS

GENERAL DESCRIPTION

The PCD3311 and PCD3312 are single-chip silicon gate CMOS integrated circuits. They are intended to provide dual-tone multi-frequency (DTMF) combinations required for tone dialling systems in telephone sets which contain a microcontroller for the control functions.

The various audio output frequencies are generated from an on-chip 3,58 MHz quartz crystal-controlled oscillator.

The devices can interface directly to all standard microcontrollers by accepting a binary-coded parallel input or serial data input (I^2C bus).

With their on-chip voltage reference the PCD3311 and PCD3312 provide constant output amplitudes which are independent of the operating supply voltage and ambient temperature.

An on-chip filtering system assures a very low total harmonic distortion in accordance with the CEPT CS 203 recommendations.

In addition to the standard DTMF frequencies the devices provide 12 MODEM frequencies (300 to 1200 bits per second) used in simplex MODEM applications and two octaves of musical scale in steps of semitones.

Features

- Stabilized output voltage level
- Low output distortion with on-chip filtering (CEPT CS 203 compatible)
- Latched inputs for data bus applications
- I^2C bus compatible
- Mode select input (selection of parallel or serial data input)
- MODEM and melody tone generators

QUICK REFERENCE DATA

parameter	symbol	min.	typ.	max.	unit
Operating supply voltage	V_{DD}	2,5	–	6,0	V
Operating supply current	I_{DD}	–	–	1,2	mA
Static standby current	I_{DDO}	–	–	3	μA
DTMF output voltage level (r.m.s. values)					
HIGH group	$V_{HG(rms)}$	158	192	205	mV
LOW group	$V_{LG(rms)}$	125	150	160	mV
Pre-emphasis of group	ΔV_G	1,85	2,10	2,35	dB
Total harmonic distortion	THD	–	–25	–	dB
Operating ambient temperature range	T_{amb}	–25	–	+70	°C

PACKAGE OUTLINES

PCD3311P: 14-lead DIL; plastic (SOT-27).
PCD3311T: 16-lead mini-pack; plastic (SO-16L; SOT-162A).
PCD3312P: 8-lead DIL; plastic (SOT-97).
PCD3312T: 8-lead mini-pack; plastic (SO-8L; SOT-176).

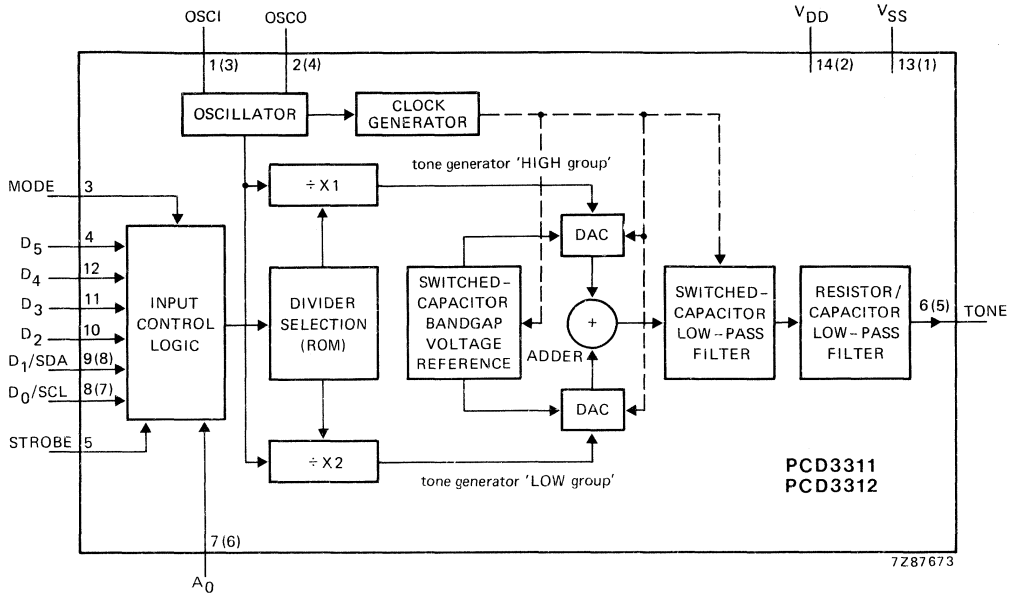


Fig. 1 Block diagram; the pin numbers in parenthesis refer to the PCD3312.

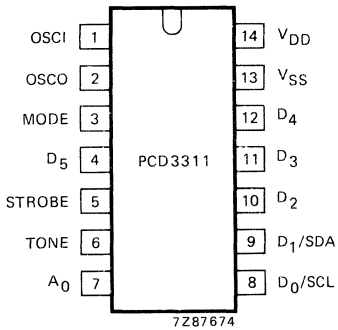


Fig. 2 Pinning diagram for the PCD3311.

PINNING

1	OSCI	oscillator input
2	OSCO	oscillator output
3	MODE	mode select input; used for the selection between serial mode (MODE = LOW) and parallel mode (MODE = HIGH)
4	D_5	parallel data input*
5	STROBE	strobe input; used for the loading of data in the parallel mode
6	TONE	frequency output for single or dual tones
7	A_0	slave address input in the serial mode; must be connected to V_{DD} or V_{SS}
8	D_0/SCL	parallel data input* or serial clock line (I^2C bus)
9	D_0/SDA	parallel data input* or serial data line (I^2C) bus)
10	D_2	parallel data inputs*
11	D_3	parallel data inputs*
12	D_4	parallel data inputs*
13	V_{SS}	negative supply
14	V_{DD}	positive supply

* MODE = HIGH.

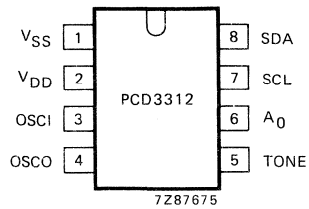


Fig. 3 Pinning diagram for the PCD3312.

PINNING

1	V_{SS}	negative supply
2	V_{DD}	positive supply
3	OSCI	oscillator input
4	OSCO	oscillator output
5	TONE	frequency output for single or dual tones
6	A_0	slave address input in the serial mode; must be connected to V_{DD} or V_{SS}
7	SCL	serial clock line (I^2C bus)
8	SDA	serial data line (I^2C bus)

FUNCTIONAL DESCRIPTION

Clock/oscillator (OSCI and OSCO)

The timebase for the PCD3311 and PCD3312 is a crystal-controlled oscillator with a 3,58 MHz quartz crystal connected between OSCI and OSCO. Alternatively, the OSCI input can be driven from an external clock.

Mode select (MODE)

This input selects the data input mode. When connected to V_{DD}, data can be received in the parallel mode (only for the PCD3311), or, when connected to V_{SS} or left open, data can be received via the serial I^2C bus (for both PCD3311 and PCD3312).

Parallel mode can only be obtained for the PCD3311 by setting MODE input HIGH.

Data inputs (D_0, D_1, D_2, D_3, D_4 and D_5)

Inputs D_0 and D_1 have no internal pull-down or pull-up resistors and must not be left open in any application. Inputs D_2 to D_5 have internal pull-down. D_5 and D_4 are used to select between DTMF dual, DTMF single, MODEM and melody tones (see Table 1). D_3 to D_0 select the combination of the tones for DTMF or single-tone itself.

Table 1 D_5 and D_4 in accordance with the selected application

D_5	D_4	application
0	0	DTMF single tones; standby; melody tones
0	1	DTMF dual tones (all 16 combinations)
1	0	MODEM tones; standby; melody tones
1	1	melody tones

1 = H = HIGH voltage level
0 = L = LOW voltage level

Note: Tables 2, 3, 4 and 5 show all input codes and their corresponding output frequencies.

DEVELOPMENT DATA

FUNCTIONAL DESCRIPTION (continued)

Strobe input (STROBE, only for the PCD3311)

This input (with internal pull-down) allows the loading of parallel data into D_0 to D_5 when MODE is HIGH.

The data inputs must be stable preceeding the positive-going edge of the strobe pulse (active HIGH). Input data are loaded at the negative-going edge of the strobe pulse and then the corresponding tone (or standby mode) is provided at the TONE output. The output remains unchanged until the negative-going edge of the next STROBE pulse (for new data) is received.

Serial mode can only be obtained for the PCD3311 by setting MODE input LOW.

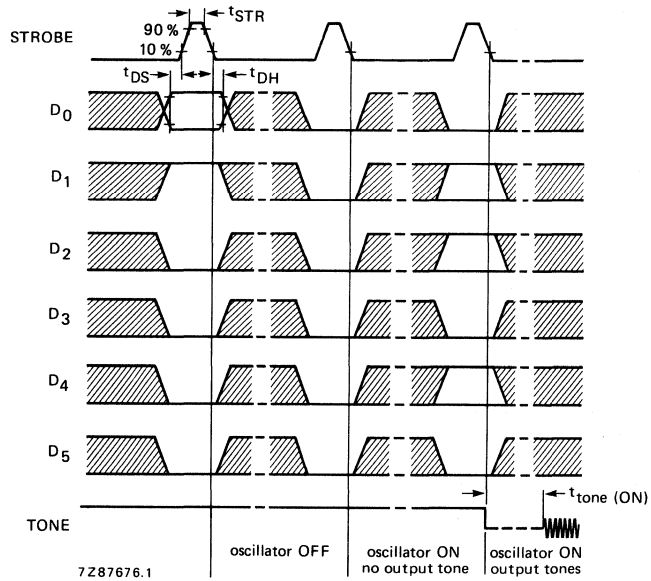


Fig. 4 Timing diagram showing control possibilities of the oscillator and the TONE output (e.g. 770 Hz + 1477 Hz) in the parallel mode (MODE = HIGH).

Serial clock and data inputs (SCL and SDA)

SCL and SDA are combined with D_0 and D_1 respectively. For the PCD3311 the selection of SCL and SDA is controlled by the MODE input. SCL and SDA are serial clock and data lines according to the I^2C bus specification (see "CHARACTERISTICS OF THE I^2C BUS"). Both inputs must be pulled-up externally to V_{DD}.

Address input (A_0)

A_0 is the slave address input and it identifies the device when up to two PCD3311 or PCD3312 devices are connected to the same I^2C bus. In any case A_0 must be connected to V_{DD} or V_{SS}.

I²C bus data configuration (see Fig. 5)

The PCD3311 and PCD3312 are always slave receivers in the I²C bus configuration (R/$\overline{W}$ bit = 0).

The slave address consists of 7 bits in the serial mode for the PCD3311 as well as for the PCD3312, where the least significant bit is selectable by hardware on input A_0 and the other more significant bits are internally fixed. In the serial mode the same input codes are used as in the parallel mode (see Tables 2, 3, 4, and 5). D_6 and D_7 are don't care (X) bits.

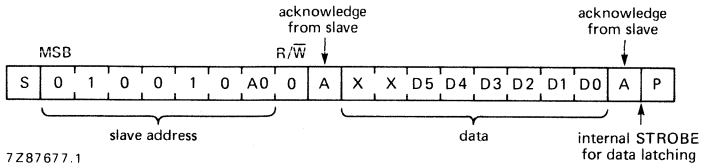


Fig. 5 I²C bus data format.

Tone output (TONE)

The single and the dual tones which are provided at the TONE output are filtered by an on-chip switched-capacitor filter, followed by an active RC low-pass filter. Therefore, the total harmonic distortion of the DTMF tones fulfils the CEPT CS 203 recommendations. An on-chip reference voltage provides output-tone levels independent of the supply voltage. Table 3 shows the frequency tolerance of the output tones for DTMF signalling; Tables 4 and 5 for the modem and melody tones.

Power-on reset

In order to avoid undefined states of the devices when the power is switched ON, an internal reset circuit sets them to the standby mode (oscillator OFF).

DEVELOPMENT DATA

Table 2 Input data for control (no output tone; TONE at V_{DD})

D_5	D_4	D_3	D_2	D_1	D_0	HEX	oscillator
X	0	0	0	0	0	00/20	ON
X	0	0	0	0	1	01/21	OFF
X	0	0	0	1	0	02/22	OFF
X	0	0	0	1	1	03/23	OFF

1 = H = HIGH voltage level
0 = L = LOW voltage level
X = don't care

FUNCTIONAL DESCRIPTION (continued)

Table 3 Input data for DTMF

D_5	D_4	D_3	D_2	D_1	D_0	HEX	symbol	standard frequency Hz	tone output freq. Hz**	frequency deviation %	frequency deviation Hz
0	0	1	0	0	0	08		697	697,90	+ 0,13	+ 0,90
0	0	1	0	0	1	09		770	770,46	+ 0,06	+ 0,46
0	0	1	0	1	0	0A		852	850,45	−0,18	−1,55
0	0	1	0	1	1	0B		941	943,23	+ 0,24	+ 2,23
0	0	1	1	0	0	0C		1209	1206,45	−0,21	−2,55
0	0	1	1	0	1	0D		1336	1341,66	+ 0,42	+ 5,66
0	0	1	1	1	0	0E		1477	1482,21	+ 0,35	+ 5,21
0	0	1	1	1	1	0F		1633	1638,24	+ 0,32	+ 5,24
0	1	0	0	0	0	10	0	941+1336			
0	1	0	0	0	1	11	1	697+1209			
0	1	0	0	1	0	12	2	697+1336			
0	1	0	0	1	1	13	3	697+1477			
0	1	0	1	0	0	14	4	770+1209			
0	1	0	1	0	1	15	5	770+1336			
0	1	0	1	1	0	16	6	770+1477			
0	1	0	1	1	1	17	7	852+1209			
0	1	1	0	0	0	18	8	852+1336			
0	1	1	0	0	1	19	9	852+1477			
0	1	1	0	1	0	1A	A	697+1633			
0	1	1	0	1	1	1B	B	770+1633			
0	1	1	1	0	0	1C	C	852+1633			
0	1	1	1	0	1	1D	D	941+1633			
0	1	1	1	1	0	1E	*	941+1209			
0	1	1	1	1	1	1F	#	941+1477			

Table 4 Input data for MODEM frequencies

D_5	D_4	D_3	D_2	D_1	D_0	HEX	standard frequency Hz	tone output freq. Hz**	frequency deviation %	frequency deviation Hz	remarks
1	0	0	1	0	0	24	1300	1296,94	−0,24	−3,06	V.23
1	0	0	1	0	1	25	2100	2103,14	+ 0,15	+ 3,14	
1	0	0	1	1	0	26	1200	1197,17	−0,24	−2,83	Bell 202
1	0	0	1	1	1	27	2200	2192,01	−0,36	−7,99	
1	0	1	0	0	0	28	980	978,82	−0,12	−1,18	V.21
1	0	1	0	0	1	29	1180	1179,03	−0,08	−0,97	
1	0	1	0	1	0	2A	1070	1073,33	+ 0,31	+ 3,33	Bell 103
1	0	1	0	1	1	2B	1270	1265,30	−0,37	−4,70	
1	0	1	1	0	0	2C	1650	1655,66	+ 0,34	+ 5,66	V.21
1	0	1	1	0	1	2D	1850	1852,77	+ 0,15	+ 2,77	
1	0	1	1	1	0	2E	2025	2021,20	−0,19	−3,80	Bell 103
1	0	1	1	1	1	2F	2225	2223,32	−0,08	−1,68	

** Tone output frequency when using a 3,579 545 MHz crystal.

1 = H = HIGH voltage level
0 = L = LOW voltage level

Table 5 Input data for melody tones

D_5	D_4	D_3	D_2	D_1	D_0	HEX	note	standard frequency Hz*	tone output frequency Hz**
1	1	0	0	0	0	30	D#5	622,3	622,5
1	1	0	0	0	1	31	E5	659,3	659,5
1	1	0	0	1	0	32	F5	698,5	697,9
1	1	0	0	1	1	33	F#5	740,0	741,1
1	1	0	1	0	0	34	G5	784,0	782,1
1	1	0	1	0	1	35	G#5	830,6	832,3
1	1	0	1	1	0	36	A5	880,0	879,3
1	1	0	1	1	1	37	A#5	932,3	931,9
1	1	1	0	0	0	38	B5	987,8	985,0
1	1	1	0	0	1	39	C6	1046,5	1044,5
1	1	1	0	1	0	3A	C#6	1108,7	1111,7
1	0	1	0	0	1	29	D6	1174,7	1179,0
1	1	1	0	1	1	3B	D#6	1244,5	1245,1
1	1	1	1	0	0	3C	E6	1318,5	1318,9
1	1	1	1	0	1	3D	F6	1396,9	1402,1
0	0	1	1	1	0	0E	F#6	1480,0	1482,2
1	1	1	1	1	0	3E	G6	1568,0	1572,0
1	0	1	1	0	0	2C	G#6	1661,2	1655,7
1	1	1	1	1	1	3F	A6	1760,0	1768,5
0	0	0	1	0	0	04	A#6	1864,7	1875,1
0	0	0	1	0	1	05	B6	1975,5	1970,0
1	0	0	1	0	1	25	C7	2093,0	2103,1
1	0	1	1	1	1	2F	C#7	2217,5	2223,3
0	0	0	1	1	0	06	D7	2349,3	2358,1
0	0	0	1	1	1	07	D#7	2489,0	2470,4

* Standard scale based on A4 = 440 Hz.

** Tone output frequency when using a 3,579 545 MHz crystal.

1 = H = HIGH voltage level

0 = L = LOW voltage level

DEVELOPMENT DATA

CHARACTERISTICS OF THE I²C BUS

The I²C bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals.

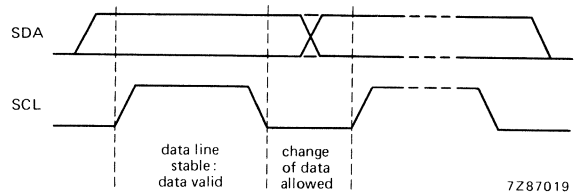


Fig. 6 Bit transfer.

Start and stop conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the stop condition (P).

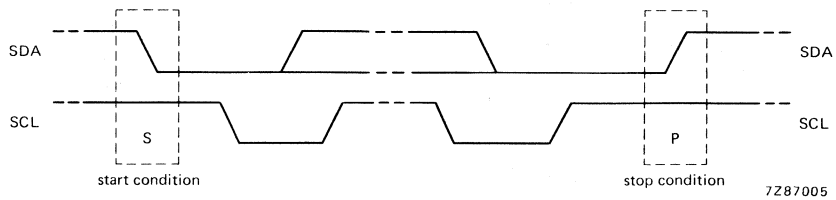


Fig. 7 Definition of start and stop conditions.

System configuration

A device generating a message is a "transmitter", a device receiving a message is the "receiver". The device that controls the message is the "master" and the devices which are controlled by the master are the "slaves".

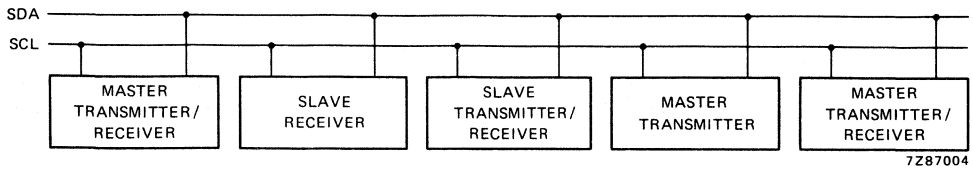


Fig. 8 System configuration.

Acknowledge

The number of data bytes transferred between the start and stop conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter whereas the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse, set-up and hold times must be taken into account. A master receiver must signal an end of data to the transmitter by *not* generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

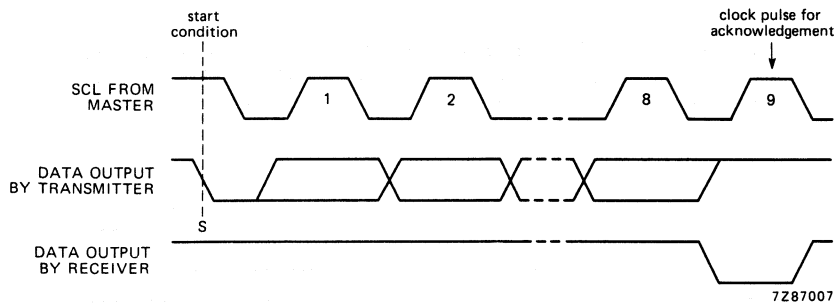


Fig. 9 Acknowledgement on the I^2C bus.

CHARACTERISTICS OF THE I²C BUS (continued)

Timing specifications

Within the I²C bus specifications a high-speed mode and a low-speed mode are defined. The ICs operate in both modes and the timing requirements are as follows:

High-speed mode

Masters generate a bus clock with a maximum frequency of 100 kHz. Detailed timing is shown in Fig. 10.

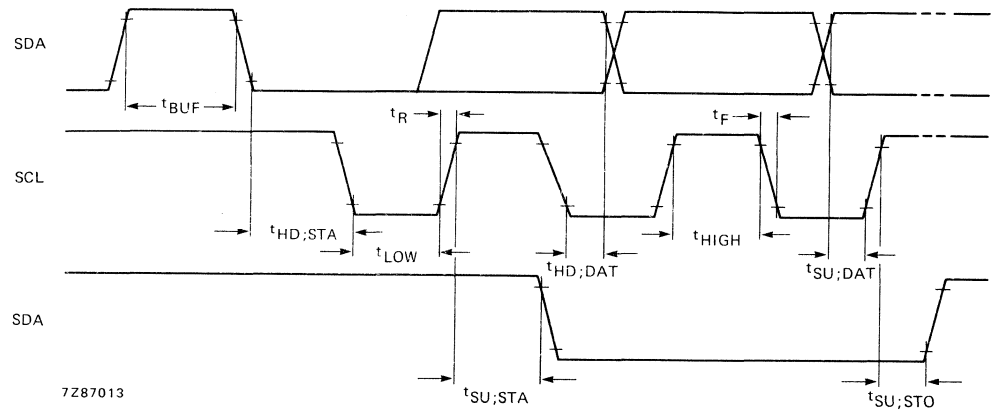


Fig. 10 Timing of the high-speed mode.

Where:

t_{BUF}	$t \geqslant t_{LOWmin}$	The minimum time the bus must be free before a new transmission can start
$t_{HD;STA}$	$t \geqslant t_{HIGHmin}$	Start condition hold time
t_{LOWmin}	4,7 μs	Clock LOW period
$t_{HIGHmin}$	4 μs	Clock HIGH period
$t_{SU;STA}$	$t \geqslant t_{LOWmin}$	Start condition set-up time, only valid for repeated start code
$t_{HD;DAT}$	$t \geqslant 0$ μs	Data hold time
$t_{SU;DAT}$	$t \geqslant 250$ ns	Data set-up time
t_R	$t \leqslant 1$ μs	Rise time of both the SDA and SCL line
t_F	$t \leqslant 300$ ns	Fall time of both the SDA and SCL line
$t_{SU;STO}$	$t \geqslant t_{LOWmin}$	Stop condition set-up time

Note

All the timing values refer to V_{IH} and V_{IL} levels with a voltage swing of V_{SS} to V_{DD}.

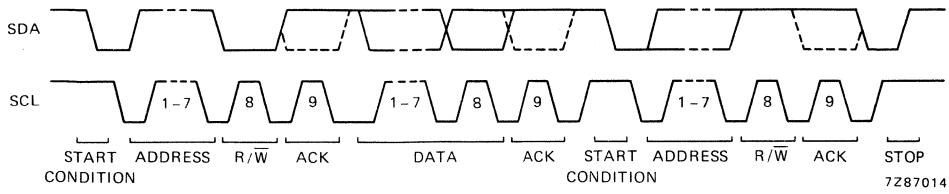


Fig. 11 Complete data transfer in the high-speed mode.

Where:

Clock t_{LOWmin}	4,7 μs
$t_{HIGHmin}$	4 μs

The dashed line is the acknowledgement of the receiver

Mark-to-space ratio	1 : 1 (LOW-to-HIGH)
Max. number of bytes	unrestricted
Premature termination of transfer	allowed by generation of STOP condition
Acknowledge clock bit	must be provided by the master

Low-speed mode

Masters generate a bus clock with a maximum frequency of 2 kHz; a minimum LOW period of 105 μs and a minimum HIGH period of 365 μs. The mark-to-space ratio is 1 : 3 LOW-to-HIGH. Detailed timing is shown in Fig. 12.

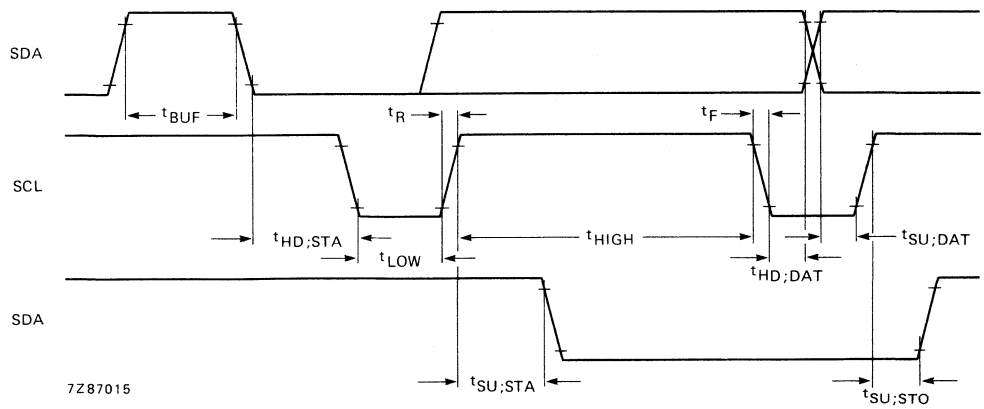


Fig. 12 Timing of the low-speed mode.

DEVELOPMENT DATA

Timing specifications (continued)

Where:

t_{BUF}	$t \geqslant 105\ \mu s$ (t_{LOWmin})
$t_{HD;STA}$	$t \geqslant 365\ \mu s$ ($t_{HIGHmin}$)
t_{LOW}	$130\ \mu s \pm 25\ \mu s$
t_{HIGH}	$390\ \mu s \pm 25\ \mu s$
$t_{SU;STA}$	$130\ \mu s \pm 25\ \mu s$ *
$t_{HD;DAT}$	$t \geqslant 0\ \mu s$
$t_{SU;DAT}$	$t \geqslant 250$ ns
t_R	$t \leqslant 1\ \mu s$
t_F	$t \leqslant 300$ ns
$t_{SU;STO}$	$130\ \mu s \pm 25\ \mu s$

Note

All the timing values refer to V_{IH} and V_{IL} levels with a voltage swing of V_{SS} to V_{DD}. For definitions see high-speed mode.

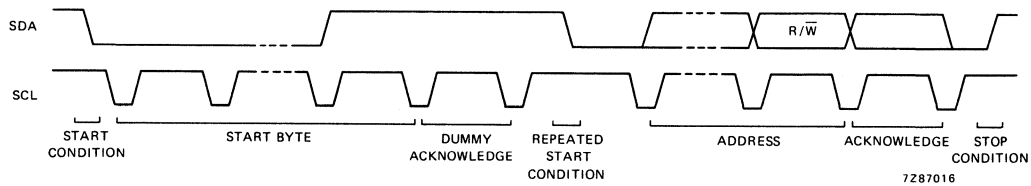


Fig. 13 Complete data transfer in the low-speed mode.

Where:

Clock t_{LOWmin}	$130\ \mu s \pm 25\ \mu s$
$t_{HIGHmin}$	$390\ \mu s \pm 25\ \mu s$
Mark-to-space ratio	1 : 3 (LOW-to-HIGH)
Start byte	0000 0001
Max. number of bytes	6
Premature termination of transfer	not allowed
Acknowledge clock bit	must be provided by master

Note

The general characteristics and detailed specification of the I^2C bus are described in a separate data sheet (serial data buses) in handbook "ICs for digital systems in radio, audio and video equipment".

* Only valid for repeated start code.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage range	V_{DD}	−0,8	+ 8,0	V
Input voltage range (any input)	V_I	−0,8	V_{DD}+0,8	V
D.C. input current (any input)	$\pm I_I$	–	10	mA
D.C. output current (any output)	$\pm I_O$	–	10	mA
Supply current	$\pm I_{DD}$; $\pm I_{SS}$	–	50	mA
Power dissipation per output	P_O	–	50	mW
Total power dissipation per package	P_{tot}	–	300	mW
Operating ambient temperature range	T_{amb}	−25	+ 70	°C
Storage temperature range	T_{stg}	−65	+ 150	°C

CHARACTERISTICS

V_{DD} = 2,5 to 6 V; V_{SS} = 0 V; crystal parameters: f_{osc} = 3,579 545 MHz, R_{Smax} = 50 Ω; T_{amb} = −25 to + 70 °C; unless otherwise specified

DEVELOPMENT DATA

parameter	symbol	min.	typ.	max.	unit
Operating supply voltage	V_{DD}	2,5	–	6,0	V
Operating supply current (note 1) oscillator ON; V_{DD} = 3 V					
no output tone	I_{DD}	–	50	100	μA
single output tone	I_{DD}	–	0,5	1,0	mA
dual output tone	I_{DD}	–	0,6	1,2	mA
Static standby current oscillator OFF; note 1	I_{DDO}	–	–	3	μA
Inputs/outputs (SDA)					
D_0 to D_5; MODE; STROBE					
Input voltage LOW	V_{IL}	0	–	0,3 x V_{DD}	V
Input voltage HIGH	V_{IH}	0,7 x V_{DD}	–	V_{DD}	V
D_2 to D_5; MODE; STROBE; A_0					
Pull-down input current V_I = V_{DD}	$-I_{IL}$	30	150	300	nA
SCL (D_0); SDA (D_1)					
Output current LOW (SDA) V_{OL} = 0,4 V	I_{OL}	3	–	–	mA
Clock frequency (see Fig. 10)	f_{SCL}	–	–	100	kHz
Input capacitance; V_I = V_{SS}	C_I	–	–	7	pF
Allowable input spike pulse width	t_I	–	–	100	ns

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
TONE output (see Fig. 14)					
DTMF output voltage levels (r.m.s. values)					
HIGH group	$V_{HG(rms)}$	158	192	205	mV
LOW group	$V_{LG(rms)}$	125	150	160	mV
D.C. voltage level	V_{DC}	–	½ V_{DD}	–	V
Pre-emphasis of group	ΔV_G	1,85	2,10	2,35	dB
Total harmonic distortion T_{amb} = 25 °C					
dual tone; note 2	THD	–	–25	–	dB
modem tone, note 3	THD	–	–29	–	dB
Output impedance	$\|Z_O\|$	–	0,1	0,5	kΩ
OSCI input					
Maximum allowable amplitude at OSCI	$V_{OSC(p-p)}$	–	–	$V_{DD}-V_{SS}$	V
Timing (V_{DD} = 3 V)					
Oscillator start-up time	$t_{OSC(ON)}$	–	3	–	ms
TONE start-up time; note 4	$t_{TONE(ON)}$	–	0,5	–	ms
STROBE pulse width; note 5	t_{STR}	400	–	–	ns
Data set-up time; note 5	t_{DS}	150	–	–	ns
Data hold time; note 5	t_{DH}	100	–	–	ns

Notes to the characteristics

1. Crystal is connected between OSCI and OSCO; D_0/SCL and D_1/SDA via a resistance of 5,6 kΩ to V_{DD}; all other pins left open.
2. Related to the level of the LOW group frequency component (CEPT CS 203).
3. Related to the level of the fundamental frequency.
4. Oscillator must be running.
5. Values are referenced to the 10% and 90% levels of the relevant pulse amplitudes, with a total voltage swing from V_{SS} to V_{DD}.

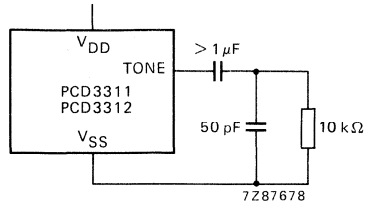


Fig. 14 TONE output test circuit.

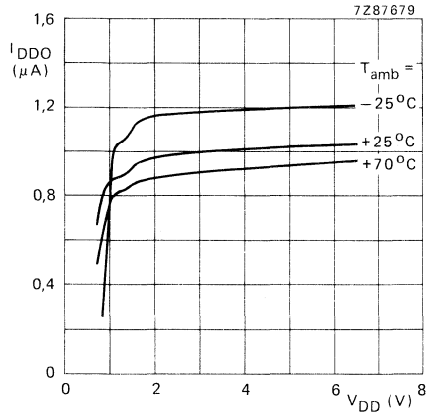


Fig. 15 Standby supply current as a function of supply voltage; oscillator OFF.

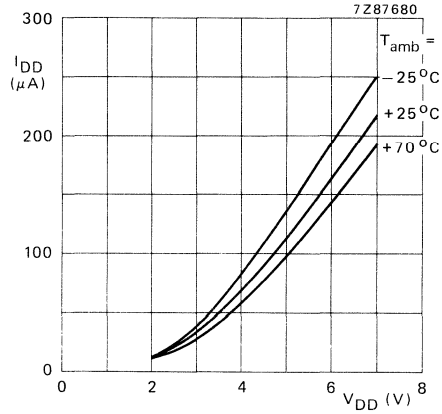


Fig. 16 Operating supply current as a function of supply voltage; oscillator ON; no output at TONE.

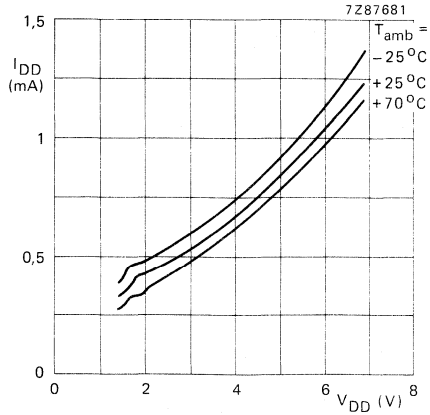


Fig. 17 Operating supply current as a function of supply voltage; oscillator ON; dual tone at TONE.

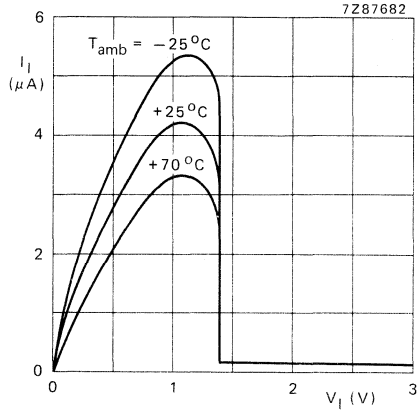


Fig. 18 Pull-down input current as a function of input voltage; V_{DD} = 3 V.

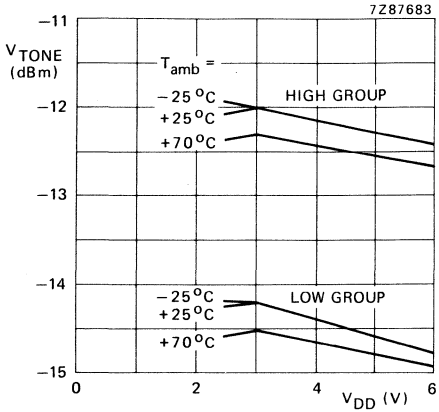


Fig. 19 DTMF output voltage levels as a function of operating supply voltage; R_L = 1 MΩ.

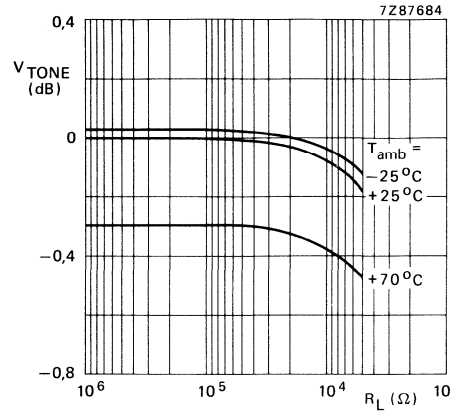


Fig. 20 Dual tone output voltage level as a function of output load resistance.

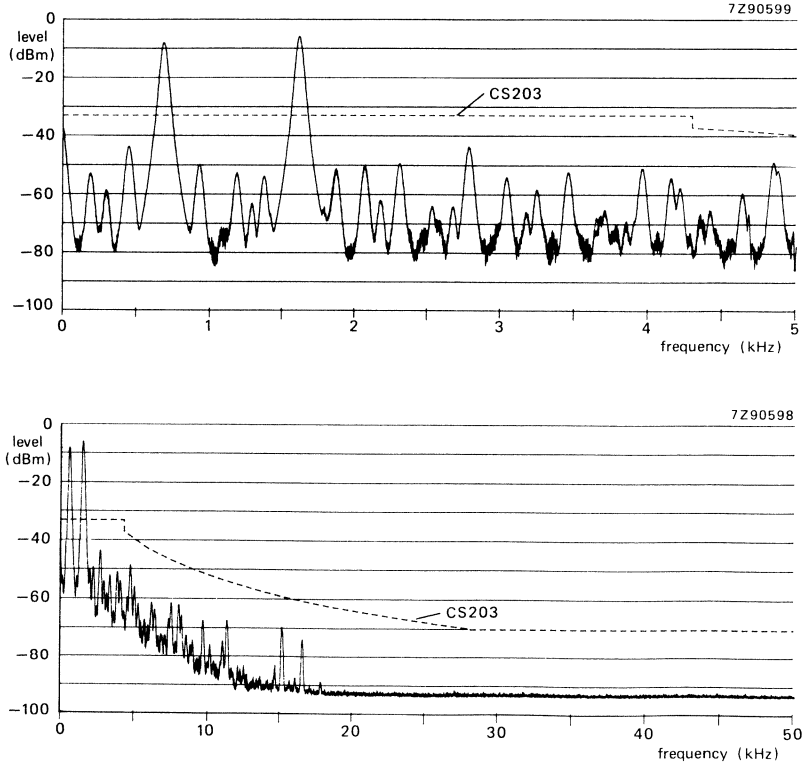


Fig. 21 Typical frequency spectrum of a dual tone signal after flat-band amplification of 6 dB.

APPLICATION INFORMATION

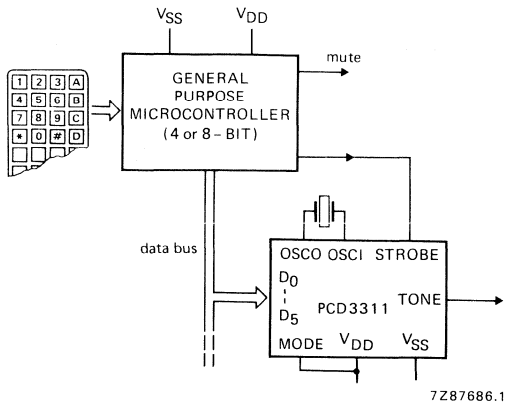


Fig. 22 PCD3311 driven by a microcontroller with parallel data-bus.

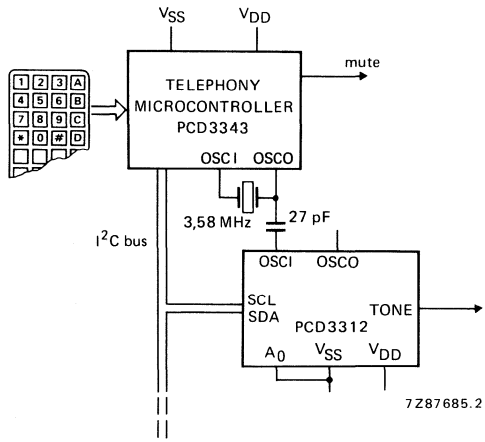


Fig. 23 PCD3312 driven by telephony microcontroller PCD3343 with serial I/O (I^2C bus).
The PCD3343 is a single-chip 8-bit microcontroller with 3K ROM/224 RAM bytes. The same application is possible with the PCD3311 with MODE = V_{SS}.

DTMF / SINGLE -TONE GENERATOR

GENERAL DESCRIPTION

The PCD3311A is a single-chip silicon gate CMOS integrated circuit. It is intended to provide dual-tone multi-frequency (DTMF) combinations required for tone dialling systems in telephone sets which contain a microcontroller for the control functions.

The various audio output frequencies are generated from an on-chip 3,58 MHz quartz crystal-controlled oscillator.

The device can interface directly to all standard microcontrollers by accepting a binary-coded parallel input or serial data input (I^2C bus).

With its on-chip voltage reference the PCD3311A provides constant output amplitudes which are independent of the operating supply voltage and ambient temperature.

An on-chip filtering system assures a very low total harmonic distortion in accordance with the CEPT CS 203 recommendations.

In addition to the standard DTMF frequencies the device provides 32 single frequencies.

Features

- Stabilized output voltage level
- Low output distortion with on-chip filtering (CEPT CS 203 compatible)
- Latched inputs for data bus applications
- I^2C bus compatible
- Mode select input (selection of parallel or serial data input)

QUICK REFERENCE DATA

parameter	symbol	min.	typ.	max.	unit
Operating supply voltage	V_{DD}	2,5	–	6,0	V
Operating supply current	I_{DD}	–	–	0,9	mA
Static standby current	I_{DDO}	–	–	3	μA
DTMF output voltage level (r.m.s. values)					
HIGH group	$V_{HG(rms)}$	158	192	205	mV
LOW group	$V_{LG(rms)}$	125	150	160	mV
Pre-emphasis of group	ΔV_G	1,85	2,10	2,35	dB
Total harmonic distortion	THD	–	–25	–	dB
Operating ambient temperature range	T_{amb}	–25	–	+70	°C

PACKAGE OUTLINE

PCD3311AT: 16-lead mini-pack; plastic (SO-16L; SOT-162A).

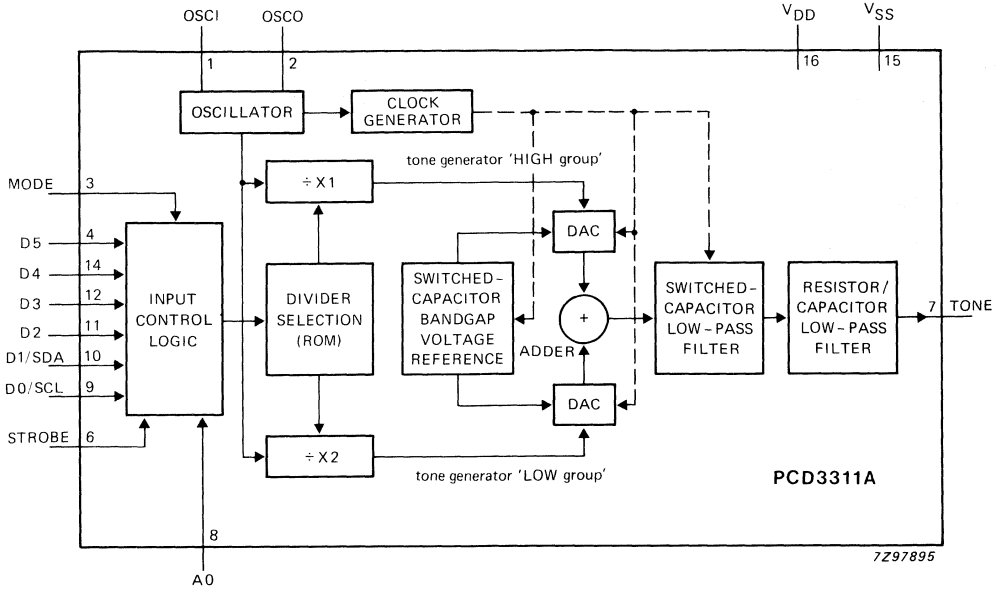


Fig. 1 Block diagram.

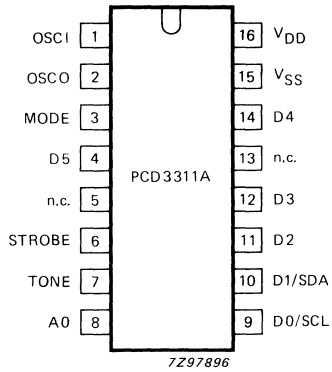


Fig. 2 Pinning diagram.

PINNING

1	OSCI	oscillator input
2	OSCO	oscillator output
3	MODE	mode select input; used for the selection between serial mode (MODE = LOW) and parallel mode (MODE = HIGH)
4	D5	parallel data input*
6	STROBE	strobe input; used for the loading of data in the parallel mode
7	TONE	frequency output for single or dual tones
8	A0	slave address input in the serial mode; must be connected to V_{DD} or V_{SS}
9	D0/SCL	parallel data input* or serial clock line (I^2C bus)
10	D1/SDA	parallel data input* or serial data line (I^2C bus)
11	D2	parallel data inputs*
12	D3	
14	D4	
15	V_{SS}	negative supply
16	V_{DD}	positive supply
5;13	n.c.	not connected

* MODE = HIGH.

FUNCTIONAL DESCRIPTION

Clock/oscillator (OSCI and OSCO)

The timebase for the PCD3311A is a crystal-controlled oscillator with a 3,58 MHz quartz crystal connected between OSCI and OSCO. Alternatively, the OSCI input can be driven from an external clock.

Mode select (MODE)

This input selects the data input mode. When connected to V_{DD}, data can be received in the parallel mode or, when connected to V_{SS} or left open, data can be received via the serial I^2C bus.

Parallel mode can only be obtained by setting MODE input HIGH.

Data inputs (D0, D1, D2, D3, D4 and D5)

Inputs D0 and D1 have no internal pulll-down or pull-up resistors and must not be left open in any application. Inputs D2 to D5 have internal pull-down.

Tables 1, 2 and 3 show all input codes and their corresponding output frequencies.

Strobe input (STROBE)

This input (with internal pull-down) allows the loading of parallel data into D0 to D5 when MODE is HIGH.

The data inputs must be stable preceeding the positive-going edge of the strobe pulse (active HIGH). Input data are loaded at the negative-going edge of the strobe pulse and then the corresponding tone (or standby mode) is provided at the TONE output. The output remains unchanged until the negative-going edge of the next STROBE pulse (for new data) is received.

Serial mode can only be obtained by setting MODE input LOW.

DEVELOPMENT DATA

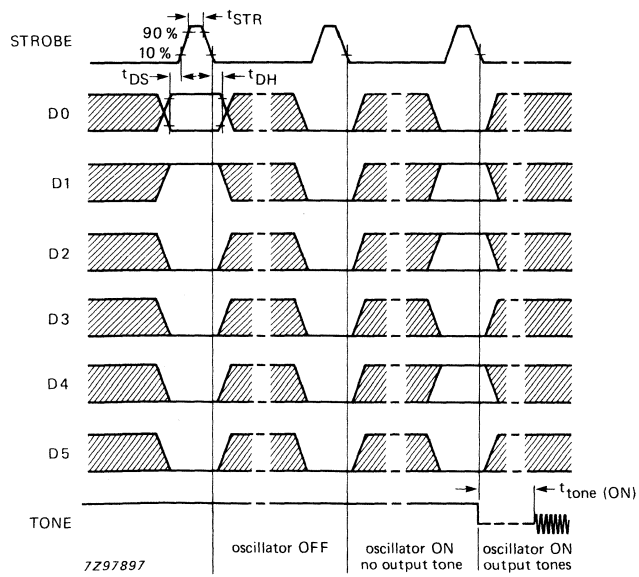


Fig. 3 Timing diagram showing control possibilities of the oscillator and the TONE output (e.g. 770 Hz + 1477 Hz) in the parallel mode (MODE = HIGH).

FUNCTIONAL DESCRIPTION (continued)

Serial clock and data inputs (SCL and SDA)

SCL and SDA are combined with D0 and D1 respectively. For the PCD3311A the selection of SCL and SDA is controlled by the MODE input. SCL and SDA are serial clock and data lines according to the I^2C bus specification (see "CHARACTERISTICS OF THE I^2C BUS"). Both inputs must be pulled-up externally to V_{DD}.

Address input (A0)

A0 is the slave address input and it identifies the device when up to two PCD3311 devices are connected to the same I^2C bus. However, A0 must be connected to V_{DD} or V_{SS}.

I^2C bus data configuration (see Fig. 4)

The PCD3311 is always a slave receiver in the I^2C bus configuration ($R/\overline{W}$ bit = 0).

The slave address consists of 7 bits in the serial mode where the least significant bit is selectable by hardware on input A0, and the other more significant bits are internally fixed. In the serial mode the same input codes are used as in the parallel mode (see Tables 1, 2 and 3). D6 and D7 are don't care (X) bits.

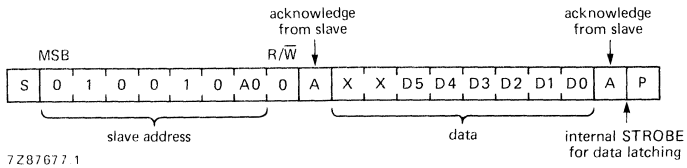


Fig. 4 I^2C bus data format.

Tone output (TONE)

The single and the dual tones which are provided at the TONE output are filtered by an on-chip switched-capacitor filter, followed by an active RC low-pass filter. Therefore, the total harmonic distortion of the DTMF tones fulfils the CEPT CS 203 recommendations. An on-chip reference voltage provides output-tone levels independent of the supply voltage. Table 2 shows the frequency tolerance of the output tones for DTMF signalling; Table 3 for the single tones.

Power-on reset

In order to avoid undefined states of the devices when the power is switched ON, an internal reset circuit sets them to the standby mode (oscillator OFF).

Table 1 Input data for control (no output tone; TONE at V_{DD})

D5	D4	D3	D2	D1	D0	HEX	oscillator
X	0	0	0	0	0	00/20	ON
X	0	0	0	0	1	01/21	OFF
X	0	0	0	1	0	02/22	OFF
X	0	0	0	1	1	03/23	OFF

Where:

1 = H = HIGH voltage level
0 = L = LOW voltage level
X = don't care.

Table 2 Input data for DTMF

D5	D4	D3	D2	D1	D0	HEX	symbol	standard frequency Hz	tone output freq. Hz*	frequency deviation %	frequency deviation Hz
0	0	1	0	0	0	08		697	697,90	+ 0,13	+ 0,90
0	0	1	0	0	1	09		770	770,46	+ 0,06	+ 0,46
0	0	1	0	1	0	0A		852	850,45	−0,18	−1,55
0	0	1	0	1	1	0B		941	943,23	+ 0,24	+ 2,23
0	0	1	1	0	0	0C		1209	1206,45	−0,21	−2,55
0	0	1	1	0	1	0D		1336	1341,66	+ 0,42	+ 5,66
0	0	1	1	1	0	0E		1477	1482,21	+ 0,35	+ 5,21
0	0	1	1	1	1	0F		1633	1638,24	+ 0,32	+ 5,24
0	1	0	0	0	0	10	0	941+1336			
0	1	0	0	0	1	11	1	697+1209			
0	1	0	0	1	0	12	2	697+1336			
0	1	0	0	1	1	13	3	697+1477			
0	1	0	1	0	0	14	4	770+1209			
0	1	0	1	0	1	15	5	770+1336			
0	1	0	1	1	0	16	6	770+1477			
0	1	0	1	1	1	17	7	852+1209			
0	1	1	0	0	0	18	8	852+1336			
0	1	1	0	0	1	19	9	852+1477			
0	1	1	0	1	0	1A	A	697+1633			
0	1	1	0	1	1	1B	B	770+1633			
0	1	1	1	0	0	1C	C	852+1633			
0	1	1	1	0	1	1D	D	941+1633			
0	1	1	1	1	0	1E	*	941+1209			
0	1	1	1	1	1	1F	#	941+1477			

Where:

1 = H = HIGH voltage level
0 = L = LOW voltage level

DEVELOPMENT DATA

* Tone output frequency when using a 3,579 545 MHz crystal.

FUNCTIONAL DESCRIPTION (continued)

Table 3 Input data for single frequencies

D5	D4	D3	D2	D1	D0	HEX	standard frequency (Hz)	tone output (Hz)*	frequency deviation	
									%	Hz
0	0	0	1	0	0	04	680	679,62	−0,06	−0,38
0	0	0	1	0	1	05	740	741,11	+0,15	+1,11
0	0	0	1	1	0	06	810	810,59	+0,07	+0,59
0	0	0	1	1	1	07	873	874,34	+0,15	+1,34
1	0	0	1	0	0	24	886	884,28	−0,20	−1,73
1	0	0	1	0	1	25	930	931,93	+0,21	+1,93
1	0	0	1	1	0	26	970	972,70	+0,28	+2,70
1	0	0	1	1	1	27	991	991,29	+0,03	+0,29
1	0	1	0	0	0	28	1055	1051,57	−0,33	−3,43
1	0	1	0	0	0	28	1060	1051,57	−0,80	−8,43
1	0	1	0	0	1	29	1124	1127,77	+0,34	+3,77
1	0	1	0	1	0	2A	1160	1161,44	+0,12	+1,44
1	0	1	0	1	1	2B	1197	1197,17	+0,01	+0,17
1	0	1	1	0	0	2C	1270	1275,68	+0,45	+5,68
1	0	1	1	0	0	2C	1275	1275,68	+0,05	+0,68
1	0	1	1	0	1	2D	1358	1353,33	−0,34	−4,68
1	0	1	1	1	0	2E	1400	1402,09	+0,15	+2,09
1	0	1	1	1	1	2F	1446	1441,04	−0,34	−4,96
1	1	0	0	0	0	30	1520	1525,81	+0,38	+5,81
1	1	0	0	0	0	30	1530	1525,81	−0,27	−4,19
1	1	0	0	0	1	31	1540	1540,92	+0,06	+0,92
1	1	0	0	1	0	32	1640	1638,24	−0,11	−1,76
1	1	0	0	1	1	33	1670	1673,47	+0,21	+3,47
1	1	0	1	0	0	34	1747	1748,68	+0,10	+1,68
1	1	0	1	0	1	35	1830	1830,97	+0,05	+0,97
1	1	0	1	1	0	36	1860	1852,77	−0,39	−7,23
1	1	0	1	1	1	37	1960	1970,03	+0,51	+10,03
1	1	0	1	1	1	37	1981	1970,03	−0,55	−10,97
1	1	1	0	0	0	38	2000	2021,20	+1,06	+21,20
1	1	1	0	0	1	39	2110	2103,14	−0,33	−6,86
1	1	1	0	1	0	3A	2200	2192,01	−0,36	−7,99
1	1	1	0	1	1	3B	2247	2255,54	+0,38	+8,54
1	1	1	1	0	0	3C	2280	2288,71	+0,38	+8,71
1	1	1	1	0	1	3D	2400	2394,34	−0,24	−5,66
1	1	1	1	1	0	3E	2600	2593,87	−0,24	−6,13
1	1	1	1	1	1	3F	2800	2779,15	−0,75	−20,85

Where:

1 = H = HIGH voltage level
0 = L = LOW voltage level

* Tone output frequency when using a 3,579545 MHz crystal.

CHARACTERISTICS OF THE I²C BUS

The I²C bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals.

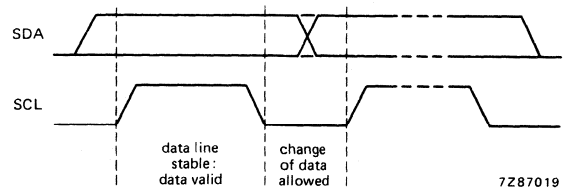


Fig. 5 Bit transfer.

Start and stop conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the stop condition (P).

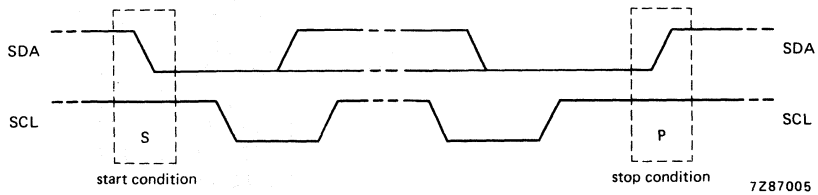


Fig. 6 Definition of start and stop conditions.

System configuration

A device generating a message is a "transmitter", a device receiving a message is the "receiver". The device that controls the message is the "master" and the devices which are controlled by the master are the "slaves".

CHARACTERISTICS OF THE I²C BUS (continued)

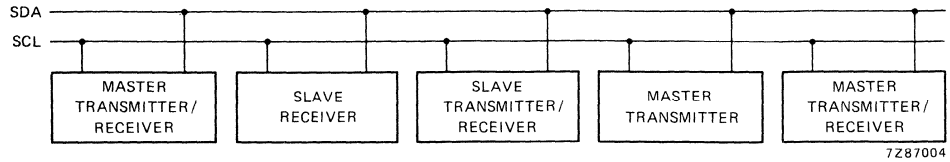


Fig. 7 System configuration.

Acknowledge

The number of data bytes transferred between the start and stop conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter whereas the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse, set-up and hold times must be taken into account. A master receiver must signal an end of data to the transmitter by *not* generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

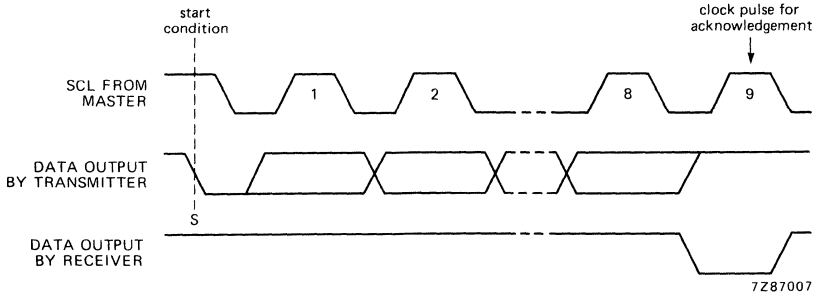


Fig. 8 Acknowledgement on the I²C bus.

DEVELOPMENT DATA

Timing specifications

Within the I^2C bus specifications a high-speed mode and a low-speed mode are defined. The ICs operate in both modes and the timing requirements are as follows:

High-speed mode

Masters generate a bus clock with a maximum frequency of 100 kHz. Detailed timing is shown in Fig. 9.

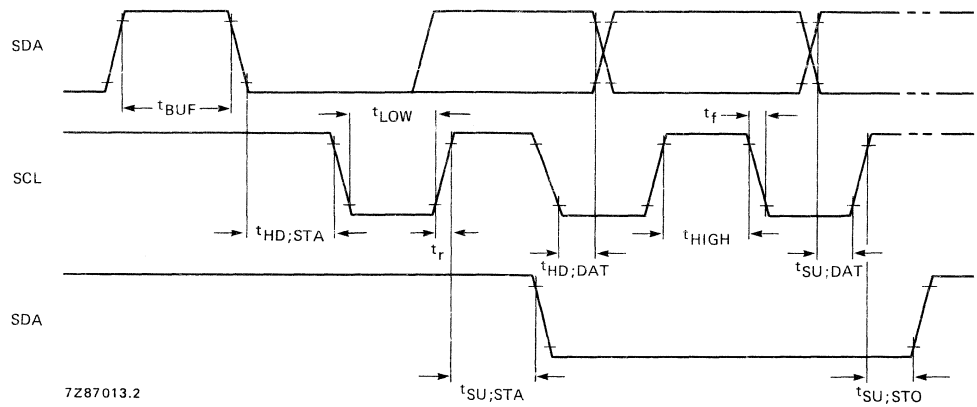


Fig. 9 Timing of the high-speed mode.

Where:

t_{BUF}	$t \geqslant t_{LOWmin}$	The minimum time the bus must be free before a new transmission can start
$t_{HD;STA}$	$t \geqslant t_{HIGHmin}$	Start condition hold time
t_{LOWmin}	4,7 μs	Clock LOW period
$t_{HIGHmin}$	4 μs	Clock HIGH period
$t_{SU;STA}$	$t \geqslant t_{LOWmin}$	Start condition set-up time, only valid for repeated start code
$t_{HD;DAT}$	$t \geqslant 0$ μs	Data hold time
$t_{SU;DAT}$	$t \geqslant 250$ ns	Data set-up time
t_r	$t \leqslant 1$ μs	Rise time of both the SDA and SCL line
t_f	$t \leqslant 300$ ns	Fall time of both the SDA and SCL line
$t_{SU;STO}$	$t \geqslant t_{LOWmin}$	Stop condition set-up time

Note

All the timing values refer to V_{IH} and V_{IL} levels with a voltage swing of V_{SS} to V_{DD}.

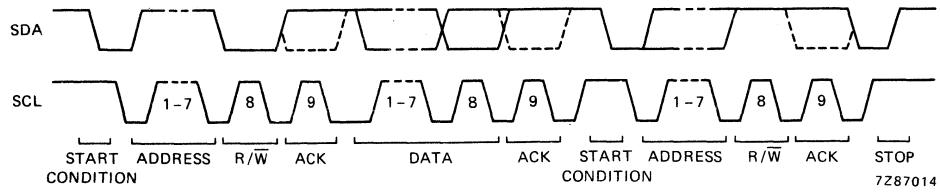


Fig. 10 Complete data transfer in the high-speed mode.

Where:

Clock t_{LOWmin}	4,7 μs
$t_{HIGHmin}$	4 μs

The dashed line is the acknowledgement of the receiver

Mark-to-space ratio	1 : 1 (LOW-to-HIGH)
Max. number of bytes	unrestricted
Premature termination of transfer	allowed by generation of STOP condition
Acknowledge clock bit	must be provided by the master

Low-speed mode

Masters generate a bus clock with a maximum frequency of 2 kHz; a minimum LOW period of 105 μs and a minimum HIGH period of 365 μs. The mark-to-space ratio is 1 : 3 LOW-to-HIGH. Detailed timing is shown in Fig. 11.

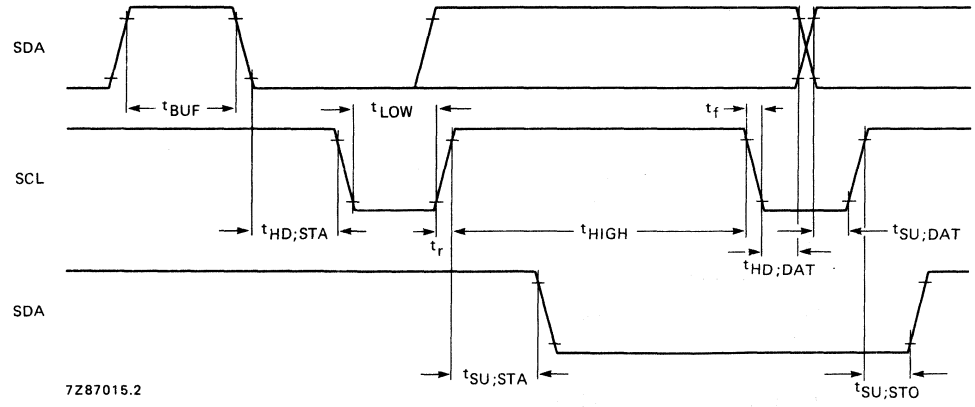


Fig. 11 Timing of the low-speed mode.

Timing specifications (continued)

Where:

t_{BUF}	$t \geqslant 105\ \mu s$ (t_{LOWmin})
$t_{HD;STA}$	$t \geqslant 365\ \mu s$ ($t_{HIGHmin}$)
t_{LOW}	$130\ \mu s \pm 25\ \mu s$
t_{HIGH}	$390\ \mu s \pm 25\ \mu s$
$t_{SU;STA}$	$130\ \mu s \pm 25\ \mu s$ *
$t_{HD;DAT}$	$t \geqslant 0\ \mu s$
$t_{SU;DAT}$	$t \geqslant 250$ ns
t_r	$t \leqslant 1\ \mu s$
t_f	$t \leqslant 300$ ns
$t_{SU;STO}$	$130\ \mu s \pm 25\ \mu s$

Note

All the timing values refer to V_{IH} and V_{IL} levels with a voltage swing of V_{SS} to V_{DD}. For definitions see high-speed mode.

DEVELOPMENT DATA

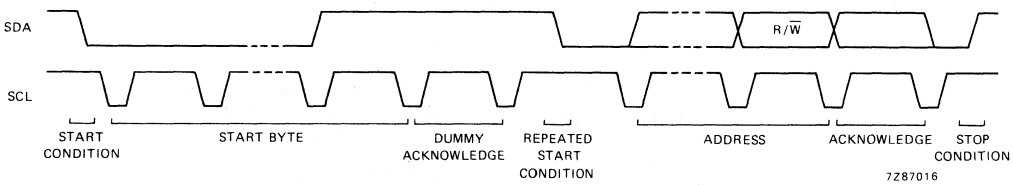


Fig. 12 Complete data transfer in the low-speed mode.

Where:

Clock t_{LOWmin}	$130\ \mu s \pm 25\ \mu s$
$t_{HIGHmin}$	$390\ \mu s \pm 25\ \mu s$
Mark-to-space ratio	1 : 3 (LOW-to-HIGH)
Start byte	0000 0001
Max. number of bytes	6
Premature termination of transfer	not allowed
Acknowledge clock bit	must be provided by master

Note

The general characteristics and detailed specification of the I^2C bus are described in a separate data sheet (serial data buses) in handbook "ICs for digital systems in radio, audio and video equipment".

* Only valid for repeated start code.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage range	V_{DD}	−0,8	+ 8,0	V
Input voltage range (any input)	V_I	−0,8	V_{DD}+0,8	V
DC input current (any input)	$\pm I_I$	–	10	mA
DC output current (any output)	$\pm I_O$	–	10	mA
Supply current	$\pm I_{DD}$; $\pm I_{SS}$	–	50	mA
Power dissipation per output	P_O	–	50	mW
Total power dissipation per package	P_{tot}	–	300	mW
Operating ambient temperature range	T_{amb}	−25	+ 70	°C
Storage temperature range	T_{stg}	−65	+ 150	°C

CHARACTERISTICS

V_{DD} = 2,5 to 6 V; V_{SS} = 0 V; crystal parameters: f_{osc} = 3,579 545 MHz, R_{Smax} = 100 Ω; T_{amb} = −25 to + 70 °C; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Operating supply voltage	V_{DD}	2,5	–	6,0	V
Operating supply current (note 1) oscillator ON; V_{DD} = 3 V					
no output tone	I_{DD}	–	50	100	μA
single output tone	I_{DD}	–	0,5	0,9	mA
dual output tone	I_{DD}	–	0,6	0,9	mA
Static standby current oscillator OFF; note 1	I_{DDO}	–	–	3	μA
Inputs/outputs (SDA)					
D0 to D5; MODE; STROBE					
Input voltage LOW	V_{IL}	0	–	0,3 x V_{DD}	V
Input voltage HIGH	V_{IH}	0,7 x V_{DD}	–	V_{DD}	V
D2 to D5; MODE; STROBE; A0					
Pull-down input current V_I = V_{DD}	$-I_{IL}$	30	150	300	nA
SCL (D0); SDA (D1)					
Output current LOW (SDA) V_{OL} = 0,4 V	I_{OL}	3	–	–	mA
Clock frequency (see Fig. 10)	f_{SCL}	–	–	100	kHz
Input capacitance; V_I = V_{SS}	C_I	–	–	7	pF
Allowable input spike pulse width	t_I	–	–	100	ns

parameter	symbol	min.	typ.	max.	unit
TONE output (see Fig. 13)					
DTMF output voltage levels (r.m.s. values)					
HIGH group	$V_{HG(rms)}$	158	192	205	mV
LOW group	$V_{LG(rms)}$	125	150	160	mV
DC voltage level	V_{DC}	–	½ V_{DD}	–	V
Pre-emphasis of group	ΔV_G	1,85	2,10	2,35	dB
Total harmonic distortion T_{amb} = 25 °C					
dual tone; note 2	THD	–	–25	–	dB
modem tone, note 3	THD	–	–29	–	dB
Output impedance	$\|Z_O\|$	–	0,1	0,5	kΩ
OSCI input					
Maximum allowable amplitude at OSCI	$V_{OSC(p-p)}$	–	–	$V_{DD}-V_{SS}$	V
Timing (V_{DD} = 3 V)					
Oscillator start-up time	$t_{OSC(ON)}$	–	3	–	ms
TONE start-up time; note 4	$t_{TONE(ON)}$	–	0,5	–	ms
STROBE pulse width; note 5	t_{STR}	400	–	–	ns
Data set-up time; note 5	t_{DS}	150	–	–	ns
Data hold time; note 5	t_{DH}	100	–	–	ns

DEVELOPMENT DATA

Notes to the characteristics

1. Crystal is connected between OSCI and OSCO; D0/SCL and D1/SDA via a resistance of 5,6 kΩ to V_{DD}; all other pins left open.
2. Related to the level of the LOW group frequency component (CEPT CS 203).
3. Related to the level of the fundamental frequency.
4. Oscillator must be running.
5. Values are referenced to the 10% and 90% levels of the relevant pulse amplitudes, with a total voltage swing from V_{SS} to V_{DD}.

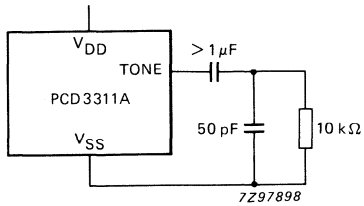


Fig. 13 TONE output test circuit.

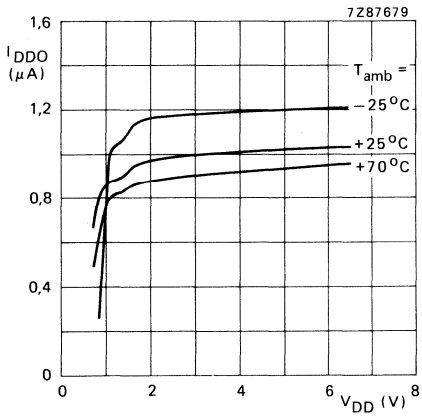


Fig. 14 Standby supply current as a function of supply voltage; oscillator OFF.

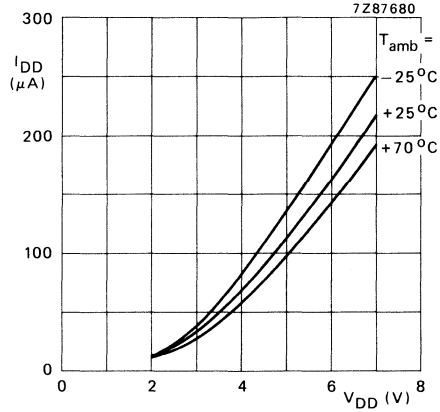


Fig. 15 Operating supply current as a function of supply voltage; oscillator ON; no output at TONE.

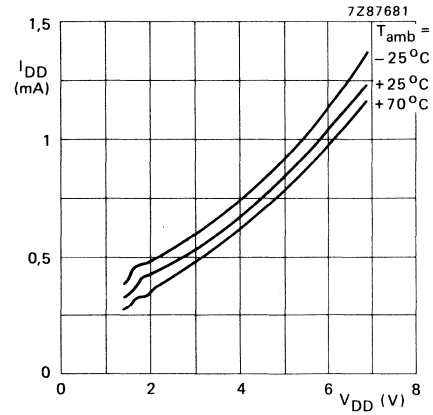


Fig. 16 Operating supply current as a function of supply voltage; oscillator ON; dual tone at TONE.

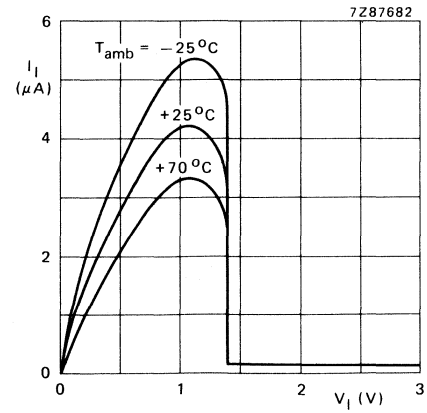


Fig. 17 Pull-down input current as a function of input voltage; V_{DD} = 3 V.

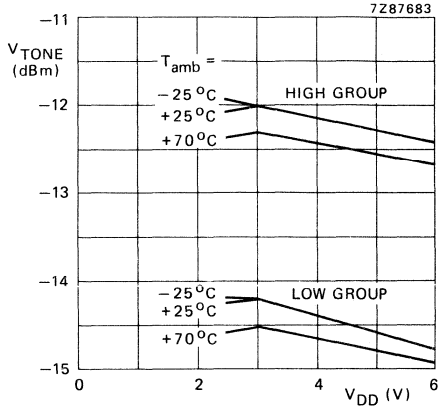


Fig. 18 DTMF output voltage levels as a function of operating supply voltage; R_L = 1 MΩ.

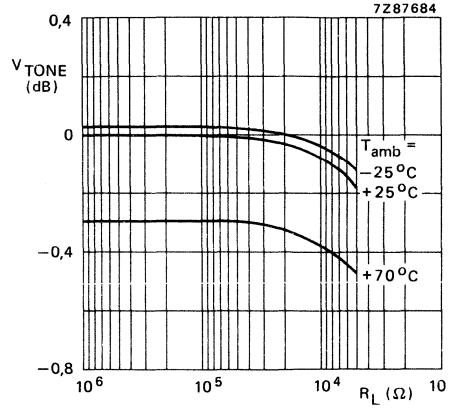


Fig. 19 Dual tone output voltage level as a function of output load resistance.

DEVELOPMENT DATA

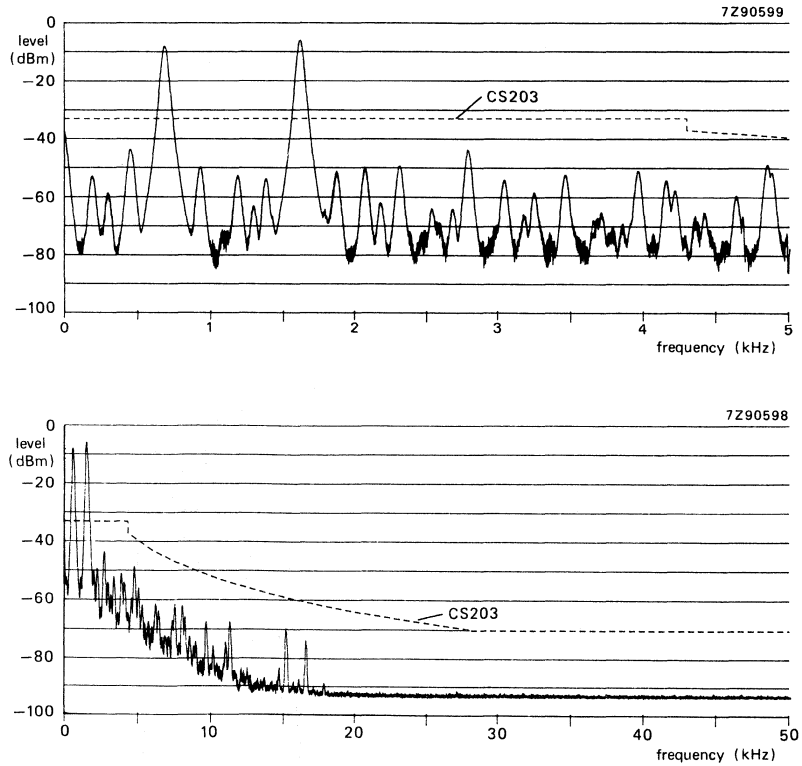


Fig. 20 Typical frequency spectrum of a dual tone signal after flat-band amplification of 6 dB.

APPLICATION INFORMATION

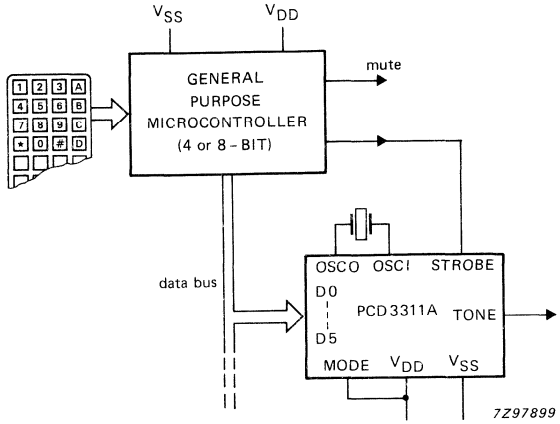


Fig. 21 PCD3311A driven by a microcontroller with parallel data-bus.

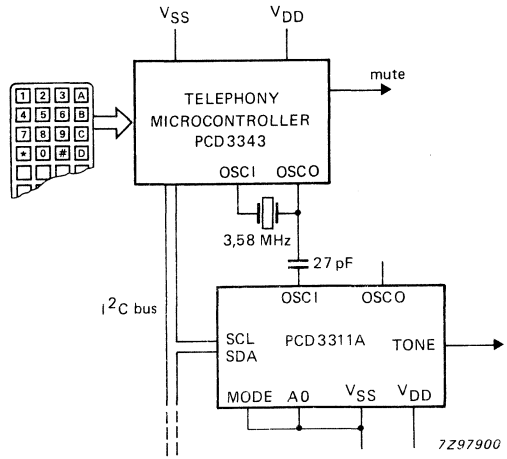


Fig. 22 PCD3311A driven by telephony microcontroller PCD3343 with serial I/O (I^2C bus).
The PCD3343 is a single-chip 8-bit microcontroller with 3K ROM/224 RAM bytes.

VOICE SYNTHESIZER

GENERAL DESCRIPTION

The PCF8200 is a CMOS integrated circuit for generating good quality speech from digital code with a programmable bit rate. The circuit is primarily intended for applications in microprocessor controlled systems, where the speech code is stored separately.
Applications include automotive, telephony, personal computers, annunciators, aids for the handicapped, and general industrial devices.

Features

- Male and female speech with good quality
- Speech-band from 0 to 5 kHz
- Bit-rate between 455 bits/second and 4545 bits/second
- Programmable frame duration
- Programmable speaking speed
- CMOS technology
- Operating temperature range −40 to + 85 °C
- Single 5 V supply with low power consumption and power-down stand-by mode
- Interfaces easily with most popular microcomputers and microprocessors through 8 bit parallel bus or I^2C bus
- Software readable status word (parallel bus or I^2C bus)
- BUSY-signal and $\overline{REQ}$-signal hardware readable
- Internal low-pass filter and 11-bit D/A converter

QUICK REFERENCE DATA

parameter	symbol	min.	typ.	max.	unit
Supply voltage	V_{DD}	–	5	–	V
Supply current	I_{DD}	–	12	*	mA
Supply current (stand-by)	$I_{DD(SB)}$	–	1	–	μA
Inputs					
Input voltage	V_{IH}	2,0	–	V_{DD}	V
Input voltage	V_{IL}	0	–	0,8	V
Input capacitance	C_I	–	7	–	pF
Outputs (D5 to D7)					
Output voltage high	V_{OH}	3,5	–	V_{DD}	V
Output voltage low	V_{OL}	0	–	0,4	V
Load capacitance	C_L	–	–	80	pF
Operating ambient temperature range	T_{amb}	−40	–	+ 85	°C

*Value to be fixed.

PACKAGE OUTLINE

24-lead DIL; plastic (SOT-101A).

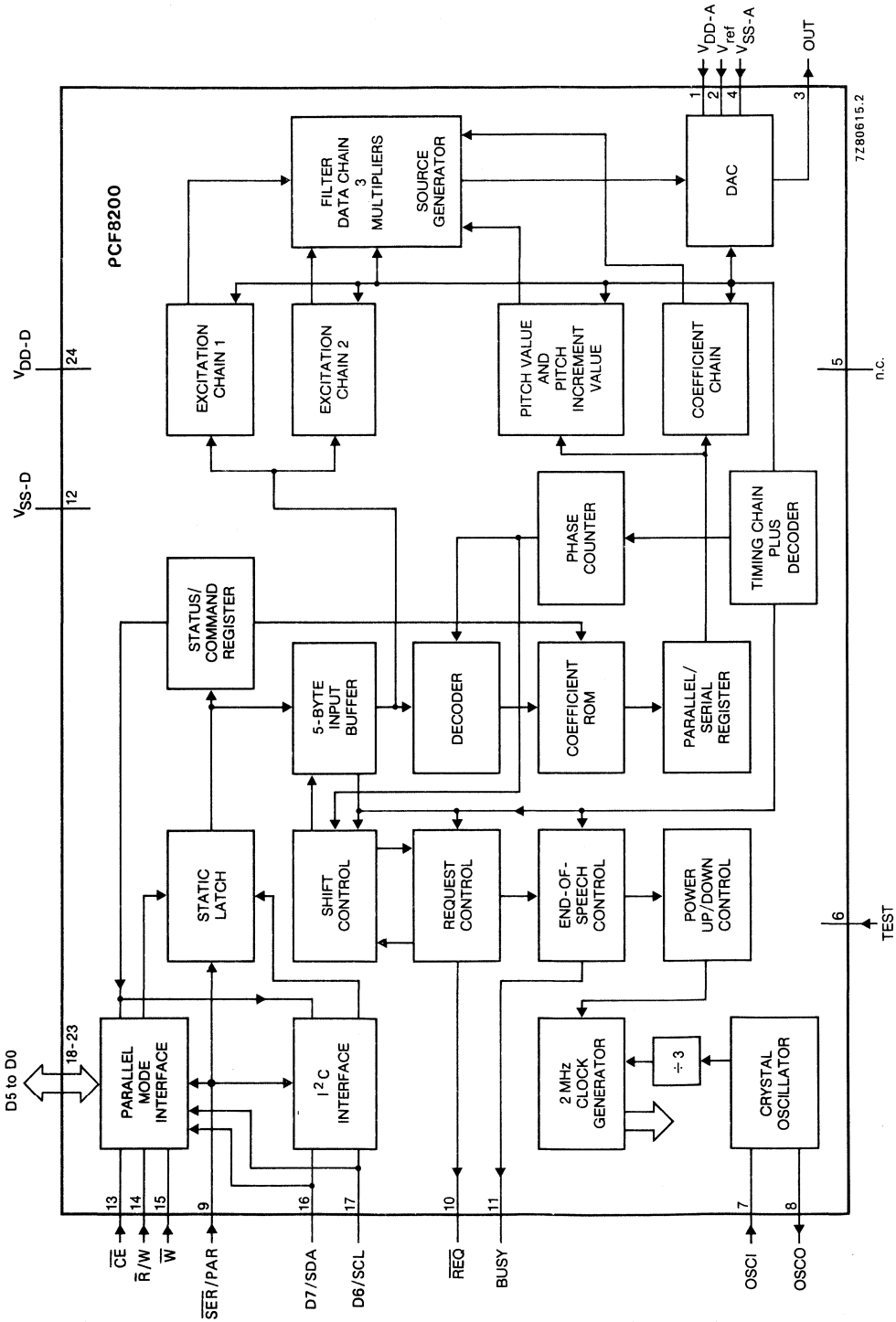


Fig. 1 Block diagram.

PINNING

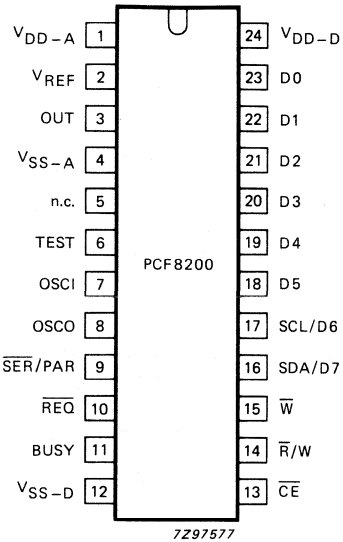


Fig. 2 Pinning diagram.

DEVELOPMENT DATA

1	V_{DD-A}	positive supply voltage for DAC output stage
2	V_{REF}	DAC reference voltage input
3	OUT	speech output
4	V_{SS-A}	negative supply voltage for DAC stage
5	n.c.	not connected
6	TEST	for normal operation this pin must be grounded (V_{SS})
7	OSCI	oscillator input
8	OSCO	oscillator output
9	$\overline{SER}$/PAR	for parallel data bus operation this pin is hard-wired to V_{DD}, or to V_{SS} to enable the I^2C bus
10	$\overline{REQ}$	status bit indicating request for data
11	BUSY	status indicating synthesizer busy
12	V_{SS-D}	negative supply voltage for digital circuits
13	$\overline{CE}$	chip-enable input
14	$\overline{R}$/W	read/write control input
15	$\overline{W}$	write input
16	SDA/D7	I^2C bus serial data input/output (serial mode) or parallel data input/output D7 (parallel mode)
17	SCL/D6	I^2C bus serial clock input/output (serial mode) or parallel data input/output D6 (parallel mode)
18	D5	parallel data input/outputs
19	D4	
20	D3	
21	D2	
22	D1	
23	D0	
24	V_{DD-D}	positive supply voltage for digital circuits

FUNCTIONAL DESCRIPTION

The synthesizer has been designed for a vocal tract modelling technique of voice synthesis. An excitation signal is fed to a series of resonators. Each resonator simulates one of the formants in the original speech. It is controlled by two parameters, one for the resonant frequency and one for the bandwidth. Five formants are needed for male speech and four for female speech. The output of this system is defined by the excitation signal, the amplitude values and the resonator settings. By periodic updating of all parameters very high quality speech can be produced.

OPERATION

Speech characteristics change quite slowly, therefore the control parameters for the speech synthesizer can be adequately updated every few tens of milliseconds with interpolation during the interval to ensure a smooth changeover from one parameter value to the next. In the PCF8200 the standard-frame duration can be set to 8,8 , 10,4, 12,8 or 17,6 milliseconds with the speed-option, speaking speed, in the command-register.
The duration of each individual speech frame is programmable to be 1, 2, 3 or 5 times the standard-frame duration.

FD1, FD0 \ FS0, FS1	10	01	00	11	
00	8,8	10,4	12,8	17,6	ms
01	17,6	20,8	25,6	35,2	ms
10	26,4	31,2	38,4	52,8	ms
11	44,0	52,0	64,0	88,0	ms

Table 1. Frame duration as a function of speed-option (FS1, FS0) and frame-duration (FD1, FD0).

The excitation signal is a random noise source for unvoiced sounds and a programmable pulse generator for voiced sounds. Both sources have an amplitude modulator which is updated 8 times in one speech-frame by linear interpolation. The pitch is updated every 1/8 of a standard frame.

The excitation signal is filtered with a five formant filter for male speech and a four formant filter for female speech. The formant filter is a cascade of all second-order sections. The control parameters, formant-frequency and formant-bandwidth, are updated eight times per speech frame by linear interpolation.
A block diagram of the formant synthesizer is shown in Fig. 3.

The filter output is upsampled to 80 kHz and filtered with a digital low-pass filter. Before the signal is digital to analogue converted (DAC), with an 11-bit switched capacitor DAC, the signal is multiplied with a DAC-amplitude factor. The use of a digital filter means that no external audio filtering is required for low-medium applications and minimal filtering is required for those applications requiring very high quality speech.

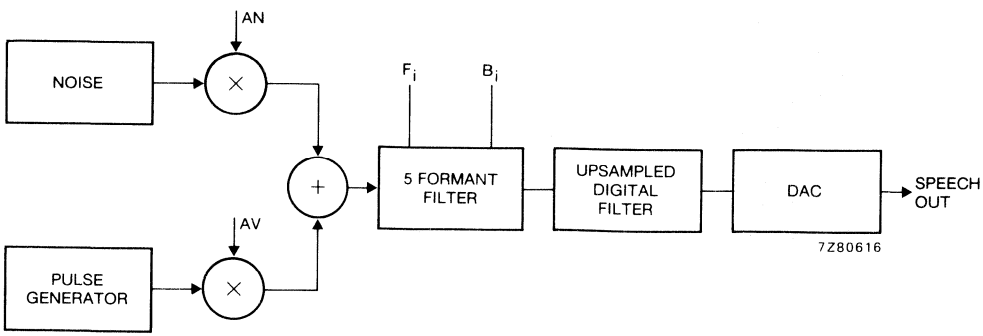


Fig. 3 Block diagram of formant synthesizer.

DATA FORMAT

Three types of format are used for data transfer to the synthesizer.

DAC-amplitude factor

The DAC-amplitude factor is one byte, which is used to optimize the digital speech signal to the 11-bit DAC. It is the first byte after a STOP or a BADSTOP or V_{DD} on. Table 2 indicates the amplitude factor.

byte	factor	dB
01110000	3,5	10,88
10110000	3,25	10,24
00110000	3,0	9,54
11010000	2,75	8,97
01010000	2,5	7,96
10010000	2,25	7,04
00010000	2,0	6,02
11100000	1,75	4,86
01100000	1,5	3,52
10100000	1,25	1,94
00100000	1,0	0,00
11000000	0,75	−2,50
01000000	0,5	−6,02
10000000	0,25	−12,04
00000000	0,0	
11110000	HEX code F0 is not allowed as a DAC amplitude	

Table 2 DAC amplitude factor.

Start pitch

The second byte after a STOP or BADSTOP, or V_{DD} on is the start pitch. It is a one byte start value for the on-chip pitch-period generator.

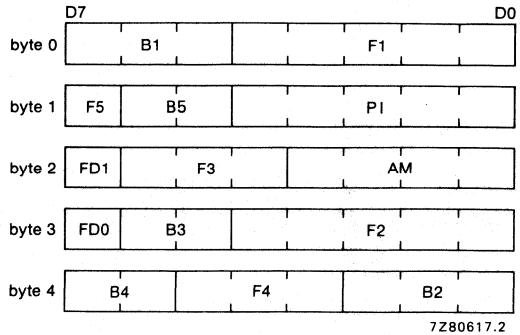
Frame Data

The frame data is a five byte block which contains the filter and source information:

pitch increment/decrement value	5 bits
amplitude	4 bits
frame duration	2 bits
frequency of 1st formant	5 bits
frequency of 2nd formant	5 bits
frequency of 3rd formant	3 bits
frequency of 4th formant	3 bits
frequency of 5th formant	1 bit
bandwidth of 1st formant	3 bits
bandwidth of 2nd formant	3 bits
bandwidth of 3rd formant	2 bits
bandwidth of 4th formant	2 bits
bandwidth of 5th formant	2 bits
	40 bits = 5 bytes

The frame-data bits are organized as shown in Fig. 4.

DEVELOPMENT DATA



It is not allowed to set byte 0 to the hexadecimal value 00.

Fig. 4 Format of frame-date.

CONTROL FORMAT

Command Write

A command write consists of two bytes, and it may occur before a data block. The four bits which can be written are shown in Fig. 5.

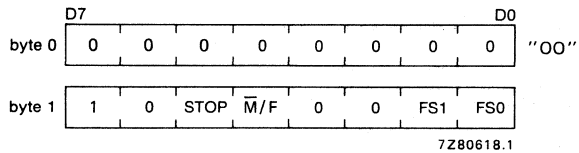


Fig. 5 Control write: first byte fixed, second byte control.

FS0, FS1 speed option

FS1	FS0	speech speed	standard-frame duration
0	0	100%	12,8 ms
0	1	145%	8,8 ms
1	0	123%	10,4 ms
1	1	73%	17,6 ms

$\overline{M}$/F, male/female option

$\overline{M}$/F = 0 male quantization table
= 1 female quantization table

STOP

STOP = 1 stop; repeat last complete frame with amplitude = 0 (no excitation signal)
= 0 if the frame data is not sent within the duration of a half frame, there will be a BADSTOP:

1. $\overline{REQ}$ = 1 STOP = 0
2. Repeat last frame with amplitude = 0
3. BUSY = 0

Status Read

Three status bits can be read out at any time without a preceding byte (00).
This is shown in Fig. 6.

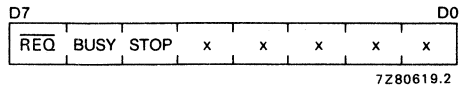


Fig. 6 Status read.

$\overline{REQ}$	= 1	No data required
	= 0	Synthesizer requesting for new data
BUSY	= 1	Busy (an utterance is pronounced)
	= 0	Idle, $\overline{REQ}$ will set to 1; the synthesizer is in STOP or BADSTOP mode
STOP		The STOP bit is the same as the stop bit written to the synthesizer during a command write. STOP = 1, BUSY = 0 stopped by the user. STOP = 0, BUSY = 0 BADSTOP because the data was not sent in time.

After initial power-up the status/command register is set to the following status:

FS0, FS1	= 0	Standard-frame duration of 12,8 ms
$\overline{M}$/F	= 0	Male quantization table
STOP	= 0	
BUSY	= 0	Idle
$\overline{REQ}$	= 1	No data required

DEVELOPMENT DATA

INTERFACE PROTOCOL

Data can be written to the synthesizer when $\overline{REQ}$ = 0 or, when $\overline{REQ}$ = 1 and BUSY = 0. Figure 7 shows the interface protocol of the synthesizer.

In parallel mode the synthesizer is activated by sending the DAC-amplitude factor. In serial mode the DAC-amplitude factor can be sent as soon as the synthesizer is powered-up.

The I²C transmitter/receiver will then acknowledge. When the request for the pitch-byte occurs the byte must be provided within the duration of a half standard frame. If the byte is not provided in time a BADSTOP will be generated.

During each data write operation, the status bit $\overline{REQ}$ will be set to '1'.
Within a frame data block, it disappears within a few microseconds, asking for the next byte of that block. If the bytes of frame data are not provided within the time-duration of a half frame, a BADSTOP will be generated.

I²C ADDRESS

On chip there is a I²C slave receiver/transmitter with the address:

7	6	5	4	3	2	1	0
0	0	1	0	0	0	0	R/W

POWER UP

The synthesizer will be set to power-up on a parallel-write sequence.

PAR-mode: The input-latches are active so they can receive the first byte

SER-mode: The I^2C transmitter/receiver will not acknowledge until the synthesizer has powered-up. To power up the synthesizer a parallel write sequence (Fig. 9) must be made to the synthesizer by using external logic for the control lines; at least one line must be toggled, $\overline{CE}$, while $\overline{W} = 0$ and $\overline{R}/W = 1$.
The synthesizer can be set to permanent power-up by hard-wired control pins ($\overline{CE} = 0$, $\overline{R}/W = 1$, $\overline{W} = 0$).

POWER DOWN MODE

When BUSY = 0 the synthesizer will be set to power-down. In the power-down mode the status/command register will be retained.
In power-down mode the clock-oscillator is switched off. After initial V_{DD} the synthesizer is in power-down mode.

HANDLING

All inputs and outputs are protected against electrostatic charge under normal handling conditions.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage	any pin with respect to V_{SS}	V_{DD}	−0,3	7,5	V
Input voltage	any pin with respect to V_{SS}	V_I	−0,3	7,5	V
Output voltage	any pin with respect to V_{SS}	V_O	−0,3	7,5	V
D.C. input diode current	$V_I < V_{SS}$	$-I_{IK}$	–	20	mA
	$V_I > V_{DD}$	I_{IK}	–	20	mA
D.C. output diode current	$V_O < V_{SS}$	$-I_{OK}$	–	20	mA
	$V_O > V_{DD}$	I_{OK}	–	20	mA
Operating ambient temperature range		T_{amb}	−40	85	°C
Storage temperature range		T_{stg}	−55	125	°C

CHARACTERISTICS

T_{amb} = −45 to + 85 °C; supply voltage (V_{DD} to V_{SS}) = 4,5 to 5,5 V with respect to V_{SS}, unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply					
Supply voltage	V_{DD}	4,5	5,0	5,5	V
Supply current	I_{DD}	–	10	–	mA
Standby current	$I_{DD(SB)}$	–	200	–	μA
Inputs					
$\overline{CE}$, R/$\overline{W}$, $\overline{W}$					
Input voltage HIGH	V_{IH}	2,0	–	V_{DD}	V
Input voltage LOW	V_{IL}	0	–	0,8	V
Input leakage current V_{in} = 0 to 5,5 V	I_{IR}	−10	–	10	μA
Rise and fall times (note 2)	t_{rf}	–	–	50	ns
Input capacitance	C_I	–	–	7	pF
OSCI					
Input voltage HIGH	V_{IH}	2,2	–	V_{DD}	V
Input voltage LOW	V_{IL}	0	–	0,8	V
Input leakage current V_{in} = 0 to 5,5 V	I_{IR}	−10	–	10	μA
Rise and fall times (note 2)	t_{rf}	–	–	50	ns
Input capacitance	C_I	–	–	7	pF
PARALLEL MODE					
Input Characteristics (D0 to D7)					
Input voltage HIGH	V_{IH}	2,0	–	V_{DD}	V
Input voltage LOW	V_{IL}	0	–	0,8	V
Input leakage current (V_{in} = 0 to 5,5 V, output off)	I_{IR}	−10	–	10	μA
Input capacitance	C_I	–	–	7	pF
Output Characteristics (D5 to D7 only)					
Output voltage HIGH (I_{OH} = −100 μA)	V_{OH}	3,5	–	V_{DD}	V
Output voltage LOW (I_{OL} = 3,2 mA)	V_{OL}	0	–	0,4	V
Load capacitance	C_L	–	–	80	pF
Rise and fall times (note 3)	t_{rf}	–	–	50	ns
SERIAL MODE					
Input characteristics (SDA and SDL)					
Input voltage HIGH	V_{IH}	3,0	–	V_{DD}	V
Input voltage LOW	V_{IL}	0	–	1,5	V
Input leakage current (V_{in} = 0 to 5,5 V, output off)	I_{IR}	−10	–	10	μA
Input capacitance	C_I	–	–	10	pF

DEVELOPMENT DATA

parameter	symbol	min.	typ.	max.	unit
Output Characteristics (SDA only, open drain)					
Output voltage LOW (I_{OL} = 3 mA)	V_{OL}	0	–	0,4	V
OSCILLATOR					
Crystal frequency	f_{XTAL}	–	6	6,1	MHz
V_{REF}					
Reference voltage	V_{REF}	1,9	–	$\frac{V_{DD}-1,5}{1,25}$	V
Input leakage current (active)	I_{IR}	–	5	–	μA
Outputs					
$\overline{REQ}$, BUSY					
Output voltage HIGH (I_{OH} = 100 μA)	V_{OH}	3,5	–	V_{DD}	V
Output voltage LOW (I_{QL} = 3,2 mA)	V_{OL}	0	–	0,4	V
Load capacitance	C_L	–	–	80	pF
Rise and fall times (note 3)	t_{rf}	–	–	50	ns
OUT					
Output voltage	V_{OUT}	0,66 x V_{REF}		1,34 x V_{REF}	V
Minimum external load		600	–	–	Ω
Timing characteristics (note 1) (Figs 8 and 9)					
Write enable	t_{WR}	200	–	–	ns
Data set-up for write	t_{DS}	150	–	–	ns
Data hold for write	t_{DH}	30	–	–	ns
Read enable	t_{RD}	200	–	–	ns
Data delay for read (note 2)	t_{DD}	–	–	150	ns
Data floating for read (note 2)	t_{DF}	–	–	150	ns
Control set-up	t_{CS}	0	–	–	ns
Control hold	t_{CH}	0	–	–	ns
REQ new (new byte of the same speech frame)	t_{RN}	–	* (≈ 3)		μs
REQ Valid	t_{RV}	0	–	–	ns
REQ Hold	t_{RH}	–	250	*	ns

NOTES TO THE CHARACTERISTICS

1. Timing reference level is 1,5 V; supply 5 V ± 10%; temperature range of −40 °C to 85 °C.
2. Levels greater than 2 V for a '1' or less than 0,8 V for a '0' are reached with a load of one TTL input and 50 pF.
3. Rise and fall times between 0,6 V and 2,2 V levels.

*Value to be fixed.

DEVELOPMENT DATA

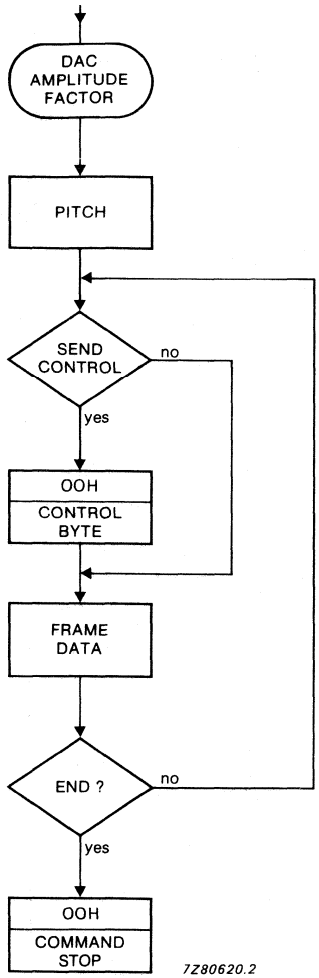
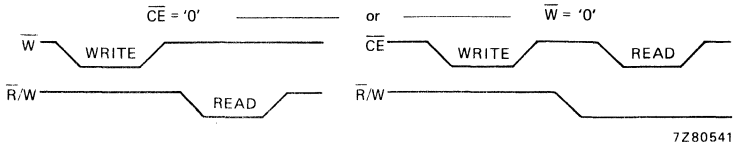


Fig. 7 Interface protocol.

Timing diagrams

The control signals $\overline{CE}$, $\overline{R}/W$ and $\overline{W}$ have been specified to enable easy interface to most microprocessors and microcomputers. For instance with connection to an MAB8048 microcomputer the $\overline{R}/W$ and $\overline{W}$ inputs can be used as the RD and WR strobe inputs.



Typical connection of control signals.

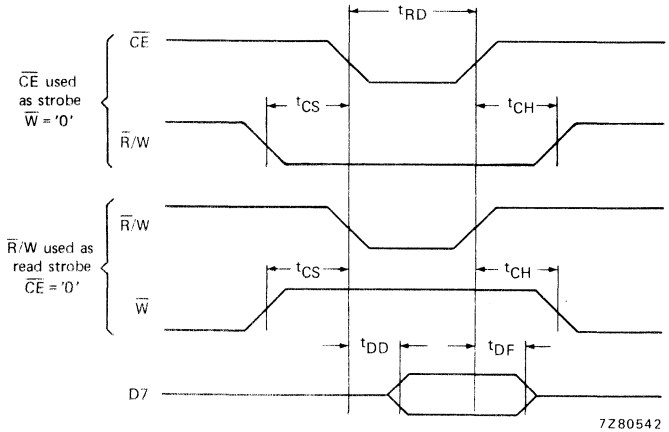


Fig. 8 Read timing.

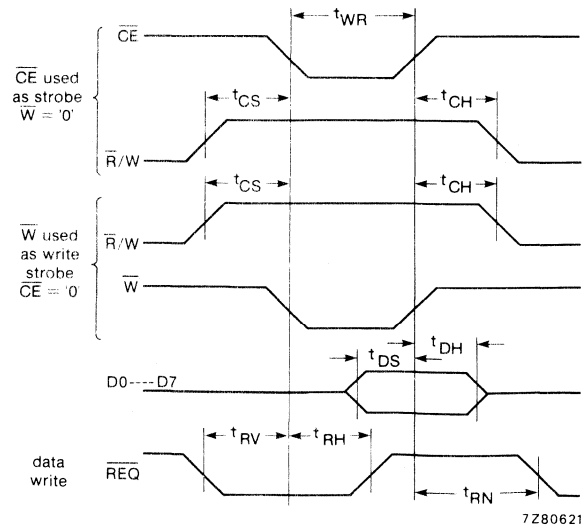


Fig. 9 Write timing.

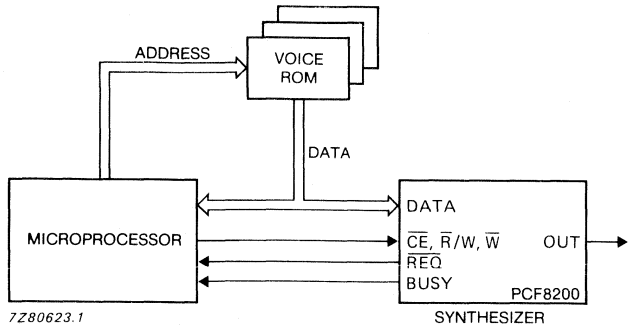


Fig. 10 Typical application configuration with parallel interface.

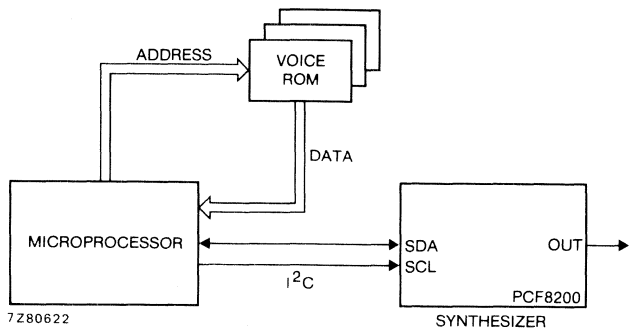


Fig. 11 Typical application configuration with series interface.

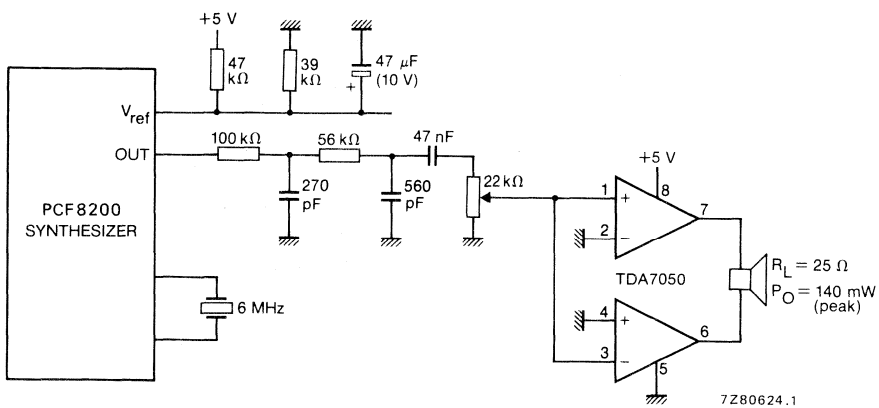


Fig. 12 An example of an output configuration.

SUPERSEDES DATA OF JUNE 1986

UNIVERSAL LCD DRIVER FOR LOW MULTIPLEX RATES

GENERAL DESCRIPTION

The PCF8566 is a peripheral device which interfaces to almost any liquid crystal display (LCD) having low multiplex rates. It generates the drive signals for any static or multiplexed LCD containing up to four backplanes and up to 24 segments and can easily be cascaded for larger LCD applications. The PCF8566 is compatible with most microprocessors/microcontrollers and communicates via a two-line bidirectional bus (I^2C). Communication overheads are minimized by a display RAM with auto-incremented addressing, by hardware subaddressing and by display memory switching (static and duplex drive modes).

Features

- Single-chip LCD controller/driver
- Selectable backplane drive configuration: static or 2/3/4 backplane multiplexing
- Selectable display bias configuration: static, 1/2 or 1/3
- Internal LCD bias generation with voltage-follower buffers
- 24 segment drives: up to twelve 8-segment numeric characters; up to six 15-segment alphanumeric characters; or any graphics of up to 96 elements
- 24 x 4-bit RAM for display data storage
- Auto-incremented display data loading across device subaddress boundaries
- Display memory bank switching in static and duplex drive modes
- Versatile blinking modes
- LCD and logic supplies may be separated
- 2,5 V to 6 V power supply range
- Low power consumption
- Power-saving mode for extremely low power consumption in battery-operated and telephone applications
- I^2C bus interface
- TTL/CMOS compatible
- Compatible with any 4-bit, 8-bit or 16-bit microprocessors/microcontrollers
- May be cascaded for large LCD applications (up to 1536 segments possible)
- Cascadable with the 40 segment LCD driver PCF8576
- Optimized pinning for single plane wiring in both single and multiple PCF8566 applications
- Space-saving 40-lead plastic mini-pack (VSO-40; SOT-158A)
- No external components required (even in multiple device applications)
- Manufactured in silicon gate CMOS process

PACKAGE OUTLINES

PCF8566P: 40-lead DIL; plastic (SOT-129).
PCF8566T: 40-lead mini-pack (VSO-40; SOT-158A).

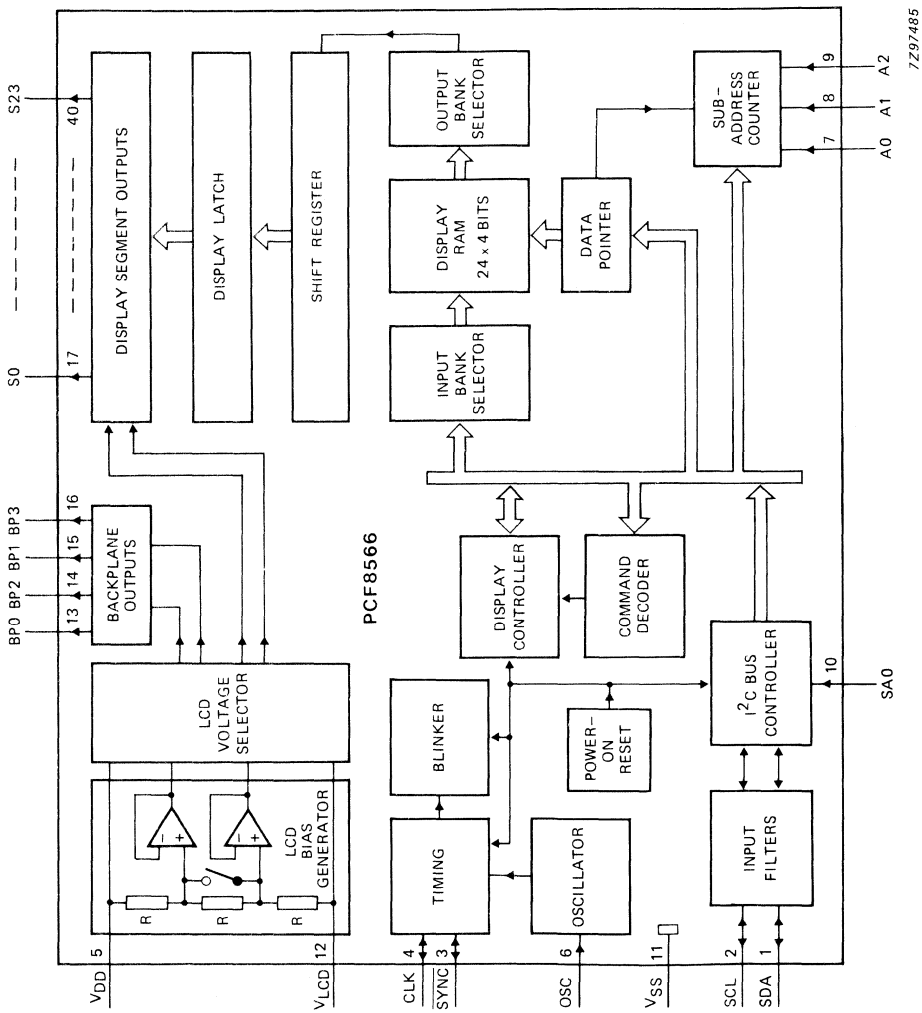


Fig. 1 Block diagram.

DEVELOPMENT DATA

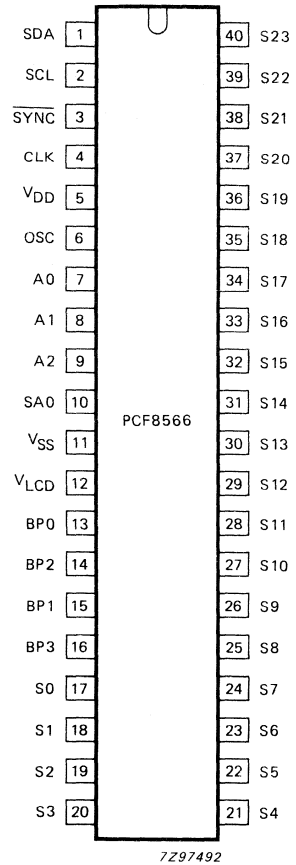


Fig. 2 Pinning diagram.

PINNING

1	SDA	I^2C bus data input/output
2	SCL	I^2C bus clock input/output
3	$\overline{SYNC}$	cascade synchronization input/output
4	CLK	external clock input/output
5	V_{DD}	positive supply voltage
6	OSC	oscillator input
7	A0	I^2C bus subaddress inputs
8	A1	
9	A2	
10	SA0	I^2C bus slave address bit 0 input
11	V_{SS}	logic ground
12	V_{LCD}	LCD supply voltage
13	BP0	LCD backplane outputs
14	BP2	
15	BP1	
16	BP3	
17	S0	LCD segment outputs
to	to	
40	S23	

FUNCTIONAL DESCRIPTION

The PCF8566 is a versatile peripheral device designed to interface any microprocessor to a wide variety of LCDs. It can directly drive any static or multiplexed LCD containing up to four backplanes and up to 24 segments. The display configurations possible with the PCF8566 depend on the number of active backplane outputs required; a selection of display configurations is given in Table 1.

Table 1 Selection of display configurations

active back-plane outputs	no. of segments	7-segment numeric	14-segment alphanumeric	dot matrix
4	96	12 digits + 12 indicator symbols	6 characters + 12 indicator symbols	96 dots (4 x 24)
3	72	9 digits + 9 indicator symbols	4 characters + 16 indicator symbols	72 dots (3 x 24)
2	48	6 digits + 6 indicator symbols	3 characters + 6 indicator symbols	48 dots (2 x 24)
1	24	3 digits + 3 indicator symbols	1 characters + 10 indicator symbols	24 dots

All of the display configurations given in Table 1 can be implemented in the typical system shown in Fig. 3. The host microprocessor/microcontroller maintains the two-line I^2C bus communication channel with the PCF8566. The internal oscillator is selected by tying OSC (pin 6) to V_{SS}. The appropriate biasing voltages for the multiplexed LCD waveforms are generated internally. The only other connections required to complete the system are to the power supplies (V_{DD}, V_{SS} and V_{LCD}) and to the LCD panel chosen for the application.

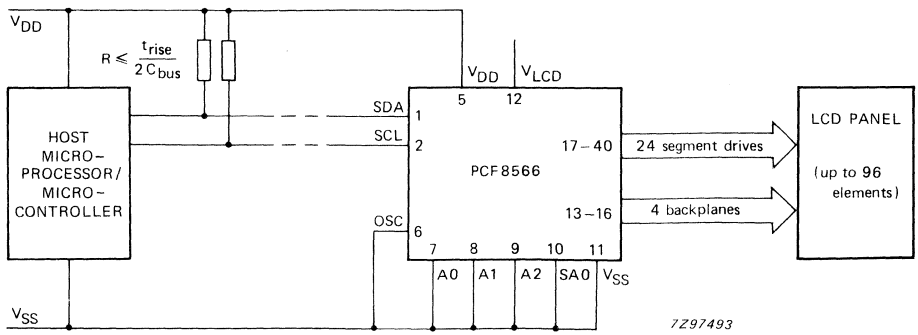


Fig. 3 Typical system configuration.

Power-on reset

At power-on the PCF8566 resets to a defined starting condition as follows:

1. All backplane outputs are set to V_{DD}.
2. All segment outputs are set to V_{DD}.
3. The drive mode '1 : 4 multiplex with 1/3 bias' is selected.
4. Blinking is switched off.
5. Input and output bank selectors are reset (as defined in Table 5).
6. The I^2C bus interface is initialized.
7. The data pointer and the subaddress counter are cleared.

Data transfers on the I^2C bus should be avoided for 1 ms following power-on to allow completion of the reset action.

LCD bias generator

The full-scale LCD voltage (V_{op}) is obtained from $V_{DD} - V_{LCD}$. The LCD voltage may be temperature compensated externally through the V_{LCD} supply to pin 12. Fractional LCD biasing voltages are obtained from an internal voltage divider of three series resistors connected between V_{DD} and V_{LCD}. The centre resistor can be switched out of circuit to provide a ½ bias voltage level for the 1 : 2 multiplex configuration.

LCD voltage selector

The LCD voltage selector coordinates the multiplexing of the LCD according to the selected LCD drive configuration. The operation of the voltage selector is controlled by MODE SET commands from the command decoder. The biasing configurations that apply to the preferred modes of operation, together with the biasing characteristics as functions of $V_{op} = V_{DD} - V_{LCD}$ and the resulting discrimination ratios (D), are given in Table 2.

Table 2 Preferred LCD drive modes: summary of characteristics

LCD drive mode	LCD bias configuration	$\frac{V_{off(rms)}}{V_{op}}$	$\frac{V_{on\ (rms)}}{V_{op}}$	$D = \frac{V_{on(rms)}}{V_{off(rms)}}$
static (1 BP)	static (2 levels)	0	1	∞
1 : 2 MUX (2 BP)	1/2 (3 levels)	$\sqrt{2}/4 = 0{,}354$	$\sqrt{10}/4 = 0{,}791$	$\sqrt{5} = 2{,}236$
1 : 2 MUX (2 BP)	1/3 (4 levels)	$1/3 = 0{,}333$	$\sqrt{5}/3 = 0{,}745$	$\sqrt{5} = 2{,}236$
1 : 3 MUX (3 BP)	1/3 (4 levels)	$1/3 = 0{,}333$	$\sqrt{33}/9 = 0{,}638$	$\sqrt{33}/3 = 1{,}915$
1 : 4 MUX (4 BP)	1/3 (4 levels)	$1/3 = 0{,}333$	$\sqrt{3}/3 = 0{,}577$	$\sqrt{3} = 1{,}732$

DEVELOPMENT DATA

LCD voltage selector (continued)

A practical value for V_{op} is determined by equating $V_{off(rms)}$ with a defined LCD threshold voltage (V_{th}), typically when the LCD exhibits approximately 10% contrast. In the static drive mode a suitable choice is $V_{op} \gtrapprox 3\ V_{th}$.
Multiplex drive ratios of 1 : 3 and 1 : 4 with 1/2 bias are possible but the discrimination and hence the contrast ratios are smaller ($\sqrt{3} = 1{,}732$ for 1 : 3 multiplex or $\sqrt{21}/3 = 1{,}528$ for 1 : 4 multiplex).
The advantage of these modes is a reduction of the LCD full scale voltage V_{op} as follows:

1 : 3 multiplex (1/2 bias) : $V_{op} = \sqrt{6}\ V_{off(rms)} = 2{,}449\ V_{off(rms)}$

1 : 4 multiplex (1/2 bias) : $V_{op} = 4\sqrt{3}/3\ V_{off(rms)} = 2{,}309\ V_{off(rms)}$

These compare with $V_{op} = 3\ V_{off(rms)}$ when 1/3 bias is used.

LCD drive mode waveforms

The static LCD drive mode is used when a single backplane is provided in the LCD. Backplane and segment drive waveforms for this mode are shown in Fig. 4.

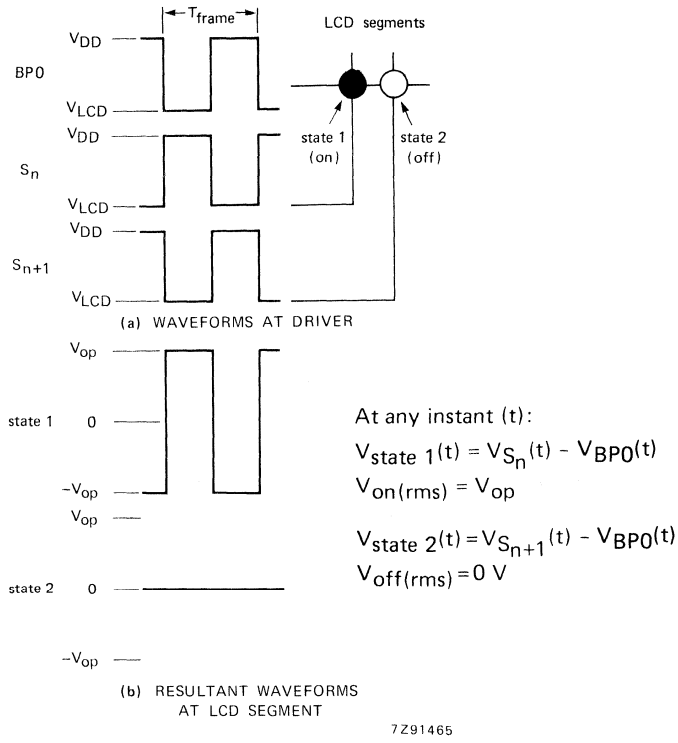


Fig. 4 Static drive mode waveforms: $V_{op} = V_{DD} - V_{LCD}$.

When two backplanes are provided in the LCD the 1 : 2 multiplex drive mode applies. The PCF8566 allows use of 1/2 or 1/3 bias in this mode as shown in Figs 5 and 6.

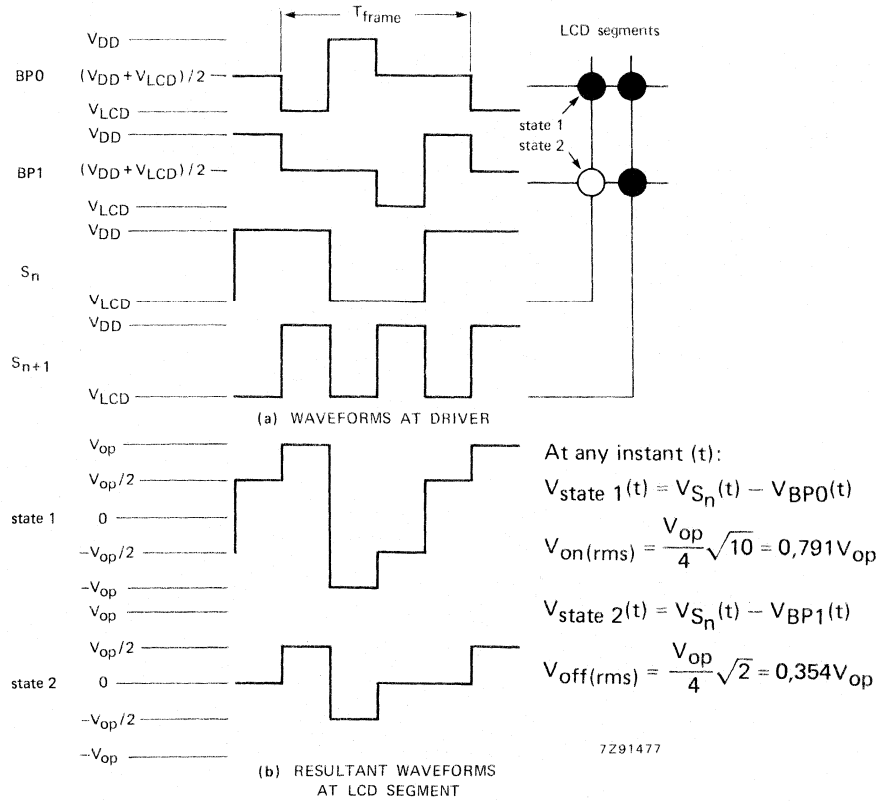


Fig. 5 Waveforms for 1 : 2 multiplex drive mode with 1/2 bias: $V_{op} = V_{DD} - V_{LCD}$.

DEVELOPMENT DATA

LCD drive mode waveforms (continued)

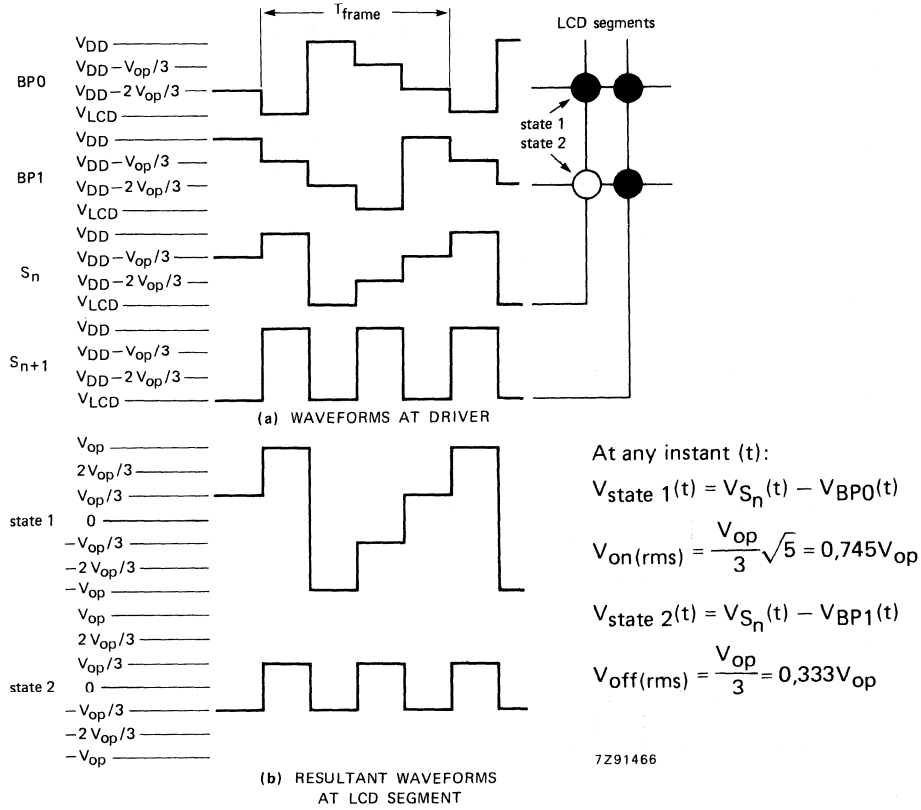


Fig. 6 Waveforms for 1 : 2 multiplex drive mode with 1/3 bias: $V_{op} = V_{DD} - V_{LCD}$.

The backplane and segment drive wavefront for the 1 : 3 multiplex drive mode (three LCD backplanes) and for the 1 : 4 multiplex drive mode (four LCD backplanes) are shown in Figs 7 and 8 respectively.

DEVELOPMENT DATA

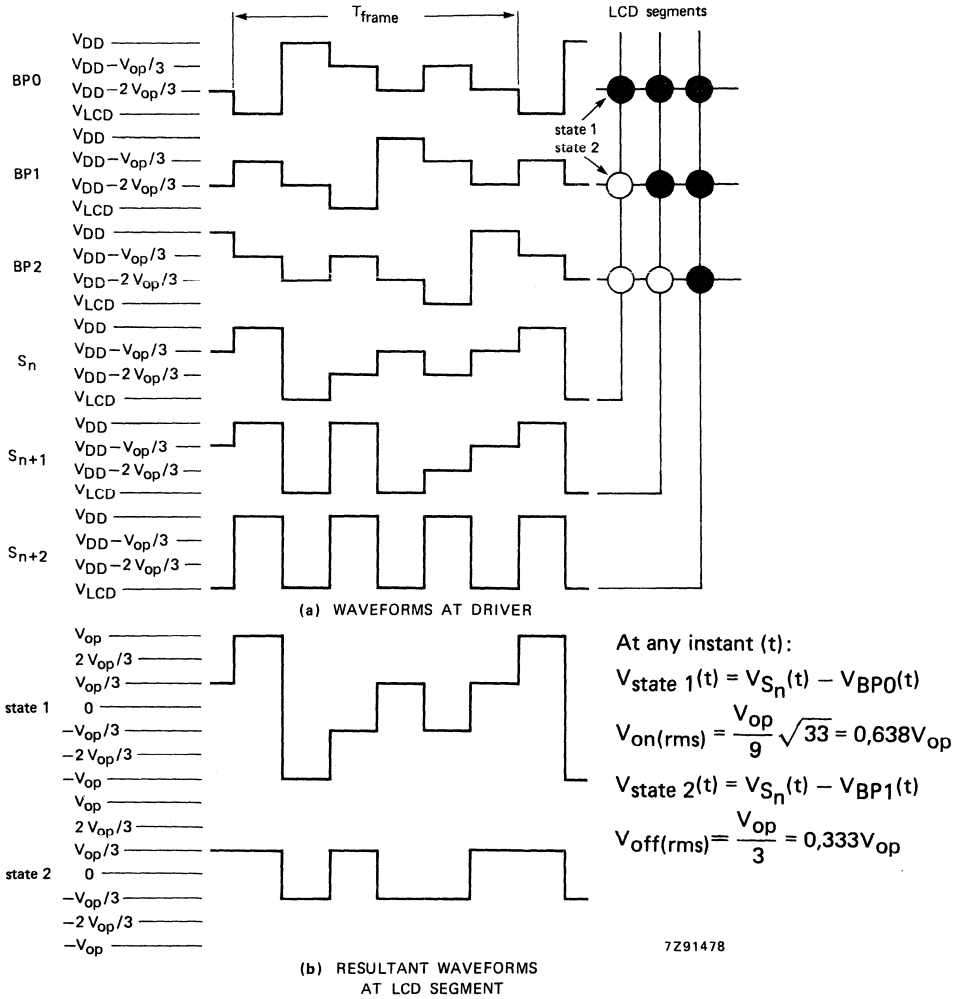


Fig. 7 Waveforms for 1 : 3 multiplex drive mode: $V_{op} = V_{DD} - V_{LCD}$.

LCD drive mode waveforms (continued)

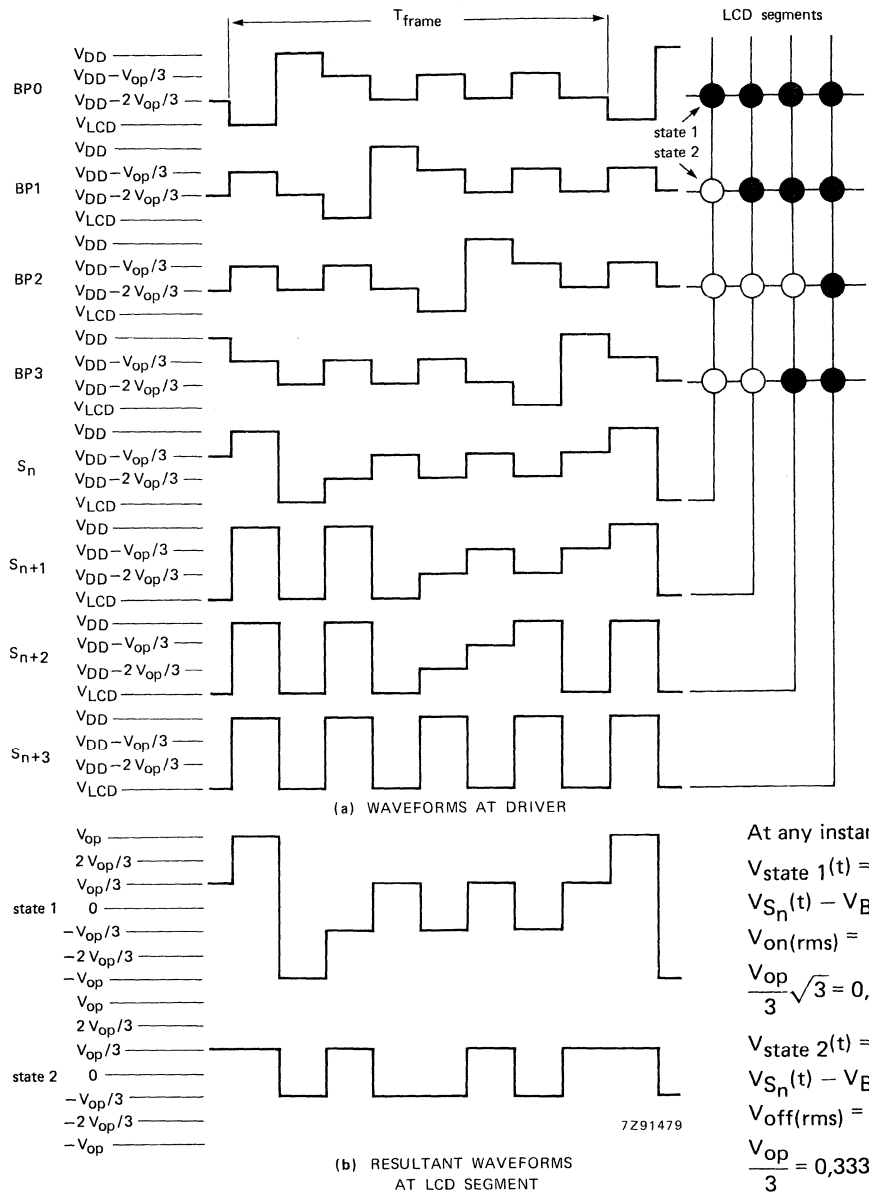


Fig. 8 Waveforms for 1 : 4 multiplex drive mode: $V_{op} = V_{DD} - V_{LCD}$.

Oscillator

The internal logic and the LCD drive signals of the PCF8566 or PCF8576 are timed either by the built-in oscillator or from an external clock.

The clock frequency (f_{CLK}) determines the LCD frame frequency and the maximum rate for data reception from the I^2C bus. To allow I^2C bus transmissions at their maximum data rate of 100 kHz, f_{CLK} should be chosen to be above 125 kHz.

A clock signal must always be supplied to the device; removing the clock may freeze the LCD in a DC state.

Internal clock

When the internal oscillator is used, OSC (pin 6) should be tied to V_{SS}. In this case, the output from CLK (pin 4) provides the clock signal for cascaded PCF8566s and PCF8576s in the system.

External clock

The condition for external clock is made by tying OSC (pin 6) to V_{DD}; CLK (pin 4) then becomes the external clock input.

Timing

The timing of the PCF8566 organizes the internal data flow of the device. This includes the transfer of display data from the display RAM to the display segment outputs. In cascaded applications, the synchronization signal $\overline{SYNC}$ maintains the correct timing relationship between the PCF8566s in the system. The timing also generates the LCD frame frequency which it derives as an integer multiple of the clock frequency (Table 3). The frame frequency is set by MODE SET commands when internal clock is used, or by the frequency applied to pin 4 when external clock is used.

Table 3 LCD frame frequencies

PCF8566 mode	f_{frame}	nominal f_{frame} (Hz)
normal mode	$f_{CLK}/2880$	64
power-saving mode	$f_{CLK}/480$	64

The ratio between the clock frequency and the LCD frame frequency depends on the mode in which the device is operating. In the power-saving mode the reduction ratio is six times smaller, this allows the clock frequency to be reduced by a factor of six. The reduced clock frequency results in a significant reduction in power dissipation. The lower clock frequency has the disadvantage of increasing the response time when large amounts of display data are transmitted on the I^2C bus. When a device is unable to 'digest' a display data byte before the next one arrives, it holds the SCL line low until the first display data byte is stored. This slows down the transmission rate of the I^2C bus but no data loss occurs.

Display latch

The display latch holds the display data while the corresponding multiplex signals are generated. There is a one-to-one relationship between the data in the display latch, the LCD segment outputs and one column of the display RAM.

Shift register

The shift register serves to transfer display information from the display RAM to the display latch while previous data are displayed.

Segment outputs

The LCD drive section includes 24 segment outputs S0 to S23 (pins 17 to 40) which should be connected directly to the LCD. The segment output signals are generated in accordance with the multiplexed backplane signals and with the data resident in the display latch. When less than 24 segment outputs are required the unused segment outputs should be left open-circuit.

Backplane outputs

The LCD drive section includes four backplane outputs BP0 to BP3 which should be connected directly to the LCD. The backplane output signals are generated in accordance with the selected LCD drive mode. If less than four backplane outputs are required the unused outputs can be left open. In the 1 : 3 multiplex drive mode BP3 carries the same signal as BP1, therefore these two adjacent outputs can be tied together to give enhanced drive capabilities. In the 1 : 2 multiplex drive mode BP0 and BP2, BP1 and BP3 respectively carry the same signals and may also be paired to increase the drive capabilities. In the static drive mode the same signal is carried by all four backplane outputs and they can be connected in parallel for very high drive requirements.

Display RAM

The display RAM is a static 24 x 4-bit RAM which stores LCD data. A logic 1 in the RAM bit-map indicates the 'on' state of the corresponding LCD segment; similarly, a logic 0 indicates the 'off' state. There is a one-to-one correspondence between the RAM addresses and the segment outputs, and between the individual bits of a RAM word and the backplane outputs. The first RAM column corresponds to the 24 segments operated with respect to backplane BP0 (Fig. 9). In multiplexed LCD applications the segment data of the second, third and fourth column of the display RAM are time-multiplexed with BP1, BP2 and BP3 respectively.

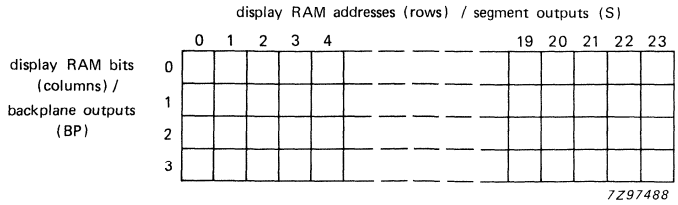


Fig. 9 Display RAM bit-map showing direct relationship between display RAM addresses and segment outputs, and between bits in a RAM word and backplane outputs.

When display data are transmitted to the PCF8566 the display bytes received are stored in the display RAM according to the selected LCD drive mode. To illustrate the filling order, an example of a 7-segment numeric display showing all drive modes is given in Fig. 10; the RAM filling organization depicted applies equally to other LCD types.

With reference to Fig. 10, in the static drive mode the eight transmitted data bits are placed in bit 0 of eight successive display RAM addresses. In the 1 : 2 multiplex drive mode the eight transmitted data bits are placed in bits 0 and 1 of four successive display RAM addresses. In the 1 : 3 multiplex drive mode these bits are placed in bits 0, 1 and 2 of three successive addresses, with bit 2 of the third address left unchanged. This last bit may, if necessary, be controlled by an additional transfer to this address but care should be taken to avoid overriding adjacent data because full bytes are always transmitted. In the 1 : 4 multiplex drive mode the eight transmitted data bits are placed in bits 0, 1, 2 and 3 of two successive display RAM addresses.

Data pointer

The addressing mechanism for the display RAM is realized using the data pointer. This allows the loading of an individual display data byte, or a series of display data bytes, into any location of the display RAM. The sequence commences with the initialization of the data pointer by the LOAD DATA POINTER command. Following this, an arriving data byte is stored starting at the display RAM address indicated by the data pointer thereby observing the filling order shown in Fig. 10. The data pointer is automatically incremented according to the LCD configuration chosen. That is, after each byte is stored, the contents of the data pointer are incremented by eight (static drive mode), by four (1 : 2 multiplex drive mode), by three (1 : 3 multiplex drive mode) or by two (1 : 4 multiplex drive mode).

Subaddress counter

The storage of display data is conditioned by the contents of the subaddress counter. Storage is allowed to take place only when the contents of the subaddress counter agree with the hardware subaddress applied to A0, A1 and A2 (pins 7, 8, and 9). A0, A1 and A2 should be tied to V_{SS} or V_{DD}. The subaddress counter value is defined by the DEVICE SELECT command. If the contents of the subaddress counter and the hardware subaddress do not agree then data storage is inhibited but the data pointer is incremented as if data storage had taken place. The subaddress counter is also incremented when the data pointer overflows.

The storage arrangements described lead to extremely efficient data loading in cascaded applications. When a series of display bytes are being sent to the display RAM, automatic wrap-over to the next PCF8566 occurs when the last RAM address is exceeded. Subaddressing across device boundaries is successful even if the change to the next device in the cascade occurs within a transmitted character.

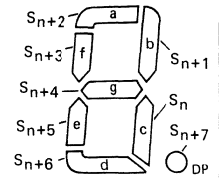
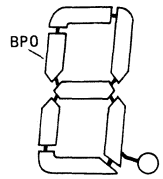
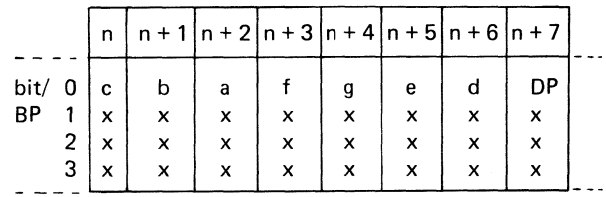
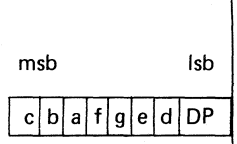
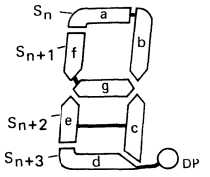
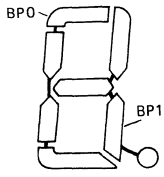
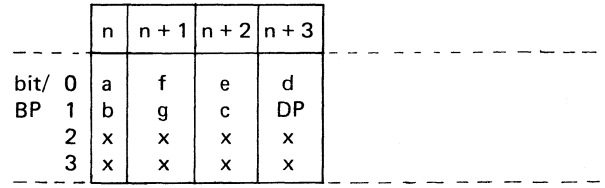
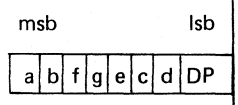
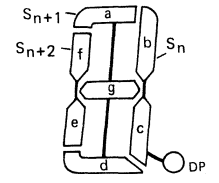
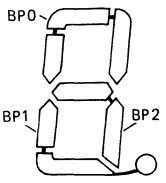
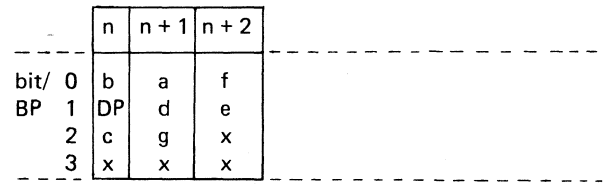
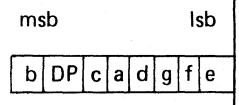
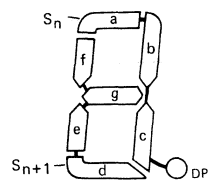
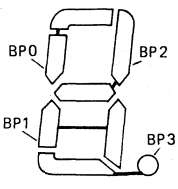
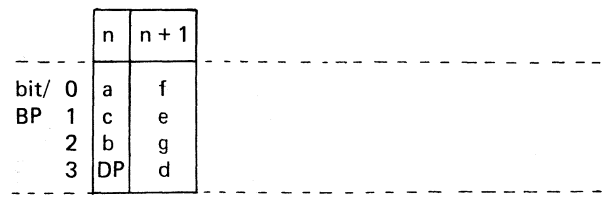
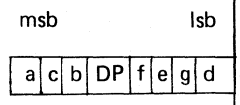
drive mode	LCD segments	LCD backplanes	display RAM filling order	transmitted display byte
static				
1 : 2 multiplex				
1 : 3 multiplex				
1 : 4 multiplex				

Fig. 10 Relationships between LCD layout, drive mode, display RAM filling order and display data transmitted over the I²C bus (x = data bit unchanged).

7Z91469

Output bank selector

This selects one of the four bits per display RAM address for transfer to the display latch. The actual bit chosen depends on the particular LCD drive mode in operation and on the instant in the multiplex sequence. In 1 : 4 multiplex, all RAM addresses of bit 0 are the first to be selected, these are followed by the contents of bit 1, bit 2 and then bit 3. Similarly in 1 : 3 multiplex, bits 0, 1 and 2 are selected sequentially. In 1 : 2 multiplex, bits 0 then 1 are selected and, in the static mode, bit 0 is selected.

The PCF8566 includes a RAM bank switching feature in the static and 1 : 2 multiplex drive modes. In the static drive mode, the BANK SELECT command may request the contents of bit 2 to be selected for display instead of bit 0 contents. In the 1 : 2 drive mode, the contents of bits 2 and 3 may be selected instead of bits 0 and 1. This gives the provision for preparing display information in an alternative bank and to be able to switch to it once it is assembled.

Input bank selector

The input bank selector loads display data into the display RAM according to the selected LCD drive configuration. Display data can be loaded in bit 2 in static drive mode or in bits 2 and 3 in 1 : 2 drive mode by using the BANK SELECT command. The input bank selector functions independently of the output bank selector.

Blinker

The display blinking capabilities of the PCF8566 are very versatile. The whole display can be blinked at frequencies selected by the BLINK command. The blinking frequencies are integer multiples of the clock frequency; the ratios between the clock and blinking frequencies depend on the mode in which the device is operating, as shown in Table 4.

An additional feature is for an arbitrary selection of LCD segments to be blinked. This applies to the static and 1 : 2 LCD drive modes and can be implemented without any communication overheads. By means of the output bank selector, the displayed RAM banks are exchanged with alternate RAM banks at the blinking frequency. This mode can also be specified by the BLINK command.

In the 1 : 3 and 1 : 4 multiplex modes, where no alternate RAM bank is available, groups of LCD segments can be blinked by selectively changing the display RAM data at fixed time intervals.

If the entire display is to be blinked at a frequency other than the nominal blinking frequency, this can be effectively performed by resetting and setting the display enable bit E at the required rate using the MODE SET command.

Table 4 Blinking frequencies

blinking mode	normal operating mode ratio	power-saving mode ratio	nominal blinking frequency f_{blink} (Hz)
off	–	–	blinking off
2 Hz	$f_{CLK}/92160$	$f_{CLK}/15360$	2
1 Hz	$f_{CLK}/184320$	$f_{CLK}/30720$	1
0,5 Hz	$f_{CLK}/368640$	$f_{CLK}/61440$	0,5

CHARACTERISTICS OF THE I²C BUS

The I²C bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals.

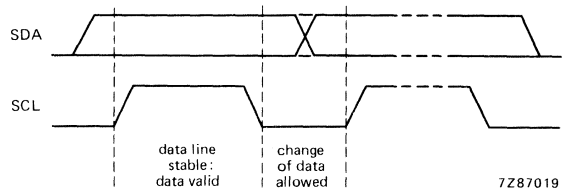


Fig. 11 Bit transfer.

Start and stop conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line while the clock is HIGH is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the stop condition (P).

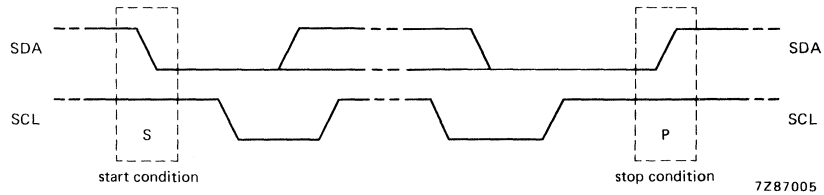


Fig. 12 Definition of start and stop conditions.

System configuration

A device generating a message is a "transmitter", a device receiving a message is a "receiver". The device that controls the message is the "master" and the devices which are controlled by the master are the "slaves".

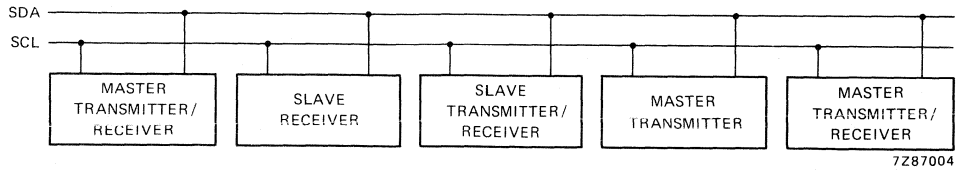


Fig. 13 System configuration.

Acknowledge

The number of data bytes transferred between the start and stop conditions from transmitter to receiver is not limited. Each byte is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter whereas the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse, set up and hold times must be taken into account. A master receiver must signal an end of data to the transmitter by *not* generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

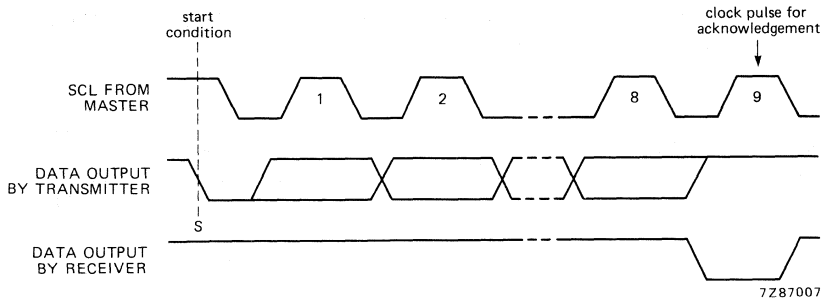


Fig. 14 Acknowledgement on the I²C bus.

Note

The general characteristics and detailed specification of the I²C bus are available on request.

PCF8566 I²C bus controller

The PCF8566 acts as an I²C slave receiver. It does not initiate I²C bus transfers or transmit data to an I²C master receiver. The only data output from the PCF8566 are the acknowledge signals of the selected devices. Device selection depends on the I²C bus slave address, on the transferred command data and on the hardware subaddress.

In single device applications, the hardware subaddress inputs A0, A1 and A2 are normally left open-circuit or tied to V_{SS} which defines the hardware subaddress 0. In multiple device applications A0, A1 and A2 are left open-circuit or tied to V_{SS} or V_{DD} according to a binary coding scheme such that no two devices with a common I²C slave address have the same hardware subaddress.

In the power-saving mode it is possible that the PCF8566 is not able to keep up with the highest transmission rates when large amounts of display data are transmitted. If this situation occurs, the PCF8566 forces the SCL line LOW until its internal operations are completed. This is known as the 'clock synchronization feature' of the I²C bus and serves to slow down fast transmitters. Data loss does not occur.

Input filters

To enhance noise immunity in electrically adverse environments, RC low-pass filters are provided on the SDA and SCL lines.

I²C bus protocol

Two I²C bus slave addresses (0111110 and 0111111) are reserved for PCF8566. The least-significant bit of the slave address that a PCF8566 will respond to is defined by the level tied at its input SA0 (pin 10). Therefore, two types of PCF8566 can be distinguished on the same I²C bus which allows:

(a) up to 16 PCF8566s on the same I²C bus for very large LCD applications;

(b) the use of two types of LCD multiplex on the same I²C bus.

The I²C bus protocol is shown in Fig. 15. The sequence is initiated with a start condition (S) from the I²C bus master which is followed by one of the two PCF8566 slave addresses available. All PCF8566s with the corresponding SA0 level acknowledge in parallel the slave address but all PCF8566s with the alternative SA0 level ignore the whole I²C bus transfer. After acknowledgement, one or more command bytes (m) follow which define the status of the addressed PCF8566s. The last command byte is tagged with a cleared most-significant bit, the continuation bit C. The command bytes are also acknowledged by all addressed PCF8566s on the bus.

After the last command byte, a series of display data bytes (n) may follow. These display data bytes are stored in the display RAM at the address specified by the data pointer and the subaddress counter. Both data pointer and subaddress counter are automatically updated and the data are directed to the intended PCF8566 device. The acknowledgement after each byte is made only by the (A0, A1, A2) addressed PCF8566. After the last display byte, the I²C bus master issues a stop condition (P).

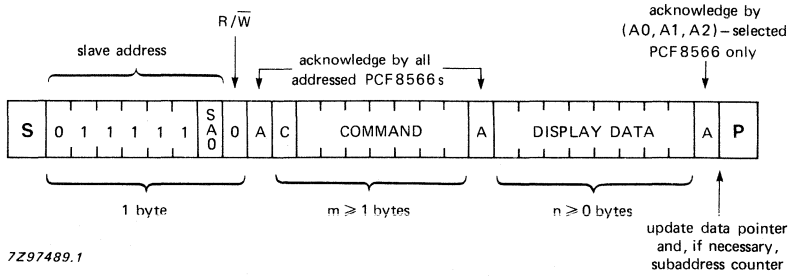


Fig. 15 I²C bus protocol.

Command decoder

The command decoder identifies command bytes that arrive on the I²C bus. All available commands carry a continuation bit C in their most-significant bit position (Fig. 16). When this bit is set, it indicates that the next byte of the transfer to arrive will also represent a command. If the bit is reset, it indicates the last command byte of the transfer. Further bytes will be regarded as display data.

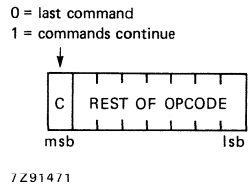


Fig. 16 General format of command byte.

The five commands available to the PCF8566 are defined in Table 5.

Command decoder (continued)

Table 5 Definition of PCF8566 commands

command/opcode	options	description
MODE SET C 1 0 LP E B M1 M0	LCD drive mode: bits M1 M0 static (1 BP): 0 1 1 : 2 MUX (2 BP): 1 0 1 : 3 MUX (3 BP): 1 1 1 : 4 MUX (4 BP): 0 0 LCD bias: bit B 1/3 bias: 0 1/2 bias: 1 display status: bit E disabled (blank): 0 enabled: 1 mode: bit LP normal mode: 0 power-saving mode: 1	Defines LCD drive mode Defines LCD bias configuration Defines display status The possibility to disable the display allows implementation of blinking under external control Defines power dissipation mode
LOAD DATA POINTER C 0 0 P4 P3 P2 P1 P0	bits P4 P3 P2 P1 P0 5-bit binary value of 0 to 23	Five bits of immediate data, bits P4 to P0, are transferred to the data pointer to define one of twenty-four display RAM addresses
DEVICE SELECT C 1 1 0 0 A2 A1 A0	bits A0 A1 A2 3-bit binary value of 0 to 7	Three bits of immediate data, bits A0 to A2, are transferred to the subaddress counter to define one of eight hardware subaddresses

DEVELOPMENT DATA

command/opcode	options	description
BANK SELECT C 1 1 1 1 0 I O	static / 1 : 2 MUX / bit I RAM bit 0 / RAM bits 0, 1 / 0 RAM bit 2 / RAM bits 2, 3 / 1 static / 1 : 2 MUX / bit O RAM bit 0 / RAM bits 0, 1 / 0 RAM bit 2 / RAM bits 2, 3 / 1	Defines input bank selection (storage of arriving display data) Defines output bank selection (retrieval of LCD display data) The BANK SELECT command has no effect in 1 : 3 and 1 : 4 multiplex drive modes
BLINK C 1 1 1 0 A BF1 BF0	blink frequency / bits BF1 / BF0 off / 0 / 0 2 Hz / 0 / 1 1 Hz / 1 / 0 0,5 Hz / 1 / 1 blink mode / bit A normal blinking / 0 alternation blinking / 1	Defines the blinking frequency Selects the blinking mode; normal operation with frequency set by bits BF1, BF0, or blinking by alternation of display RAM banks. Alternation blinking does not apply in 1 : 3 and 1 : 4 multiplex drive modes

Display controller

The display controller executes the commands identified by the command decoder. It contains the status registers of the PCF8566 and coordinates their effects. The controller is also responsible for loading display data into the display RAM as required by the filling order.

Cascaded operation

In large display configurations, up to 16 PCF8566s can be distinguished on the same I^2C bus by using the 3-bit hardware subaddress (A0, A1, A2) and the programmable I^2C slave address (SA0). It is also possible to cascade up to 16 PCF8566s. When cascaded, several PCF8566s are synchronized so that they can share the backplane signals from one of the devices in the cascade. Such an arrangement is cost-effective in large LCD applications since the backplane outputs of only one device need to be through-plated to the backplane electrodes of the display. The other PCF8566s of the cascade contribute additional segment outputs but their backplane outputs are left open-circuit (Fig. 17).

The $\overline{SYNC}$ line is provided to maintain the correct synchronization between all cascaded PCF8566s. This synchronization is guaranteed after the power-on reset. The only time that $\overline{SYNC}$ is likely to be needed is if synchronization is accidently lost (e.g. by noise in adverse electrical environments; or by the definition of a multiplex mode when PCF8566s with differing SA0 levels are cascaded). $\overline{SYNC}$ is organized as an input/output pin; the output section being realized as an open-drain driver with an internal pull-up resistor. A PCF8566 asserts the $\overline{SYNC}$ line at the onset of its last active backplane signal and monitors the $\overline{SYNC}$ line at all other times. Should synchronization in the cascade be lost, it will be restored by the first PCF8566 to assert $\overline{SYNC}$. The timing relationships between the backplane waveforms and the $\overline{SYNC}$ signal for the various drive modes of the PCF8576 are shown in Fig. 18. The waveforms are identical with the parent device PCF8576. Casadability between PCF8566s and PCF8576s is possible, giving cost effective LCD applications.

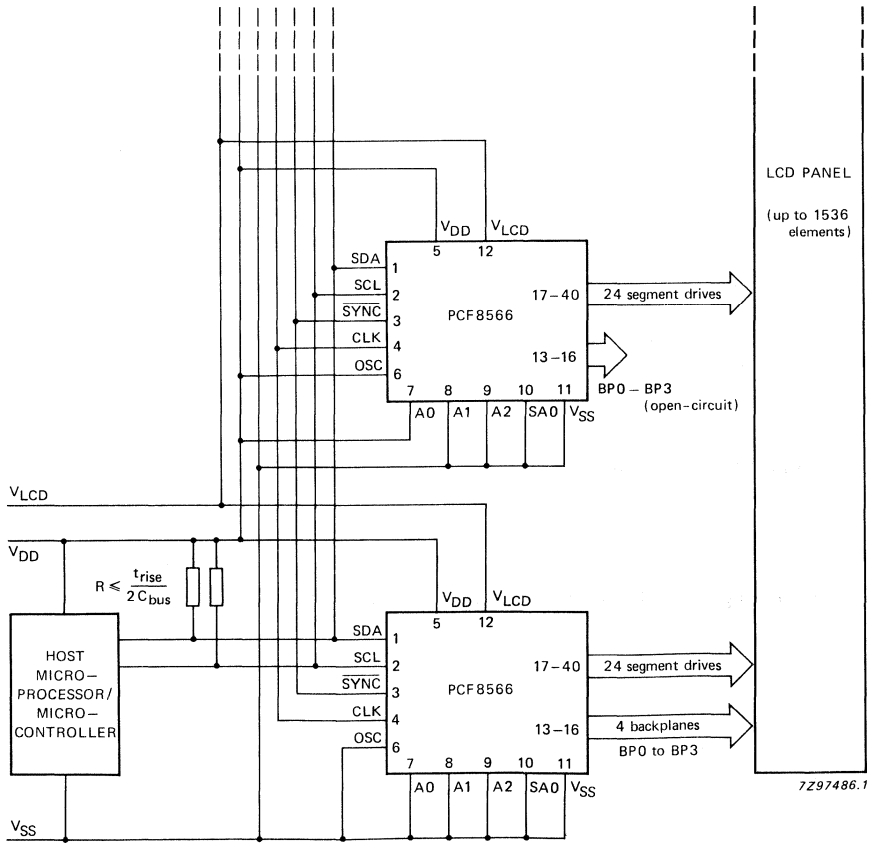


Fig. 17 Cascaded PCF8566 configuration.

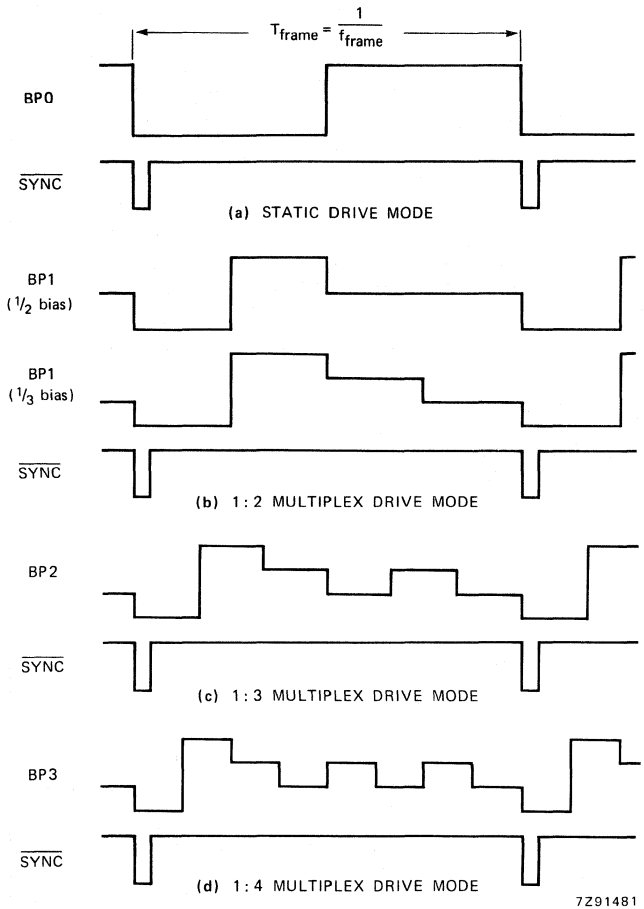


Fig. 18 Synchronization of the cascade for the various PCF8566 drive modes.

For single plane wiring of PCF8566s, see section "APPLICATION INFORMATION".

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range; see note	V_{DD}		−0,5 to + 7 V
LCD supply voltage range	V_{LCD}		V_{DD} −7 to V_{DD} V
Input voltage range (SCL; SDA; A0 to A2; OSC; CLK; $\overline{SYNC}$; SA0)	V_I		V_{SS} −0,5 to V_{DD} + 0,5 V
Output voltage range (S0 to S23; BP0 to BP3)	V_O		V_{LCD}−0,5 to V_{DD} + 0,5 V
DC input current	$\pm I_I$	max.	20 mA
DC output current	$\pm I_O$	max.	25 mA
V_{DD}, V_{SS} or V_{LCD} current	$\pm I_{DD}$, $\pm I_{SS}$, $\pm I_{LCD}$	max.	50 mA
Power dissipation per package	P_{tot}	max.	400 mW
Power dissipation per output	P_O	max.	100 mW
Storage temperature range	T_{stg}		−65 to + 150 °C

Note

Inputs and outputs are protected against electrostatic discharges in normal handling. However, to be totally safe, it is advised to take handling precautions appropriate to handling MOS devices (see 'Handling MOS devices').

DC CHARACTERISTICS

V_{SS} = 0 V; V_{DD} = 2,5 to 6 V; V_{LCD} = V_{DD} −2,5 to V_{DD} −6 V;

T_{amb} = −40 to +85 °C; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Operating supply voltage	V_{DD}	2,5	–	6	V
LCD supply voltage	V_{LCD}	V_{DD} −6	–	V_{DD} −2,5	V
Operating supply current (normal mode) at f_{CLK} = 200 kHz (note 1)	I_{DD}	–	30	90	μA
Power-saving mode supply current at V_{DD} = 3,5 V; V_{LCD} = 0 V; f_{CLK} = 35 kHz; A0, A1 and A2 tied to V_{SS} (note 1)	I_{LP}	–	15	40	μA

parameter	symbol	min.	typ.	max.	unit
Logic					
Input voltage LOW	V_{IL}	V_{SS}	–	0,3 V_{DD}	V
Input voltage HIGH	V_{IH}	0,7 V_{DD}	–	V_{DD}	V
Output voltage LOW at I_O = 0 mA	V_{OL}	–	–	0,05	V
Output voltage HIGH at I_O = 0 mA	V_{OH}	V_{DD} −0,05	–	–	V
Output current LOW (CLK, $\overline{SYNC}$) at V_{OL} = 1,0 V; V_{DD} = 5 V	I_{OL1}	1	–	–	mA
Output current HIGH (CLK) at V_{OH} = 4,0 V; V_{DD} = 5 V	I_{OH}	–	–	−1	mA
Output current LOW (SDA; SCL) at V_{OL} = 0,4 V; V_{DD} = 5 V	I_{OL2}	3	–	–	mA
Leakage current (SA0, CLK, OSC, A0, A1, A2, SCL, SDA) at $V_I = V_{SS}$ or V_{DD}	$\pm I_L$	–	–	1	μA
Pull-down current (A0; A1; A2; OSC) at V_I = 1 V and V_{DD} = 5 V	I_{pd}	15	50	150	μA
Pull-up resistor ($\overline{SYNC}$)	R_{SYNC}	15	25	60	kΩ
Power-on reset level (note 2)	V_{REF}	–	1,3	2,0	V
Tolerable spike width on bus	t_{sw}	–	–	100	ns
Input capacitance (note 3)	C_I	–	–	7	pF
LCD outputs					
D.C. voltage component (BP0 to BP3) at C_{BP} = 35 nF	$\pm V_{BP}$	–	20	–	mV
D.C. voltage component (S0 to S23) at C_S = 5 nF	$\pm V_S$	–	20	–	mV
Output impedance (BP0 to BP3) at $V_{LCD} = V_{DD}$ −5 V (note 4)	R_{BP}	–	1	5	kΩ
Output impedance (S0 to S23) at $V_{LCD} = V_{DD}$ −5 V (note 4)	R_S	–	3	7,0	kΩ

DEVELOPMENT DATA

AC CHARACTERISTICS (note 5)

V_{SS} = 0 V; V_{DD} = 2,5 to 6 V; V_{LCD} = V_{DD} −2,5 to V_{DD} −6 V;
T_{amb} = −40 to +85 °C; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Oscillator frequency (normal mode) at V_{DD} = 5 V (note 6)	f_{CLK}	125	200	315	kHz
Oscillator frequency (power-saving mode) at V_{DD} = 3,5 V	f_{CLKLP}	21	31	48	kHz
CLK HIGH time	t_{CLKH}	1	–	–	μs
CLK LOW time	t_{CLKL}	1	–	–	μs
$\overline{\text{SYNC}}$ propagation delay	t_{PSYNC}	–	–	400	ns
$\overline{\text{SYNC}}$ LOW time	t_{SYNCL}	1	–	–	μs
Driver delays with test loads at V_{LCD} = V_{DD} −5 V	t_{PLCD}	–	–	30	μs
I²C bus					
Bus free time	t_{BUF}	4,7	–	–	μs
Start condition hold time	$t_{HD;STA}$	4	–	–	μs
SCL LOW time	t_{LOW}	4,7	–	–	μs
SCL HIGH time	t_{HIGH}	4	–	–	μs
Start condition set-up time (repeated start code only)	$t_{SU;STA}$	4,7	–	–	μs
Data hold time	$t_{HD;DAT}$	0	–	–	μs
Data set-up time	$t_{SU;DAT}$	250	–	–	ns
Rise time	t_r	–	–	1	μs
Fall time	t_f	–	–	300	ns
Stop condition set-up time	$t_{SU;STO}$	4,7	–	–	μs

Notes to characteristics

1. Outputs open; inputs at V_{SS} or V_{DD}; external clock with 50% duty factor; I²C bus inactive.
2. Resets all logic when $V_{DD} < V_{REF}$.
3. Periodically sampled, not 100% tested.
4. Outputs measured one at a time.
5. All timing values referred to V_{IH} and V_{IL} levels with an input voltage swing of V_{SS} to V_{DD}.
6. At $f_{CLK} < 125$ kHz, I²C bus maximum transmission speed is derated.

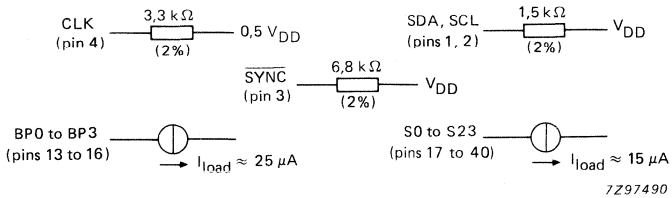


Fig. 19 Test loads.

DEVELOPMENT DATA

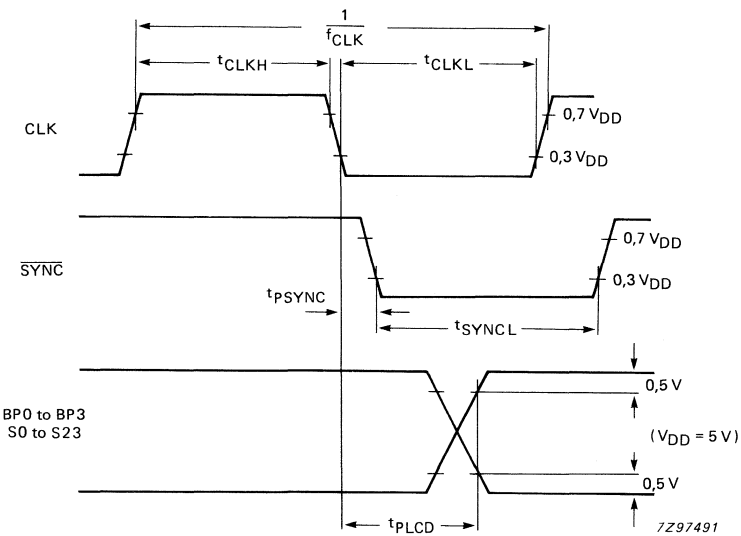


Fig. 20 Driver timing waveforms.

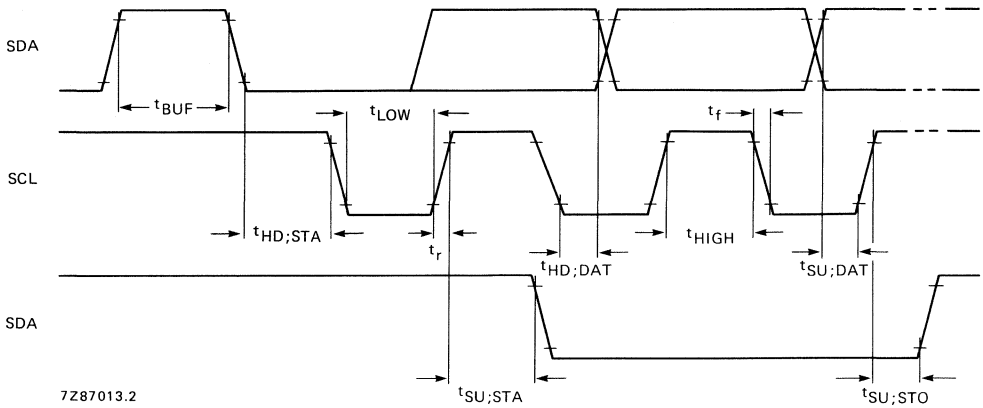
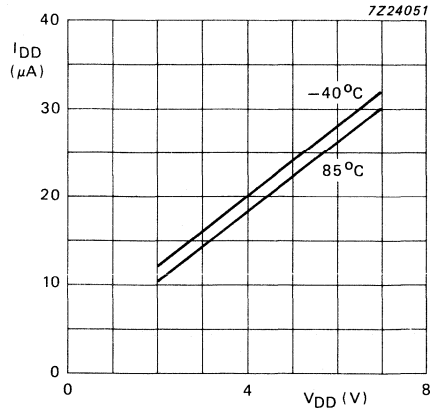
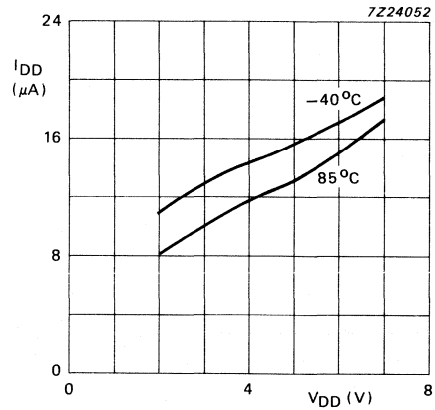


Fig. 21 I^2C bus timing waveforms.



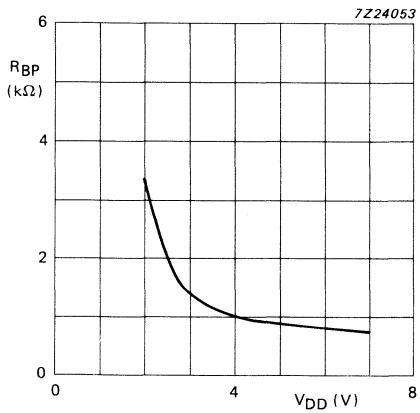
(a) Normal mode; V_{LCD} = 0 V; external clock = 200 kHz.



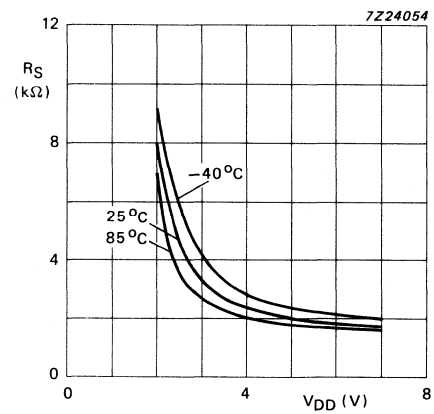
(b) Low power mode; V_{LCD} = 0 V; external clock = 35 kHz.

Fig. 22 Typical supply current characteristics.

DEVELOPMENT DATA



(a) Backplane output impedance BP0 to BP3 (R_{BP}); V_{DD} = 5 V; T_{amb} = −40 to + 85 °C.



(b) Segment output impedance S0 to S23 (R_S); V_{DD} = 5 V.

Fig. 23 Typical characteristics of LCD outputs.

APPLICATION INFORMATION

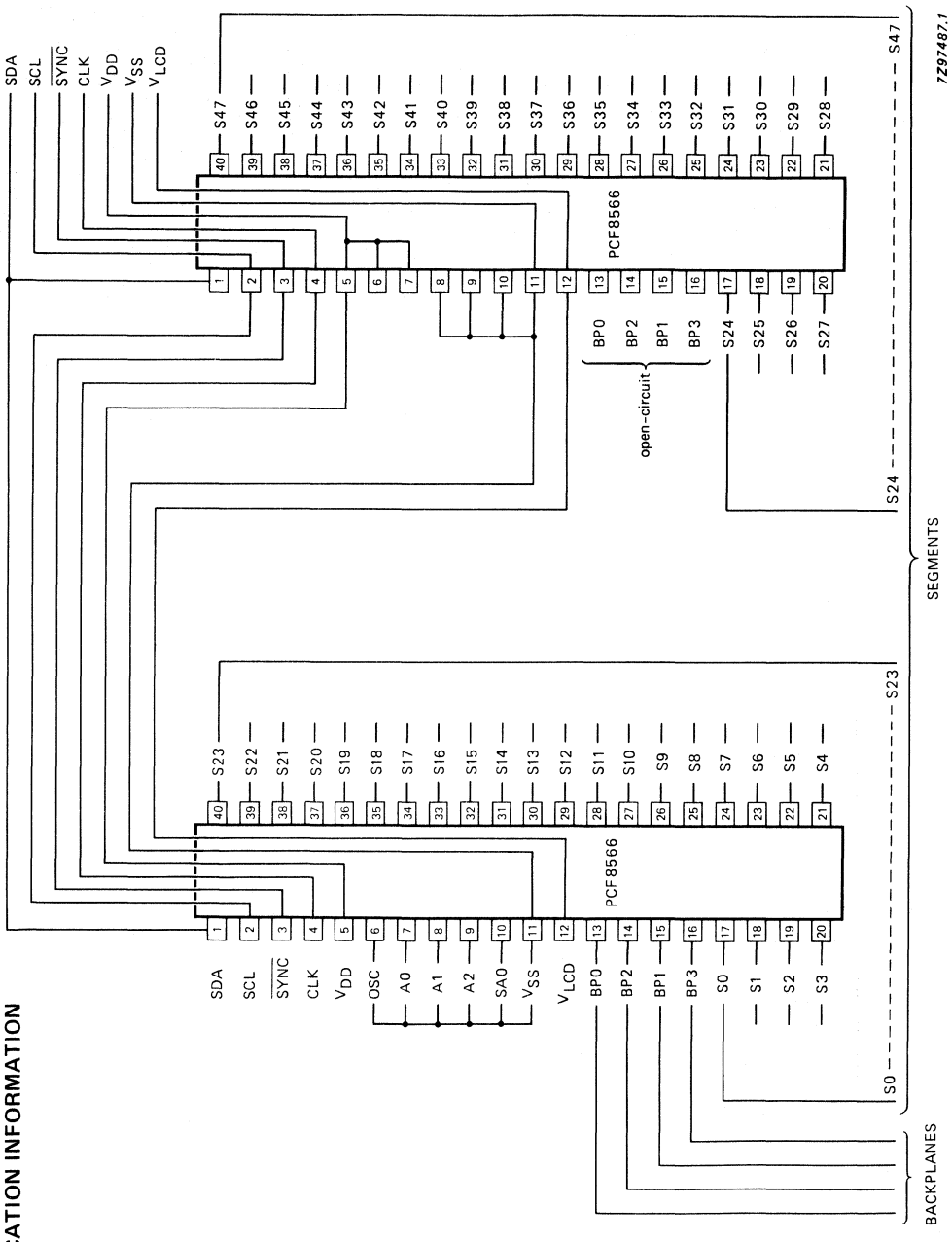


Fig. 24 Single plane wiring of packaged PCF8566s.

SUPERSEDES DATA OF AUGUST 1987

128 x 8 BIT/256 x 8 BIT STATIC RAMs WITH I²C BUS INTERFACE

GENERAL DESCRIPTION

The PCF8570, PCF8570C and PCF8571 are low-power static CMOS RAMs. The PCF8570 and PCF8570C are organized as 256 words by 8-bits and the PCF8571 is organized as 128 words by 8-bits. Addresses and data are transferred serially via a two-line bidirectional bus (I²C). The built-in word address register is incremented automatically after each written or read data byte. Three address pins A0, A1 and A2 are used for hardware address, allowing the use of up to eight devices connected to the bus without additional hardware. For system expansion over 8 devices the PCF8570/71 can be used in conjunction with the PCF8750C which has an alternative slave address for memory extension up to 16 devices.

Features

- Operating supply voltage 2,5 V to 6 V
- Low data retention voltage min. 1,0 V
- Low standby current max. 15 μA
- Power saving mode typ. 50 nA
- Serial input/output bus (I²C)
- Address by 3 hardware address pins
- Automatic word address incrementing
- 8-lead DIL package

Applications

- Telephony — RAM expansion for stored numbers in repertory dialling (e.g. PCD3343 applications)
- Radio and television — channel presets
- Video cassette recorder — channel presets
- General purpose — RAM expansion for the microcontroller families MAB8400, PCF84CXX and most other microcontrollers

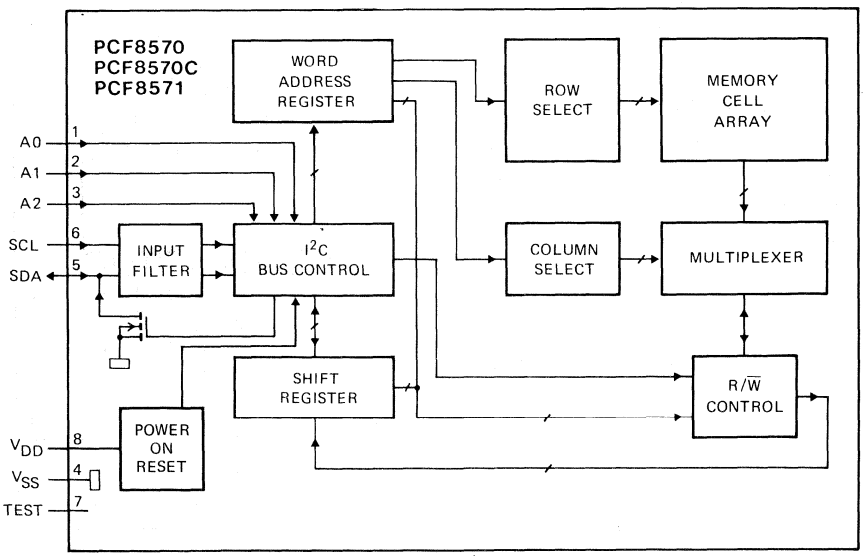


Fig. 1 Block diagram.

7Z90775.3

PACKAGE OUTLINES

PCF8570/PCF8570C/PCF8571/P: 8-lead DIL; plastic (SOT-97).
PCF8570/PCF8570C/PCF8571/T: 8-lead mini-pack (SO-8L; SOT-176).

PINNING

1 to 3	A0 to A2	address inputs
4	V_{SS}	negative supply
5	SDA	serial data line (I^2C bus)
6	SCL	serial clock line (I^2C bus)
7	TEST	test input for test speed-up; must be connected to V_{SS} when not in use (power saving mode, see Figs 12 and 13)
8	V_{DD}	positive supply

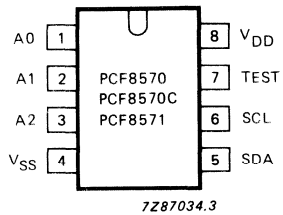


Fig. 2 Pinning diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range (pin 8)	V_{DD}		−0,8 to + 8,0 V
Voltage range on any input	V_I		−0,8 to V_{DD} + 0,8 V
DC input current (any input)	$\pm I_I$	max.	10 mA
DC output current (any output)	$\pm I_O$	max.	10 mA
Supply current (pin 8 or pin 4)	$\pm I_{DD}$; I_{SS}	max.	50 mA
Power dissipation per package	P_{tot}	max.	300 mW
Power dissipation per output	P	max.	50 mW
Storage temperature range	T_{stg}		−65 to + 150 °C
Operating ambient temperature range	T_{amb}		−40 to + 85 °C

CHARACTERISTICS

V_{DD} = 2,5 to 6 V; V_{SS} = 0 V; T_{amb} = −40 to + 85 °C unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply					
Supply voltage	V_{DD}	2,5	–	6	V
Supply current at $V_I = V_{SS}$ or V_{DD};					
operating at f_{SCL} = 100 kHz	I_{DD}	–	–	200	μA
standby at f_{SCL} = 0 Hz	I_{DDO}	–	–	15	μA
standby at T_{amb} = −25 to + 70 °C	I_{DDO}	–	–	5	μA
Power-on reset voltage level*	V_{POR}	1,5	1,9	2,3	V
Inputs; input/output SDA					
Input voltage LOW**	V_{IL}	−0,8	–	0,3 x V_{DD}	V
Input voltage HIGH**	V_{IH}	0,7 x V_{DD}	–	V_{DD} + 0,8	V
Output current LOW at V_{OL} = 0,4 V	I_{OL}	3	–	–	mA
Output leakage current HIGH at $V_{OH} = V_{DD}$	I_{OH}	–	–	250	nA
Input leakage current at $V_I = V_{DD}$ or V_{SS}	$\pm I_I$	–	–	250	nA
Clock frequency (Fig. 7)	f_{SCL}	0	–	100	kHz
Input capacitance (SCL, SDA) at $V_I = V_{SS}$	C_I	–	–	7	pF
Tolerable spike width on bus	t_{SW}	–	–	100	ns
LOW V_{DD} data retention					
Supply voltage for data retention	V_{DDR}	1	–	6	V
Supply current at V_{DDR} = 1 V	I_{DDR}	–	–	5	μA
Supply current at V_{DDR} = 1 V; T_{amb} = −25 to + 70 °C	I_{DDR}	–	–	2	μA
Power saving mode (Fig. 12 and 13)					
Supply current at T_{amb} = 25 °C; TEST = V_{DD};					
PCF8570/8570C	I_{DDR}	–	50	400	nA
PCF8571	I_{DDR}	–	50	200	nA
Recovery time	t_{HD2}	–	50	–	μs

* The power-on reset circuit resets the I²C bus logic when $V_{DD} < V_{POR}$. The status of the device after a power-on reset condition can be tested by sending the slave address and testing the acknowledge bit.

** If the input voltages are a diode voltage above or below the supply voltage V_{DD} or V_{SS} an input current will flow: this current must not exceed ± 0,5 mA.

CHARACTERISTICS OF THE I²C BUS

The I²C bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals.

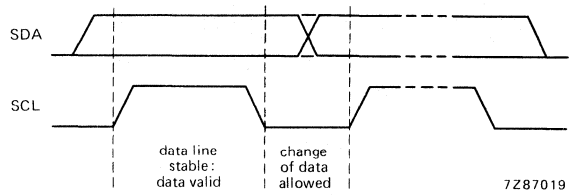


Fig. 3 Bit transfer.

Start and stop conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the stop condition (P).

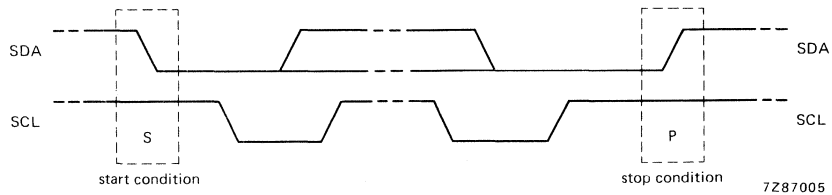


Fig. 4 Definition of start and stop conditions.

System configuration

A device generating a message is a "transmitter", a device receiving a message is the "receiver". The device that controls the message is the "master" and the devices which are controlled by the master are the "slaves".

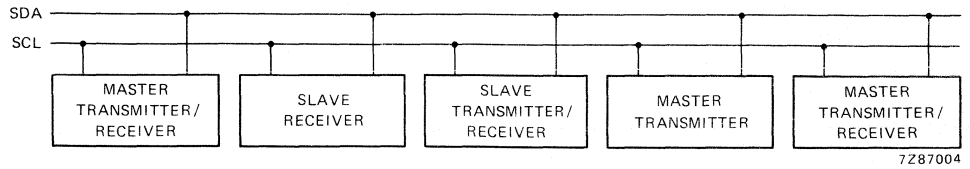


Fig. 5 System configuration.

Acknowledge

The number of data bytes transferred between the start and stop conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter whereas the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse, set-up and hold times must be taken into account. A master receiver must signal an end of data to the transmitter by *not* generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

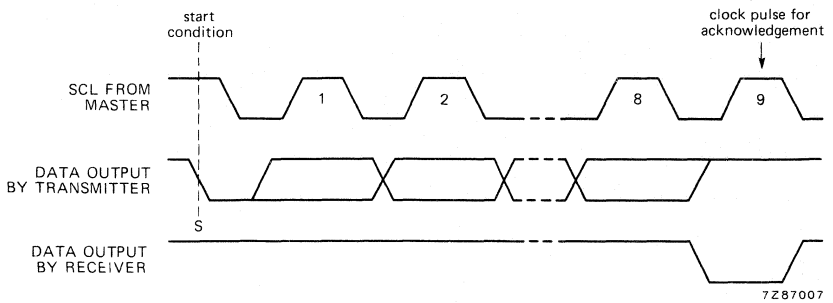


Fig. 6 Acknowledgement on the I²C bus.

Timing specifications

All the timing values are valid within the operating supply voltage and ambient temperature range and refer to V_{IL} and V_{IH} with an input voltage swing of V_{SS} to V_{DD}.

parameter	symbol	min.	typ.	max.	unit
SCL clock frequency	f_{SCL}	–	–	100	kHz
Tolerable spike width on bus	t_{SW}	–	–	100	ns
Bus free time	t_{BUF}	4,0	–	–	μs
Start condition set-up time	$t_{SU;STA}$	4,0	–	–	μs
Start condition hold time	$t_{HD;STA}$	4,7	–	–	μs
SCL LOW time	t_{LOW}	4,7	–	–	μs
SCL HIGH time	t_{HIGH}	4,0	–	–	μs
SCL and SDA rise time	t_r	–	–	1,0	μs
SCL and SDA fall time	t_f	–	–	0,3	μs
Data set-up time	$t_{SU;DAT}$	250	–	–	ns
Data hold time	$t_{HD;DAT}$	0	–	–	ns
SCL LOW to data out valid	$t_{VD;DAT}$	–	–	3,4	μs
Stop condition set-up time	$t_{SU;STO}$	4,0	–	–	μs

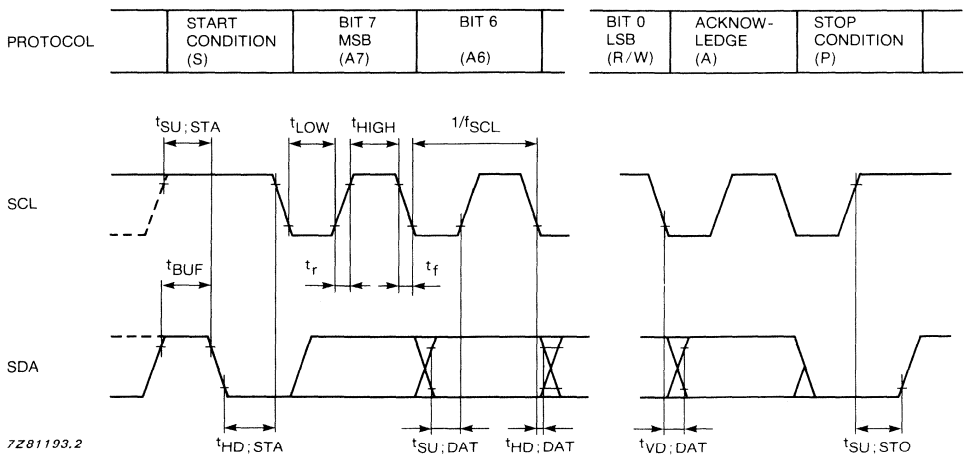


Fig. 7 I^2C bus timing diagram.

Bus protocol

Before any data is transmitted on the I²C bus, the device which should respond is addressed first. The addressing is always done with the first byte transmitted after the start procedure. The I²C bus configuration for different PCF8570/PCF8570C/PCF8571 READ and WRITE cycles is shown in Fig. 8.

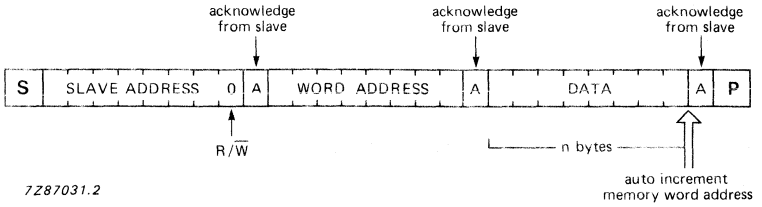


Fig. 8(a) Master transmits to slave receiver (WRITE mode).

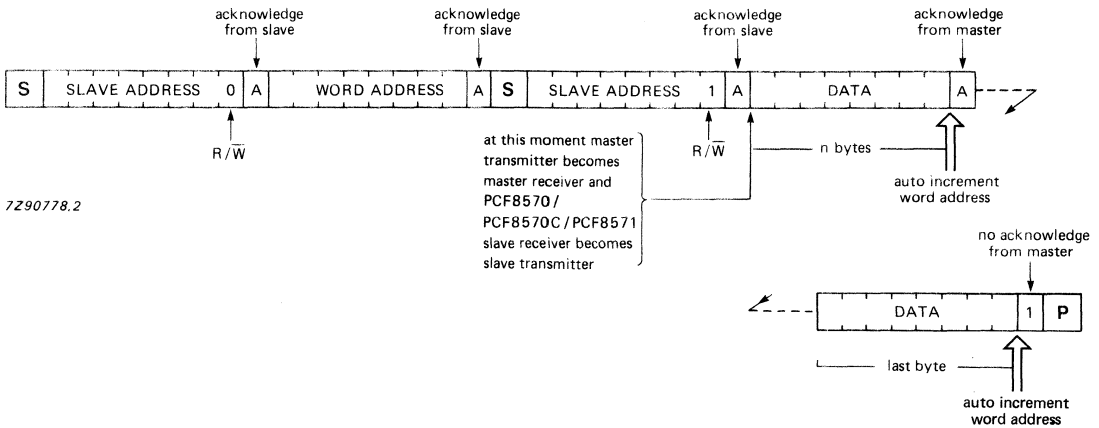


Fig. 8(b) Master reads after setting word address (WRITE word address; READ data).

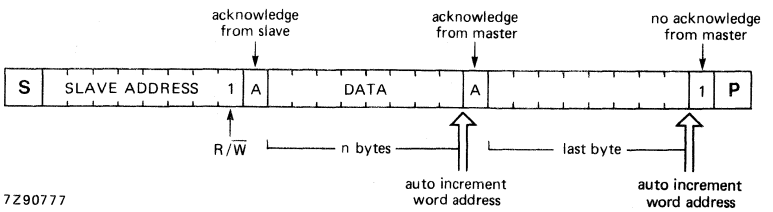


Fig. 8(c) Master reads slave immediately after first byte (READ mode).

APPLICATION INFORMATION

The PCF8570/PCF8571 slave address has a fixed combination 1010 as group 1, while group 2 is fully programmable (see Fig. 9). The PCF8570C has slave address 1011 as group 1, while group 2 is fully programmable (see Fig. 10).

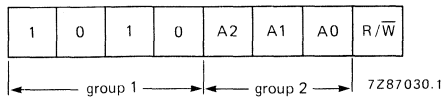


Fig. 9 PCF8570 and PCF8571 address.

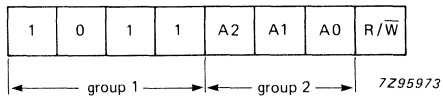


Fig. 10 PCF8570C address.

Note

A0, A1, and A2 inputs must be connected to V_{DD} or V_{SS} but not left open-circuit.

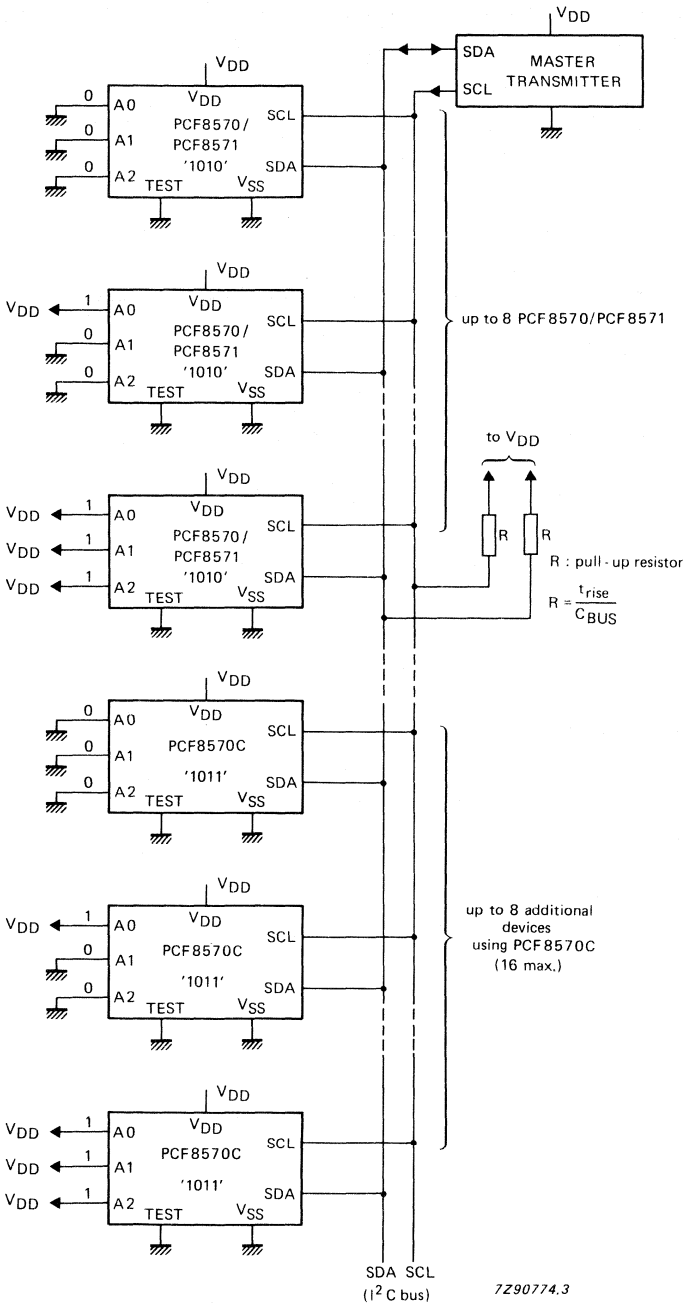
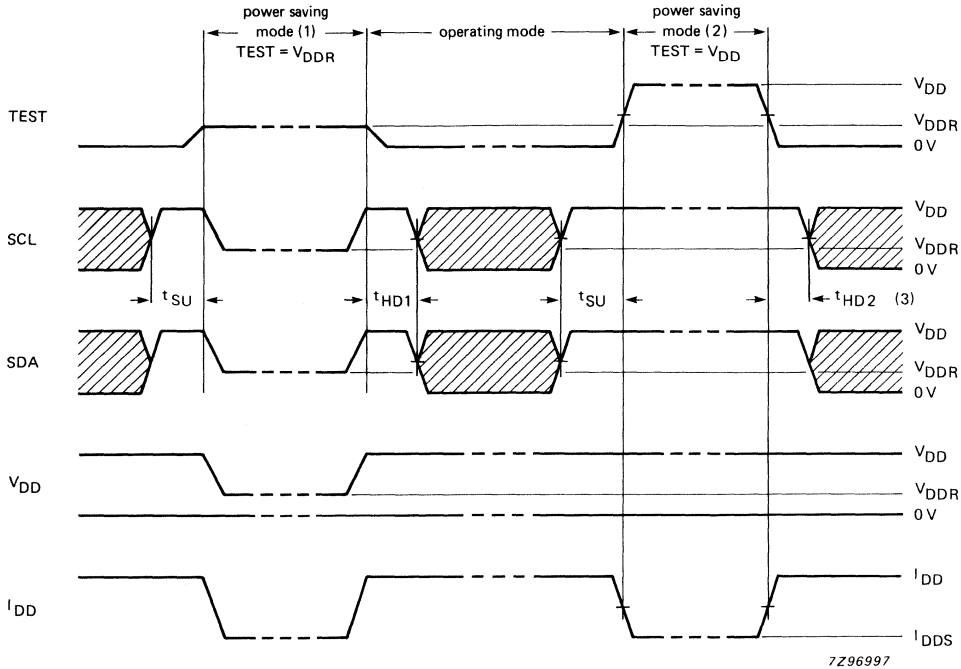


Fig. 11 Application diagram.

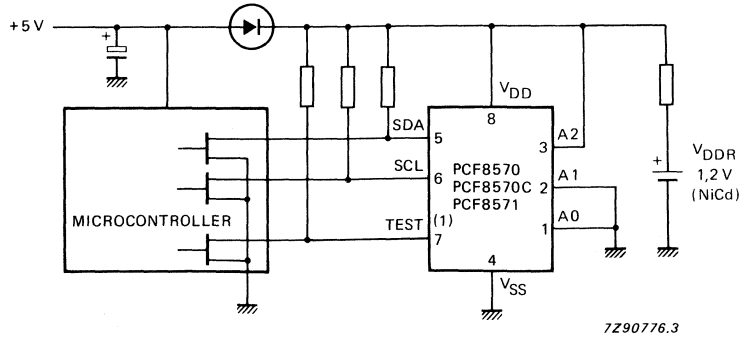
POWER SAVING MODE

With the condition **TEST** = V_{DD} or V_{DDR} the PCF8570/PCF8570C/PCF8571 goes into the power saving mode and I^2C bus logic is reset.



(1) Power saving mode without 5 V supply voltage.
(2) Power saving mode with 5 V supply voltage.
(3) t_{SU} and $t_{HD1} \geqslant 4\ \mu s$ and $t_{HD2} \geqslant 50\ \mu s$.

Fig. 12 Timing for power saving mode.



(1) In the operating mode TEST = 0; In the power saving mode TEST = V_{DDR}.

Fig. 13 Application example for power saving mode.

CLOCK/CALENDAR WITH SERIAL I/O

GENERAL DESCRIPTION

The PCF8573 is a low threshold, monolithic CMOS peripheral circuit that functions as a real time clock/calendar with an Inter IC (I^2C) bus interface.
The device incorporates an addressable time counter and an addressable alarm register for minutes, hours, days and months. Three special control/status flags, COMP, POWF and NODA are also available. Information is transferred via a serial, two-line bidirectional bus (I^2C). Back-up for the clock during supply interruption is provided by a 1.2 V nickel cadmium battery. The time base is generated from a 32,768 kHz crystal controlled oscillator.

Features

- Serial input/output bus (I^2C) interface for minutes, hours, days and months
- Additional pulse outputs for seconds and minutes
- Alarm register for presetting a time for alarm or remote switching functions
- Battery back-up for clock function during supply interruption
- Crystal oscillator control (32,768 kHz)

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage (clock)		$V_{DD}-V_{SS1}$	1,1	--	6,0	V
Supply voltage (I^2C interface)		$V_{DD}-V_{SS2}$	2,5	–	6,0	V
Crystal oscillator		f_{osc}	–	32,768	–	kHz

PACKAGE OUTLINES

PCF8573P: 16-lead DIL; plastic (SOT-38).
PCF8573T: 16-lead mini-pack; plastic (SO-16L; SOT-162A).

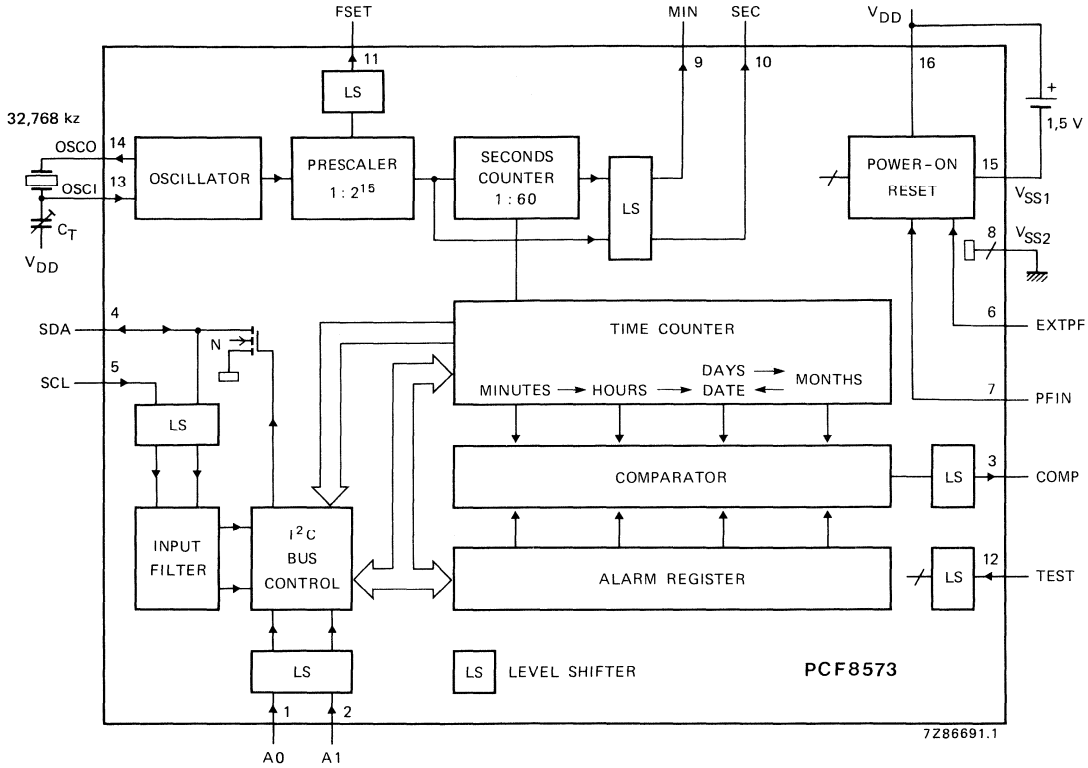


Fig. 1 Block diagram.

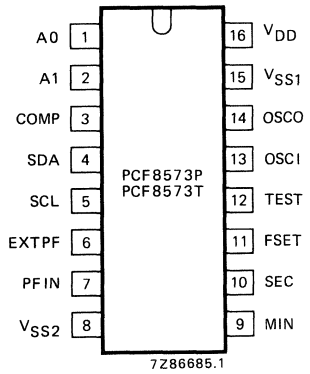


Fig. 2 Pinning diagram.

PINNING

1	A0	address input
2	A1	address input
3	COMP	comparator output
4	SDA	serial data line (I^2C bus)
5	SCL	serial clock line (I^2C bus)
6	EXTPF	enable power fail flag input
7	PFIN	power fail flag input
8	V_{SS2}	negative supply 2 (I^2C interface)
9	MIN	one pulse per minute output
10	SEC	one pulse per second output
11	FSET	oscillator tuning output
12	TEST	test input; must be connected to V_{SS2} when not in use
13	OSCI	oscillator input
14	OSCO	oscillator input/output
15	V_{SS1}	negative supply 1 (clock)
16	V_{DD}	common positive supply

FUNCTIONAL DESCRIPTION

Oscillator

The PCF8573 has an integrated crystal-controlled oscillator which provides the timebase for the prescaler. The frequency is determined by a single 32,768 kHz crystal connected between OSCI and OSCO. A trimmer is connected between OSCI and V_{DD}.

Prescaler and time counter

The prescaler provides a 128 Hz signal at the FSET output for fine adjustment of the crystal oscillator without loading it. The prescaler also generates a pulse once a second to advance the seconds counter. The carry of the prescaler and the seconds counter are available at the outputs SEC, MIN respectively, and are also readable via the I^2C bus. The mark-to-space ratio of both signals is 1 : 1. The time counter is advanced one count by the falling edge of output signal MIN. A transition from HIGH to LOW of output signal SEC triggers MIN to change state. The time counter counts minutes, hours, days and months, and provides a full calendar function which needs to be corrected once every four years. Cycle lengths are shown in Table 1.

Table 1 Cycle length of the time counter

unit	number of bits	counting cycle	carry for following unit	content of month counter
minutes	7	00 to 59	59 → 00	
hours	6	00 to 23	23 → 00	
days	6	01 to 28	28 → 01	2 (note 1)
			or 29 → 01	2 (note 1)
		01 to 30	30 → 01	4, 6, 9, 11
		01 to 31	31 → 01	1, 3, 5, 7, 8, 10, 12
months	5	01 to 12	12 → 01	

Note to Table 1

1. Day counter may be set to 29 by a write transmission with EXECUTE ADDRESS.

Alarm register

The alarm register is a 24-bit memory. It stores the time-point for the next setting of the status flag COMP. Details of writing and reading of the alarm register are included in the description of the characteristics of the I^2C bus.

Comparator

The comparator compares the contents of the alarm register and the time counter, each with a length of 24 bits. When these contents are equal the flag COMP will be set 4 ms after the falling edge of MIN. This set condition occurs once at the beginning of each minute. This information is latched, but can be cleared by an instruction via the I^2C bus. A clear instruction may be transmitted immediately after the flag is set and will be executed. Flag COMP information is also available at the output COMP. The comparison may be based upon hours and minutes only if the internal flag NODA (no date) is set. Flag NODA can be set and cleared by separate instructions via the I^2C bus, but it is undefined until the first set or clear instruction has been received. Both COMP and NODA flags are readable via the I^2C bus.

FUNCTIONAL DESCRIPTION (continued)

Power on/power fail detection

If the voltage $V_{DD}-V_{SS1}$ falls below a certain value the operation of the clock becomes undefined. Thus a warning signal is required to indicate that faultless operation of the clock is not guaranteed. This information is latched in a flag called POWF (Power Fail) and remains latched after restoration of the correct supply voltage until a write procedure with EXECUTE ADDRESS has been received. The flag POWF can be set by an internally generated power fail level-discriminator signal for application with ($V_{DD}-V_{SS1}$) greater than V_{TH1}, or by an externally generated power fail signal for application with ($V_{DD}-V_{SS1}$) less than V_{TH1}. The external signal must be applied to the input PFIN. The input stage operates with signals of any slow rise and fall times. Internally or externally controlled POWF can be selected by input EXTPF as shown in Table 2.

Table 2 Power fail selection

EXTPF	PFIN	function
0	0	power fail is sensed internally
0	1	test mode
1	0	power fail is sensed externally
1	1	no power fail sensed

0 : connected to V_{SS1} (LOW)
1 : connected to V_{DD} (HIGH)

The external power fail control operates by absence of the $V_{DD}-V_{SS2}$ supply. Therefore the input levels applied to PFIN and EXTPF must be within the range of $V_{DD}-V_{SS1}$. A LOW level at PFIN indicates a power fail. POWF is readable via the I^2C bus. A power on reset for the I^2C bus control is generated on-chip when the supply voltage $V_{DD}-V_{SS2}$ is less than V_{TH2}.

Interface level shifters

The level shifters adjust the 5 V operating voltage ($V_{DD}-V_{SS2}$) of the microcontroller to the internal supply voltage ($V_{DD}-V_{SS1}$) of the clock/calendar. The oscillator and counter are not influenced by the $V_{DD}-V_{SS2}$ supply voltage. If the voltage $V_{DD}-V_{SS2}$ is absent ($V_{SS2} = V_{DD}$) the output signal of the level shifter is HIGH because V_{DD} is the common node of the $V_{DD}-V_{SS2}$ and the $V_{DD}-V_{SS1}$ supplies. Because the level shifters invert the input signal, the internal circuit behaves as if a LOW signal is present on the inputs. FSET, SEC, MIN and COMP are CMOS push-pull output stages. The driving capability of these outputs is lost when the supply voltage $V_{DD}-V_{SS2} = 0$.

CHARACTERISTICS OF THE I²C BUS

The I²C bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

Bit transfer (see Fig. 3)

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals.

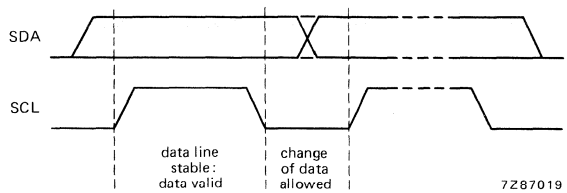


Fig. 3 Bit transfer.

Start and stop conditions (see Fig. 4)

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the stop condition (P).

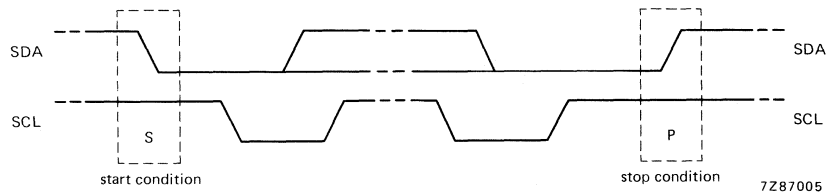


Fig. 4 Definition of start and stop conditions.

System configuration (see Fig. 5)

A device generating a message is a "transmitter", a device receiving a message is the "receiver". The device that controls the message is the "master" and the devices which are controlled by the master are the "slaves".

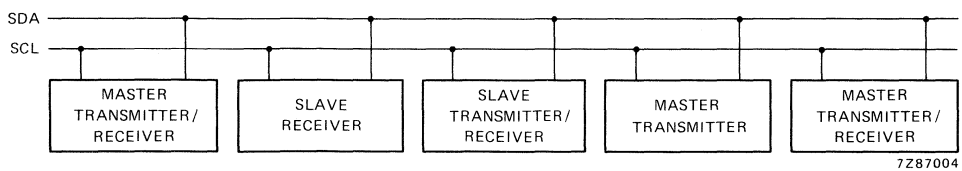


Fig. 5 System configuration.

CHARACTERISTICS OF THE I²C bus (continued)

Acknowledge (see Fig. 6)

The number of data bytes transferred between the start and stop conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter whereas the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse, set up and hold times must be taken into account. A master receiver must signal an end of data to the transmitter by *not* generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition. (See Fig. 11 and Fig. 12.)

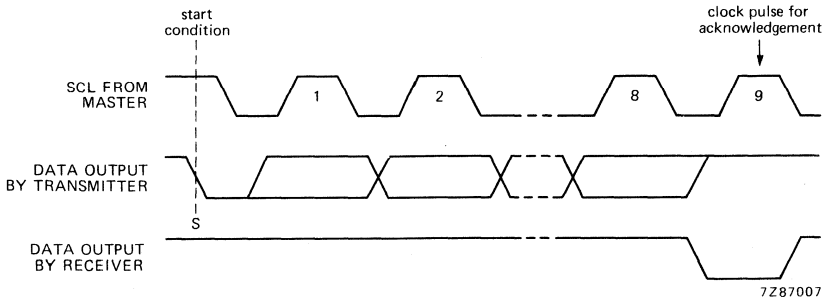


Fig. 6 Acknowledgement on the I²C bus.

Timing specifications

Masters generate a bus clock with a maximum frequency of 100 kHz. Detailed timing is shown in Fig. 7.

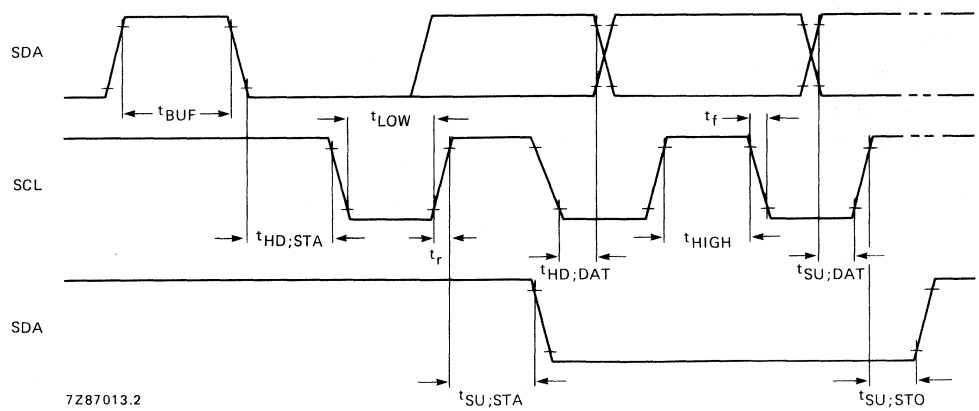


Fig. 7 Timing.

Where:

t_{BUF}	$t \geqslant t_{LOWmin}$	The minimum time the bus must be free before a new transmission can start
$t_{HD;STA}$	$t \geqslant t_{HIGHmin}$	Start condition hold time
t_{LOWmin}	4,7 μs	Clock LOW period
$t_{HIGHmin}$	4 μs	Clock HIGH period
$t_{SU;STA}$	$t \geqslant t_{LOWmin}$	Start condition set-up time, only valid for repeated start code
$t_{HD;DAT}$	$t \geqslant 0$ μs	Data hold time
$t_{SU;DAT}$	$t \geqslant 250$ ns	Data set-up time
t_r	$t \leqslant 1$ μs	Rise time of both the SDA and SCL line
t_f	$t \leqslant 300$ ns	Fall time of both the SDA and SCL line
$t_{SU;STO}$	$t \geqslant t_{LOWmin}$	Stop condition set-up time

Note

All the values refer to V_{IH} and V_{IL} levels with a voltage swing of V_{DD} to V_{SS2}.

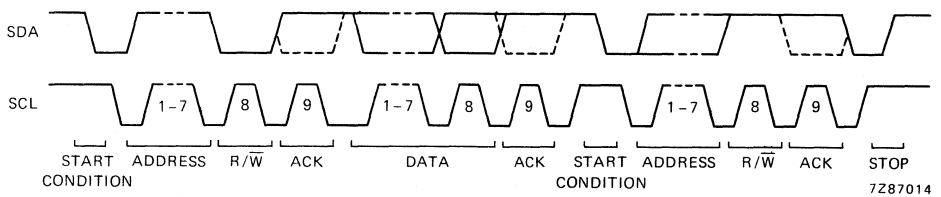


Fig. 8 Complete data transfer.

Where:

Clock t_{LOWmin}	4,7 μs
$t_{HIGHmin}$	4 μs
The dashed line is the acknowledgement of the receiver	
Max. number of bytes	unrestricted
Premature termination of transfer	allowed by generation of STOP condition
Acknowledge clock bit	must be provided by the master

ADDRESSING

Before any data is transmitted on the I²C bus, the device which should respond is addressed first. The addressing is always done with the first byte transmitted after the start procedure.

Slave address

The clock/calendar acts as a slave receiver or slave transmitter. Therefore the clock signal SCL is only an input signal, but the data signal SDA is a bidirectional line. The clock calendar slave address is shown in Fig. 9.

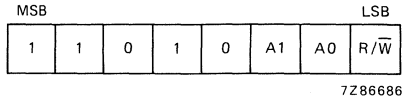


Fig. 9 Slave address.

The subaddress bits A0 and A1 correspond to the two hardware address pins A0 and A1 which allows the device to have 1 of 4 different addresses.

Clock/calendar READ/WRITE cycles

The I²C bus configuration for different clock/calendar READ and WRITE cycles is shown in Fig. 10 and Fig. 11.

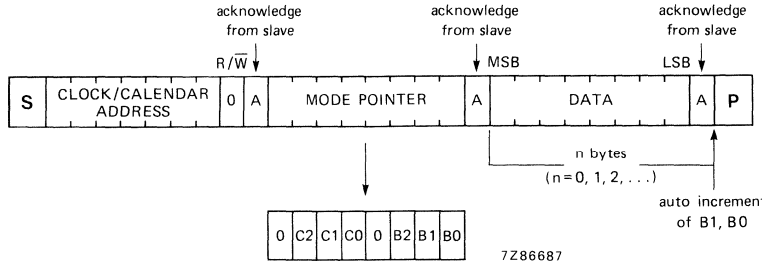


Fig. 10 Master transmitter transmits to clock/calendar slave receiver.

The write cycle is used to set the time counter, the alarm register and the flags. The transmission of the clock/calendar address is followed by the MODE-POINTER-WORD which contains a CONTROL-nibble (Table 3) and an ADDRESS-nibble (Table 4). The ADDRESS-nible is valid only if the preceding CONTROL-nibble is set to EXECUTE ADDRESS. The third transmitted word contains the data to be written into the time counter or alarm register.

Table 3 CONTROL-nibble

	C2	C1	C0	function
0	0	0	0	execute address
0	0	0	1	read control/status flags
0	0	1	0	reset prescaler, including seconds counter; without carry for minute counter
0	0	1	1	time adjust, with carry for minute counter (see note)
0	1	0	0	reset NODA flag
0	1	0	1	set NODA flag
0	1	1	0	reset COMP flag

Note

If the seconds counter is below 30 there is no carry. This causes a time adjustment of max. −30 s. From the count 30 there is a carry which adjusts the time by max. + 30 s.

Table 4 ADDRESS-nibble

	B2	B1	B0	addressed to:
0	0	0	0	time counter hours
0	0	0	1	time counter minutes
0	0	1	0	time counter days
0	0	1	1	time counter months
0	1	0	0	alarm register hours
0	1	0	1	alarm register minutes
0	1	1	0	alarm register days
0	1	1	1	alarm register months

At the end of each data word the address bits B1, B0 will be incremented automatically provided the preceding CONTROL-nibble is set to EXECUTE ADDRESS. There is no carry to B2.

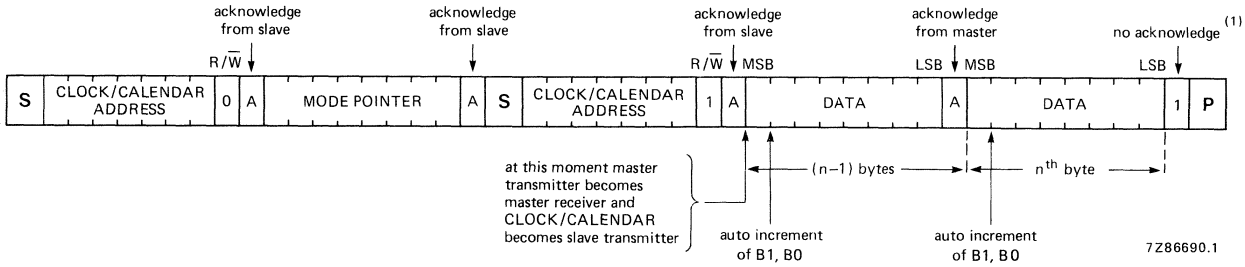
Table 5 shows the placement of the BCD upper and lower digits in the DATA byte for writing into the addressed part of the time counter and alarm register respectively.

Table 5 Placement of BCD digits in the DATA byte

MSB				DATA			LSB	
upper digit				lower digit				
UD	UC	UB	UA	LD	LC	LB	LA	addressed to:
X	X	D	D	D	D	D	D	hours
X	D	D	D	D	D	D	D	minutes
X	X	D	D	D	D	D	D	days
X	X	X	D	D	D	D	D	months

Where:

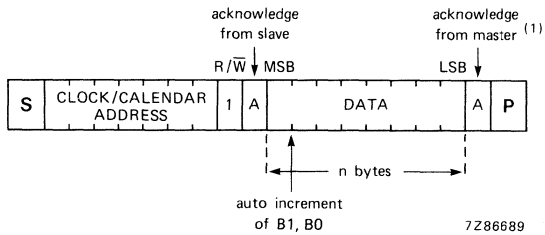
"X" is the don't care bit
"D" is the data bit
Acknowledgement response of the clock calendar as slave receiver is shown in Table 6.



(1) The master receiver must signal an end of data to the slave transmitter by *not* generating an acknowledge on the *last byte* that has been clocked out of the slave.

Fig. 11 Master transmitter reads clock/calendar after setting mode pointer.

To read the addressed part of the time counter and alarm register, plus information from specified control/status flags, the BCD digits in the DATA byte are organized as shown in Table 7.



(1) The master receiver must signal an end of data to the slave transmitter by *not* generating an acknowledge on the *last byte* that has been clocked out of the slave.

Fig. 12 Master reads clock/calendar immediately after first byte.

The status of the MODE-POINTER-WORD concerning the CONTROL-nibble remains unchanged until a write to MODE POINTER condition occurs.

ADDRESSING (continued)

Table 6 Slave receiver acknowledgement

mode pointer								acknowledge on byte		
								address	mode pointer	data
	C2	C1	C0		B2	B1	B0			
0	0	0	0	0	X	X	X	yes	yes	yes
0	0	0	0	1	X	X	X	yes	no	no
0	0	0	1	X	X	X	X	yes	yes	no
0	0	1	0	X	X	X	X	yes	yes	no
0	0	1	1	X	X	X	X	yes	yes	no
0	1	0	0	X	X	X	X	yes	yes	no
0	1	0	1	X	X	X	X	yes	yes	no
0	1	1	0	X	X	X	X	yes	yes	no
0	1	1	1	X	X	X	X	yes	no	no
1	X	X	X	X	X	X	X	yes	no	no

Where:

"X" is the don't care bit.

Table 7 Organization of the BCD digits in the DATA byte

MSB DATA LSB								
upper digit				lower digit				
UD	UC	UB	UA	LD	LC	LB	LA	addressed to
0	0	D	D	D	D	D	D	hours
0	D	D	D	D	D	D	D	minutes
0	0	D	D	D	D	D	D	days
0	0	0	D	D	D	D	D	months
0	0	0	*	**	NODA	COMP	POWF	control/status flags

Where:

"D" is the data bit.

* = minutes.

** = seconds.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	condition	symbol	min.	max.	unit
Supply voltage ranges		$V_{DD}-V_{SS1}$ $V_{DD}-V_{SS2}$	−0,3 −0,3	8 8	V V
Voltage input (pins 4; 5)		V_I	$V_{SS2}-0,8$	$V_{DD}+0,8$	V*
Voltage input (pins 6; 7; 13, 14)		V_I	$V_{SS1}-0,6$	$V_{DD}+0,6$	V
Voltage on any other pin		V_I	$V_{SS2}-0,6$	$V_{DD}+0,6$	V
Input current		I_I	–	10	mA
Output current		I_O	–	10	mA
Power dissipation per output		P_O	–	100	mW
Total power dissipation		P_{tot}	–	200	mW
Operating ambient temperature range		T_{amb}	−40	+85	°C
Storage temperature range		T_{stg}	−55	+125	°C

HANDLING

Inputs and outputs are protected against electrostatic charge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see 'Handling MOS devices').

* Impedance min. 500 Ω.

CHARACTERISTICS

V_{SS2} = 0 V; T_{amb} = −40 to + 85 °C unless otherwise specified. Typical values at T_{amb} = + 25 °C.

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage I^2C interface		$V_{DD}-V_{SS2}$	2,5	5,0	6,0	V
Supply voltage (clock)		$V_{DD}-V_{SS1}$	1,1	1,5	$V_{DD}-V_{SS2}$	V
Supply current V_{SS1}	$V_{DD}-V_{SS1}$ = 1,5 V	$-I_{SS1}$	–	3	10	μA
	$V_{DD}-V_{SS1}$ = 5 V	$-I_{SS1}$	–	12	50	μA
Supply current V_{SS2}	$V_{DD}-V_{SS2}$ = 5 V; (I_O = 0 mA on all outputs)	$-I_{SS2}$	–	–	50	μA
Inputs SCL, SDA, A0, A1, TEST						
Input voltage HIGH		V_{IH}	0,7 x V_{DD}	–	–	V
Input voltage LOW		V_{IL}	–	–	0,3 x V_{DD}	V
Input leakage current	V_I = V_{SS2} to V_{DD}	$\pm I_I$	–	–	1	μA
Inputs EXTPF, PFIN						
Input voltage HIGH		$V_{IH}-V_{SS1}$	0,7 x $V_{DD}-V_{SS1}$	–	–	V
Input voltage LOW		$V_{IL}-V_{SS1}$	0	–	0,3 x $V_{DD}-V_{SS1}$	V
Input leakage current	V_I = V_{SS1} to V_{DD} T_{amb} = 25 °C;	$\pm I_I$	–	–	1,0	μA
	V_I = V_{SS1} to V_{DD}	$\pm I_I$	–	–	0,1	μA

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Outputs SEC, MIN, COMP, FSET (normal buffer outputs)						
Output voltage HIGH	$V_{DD}-V_{SS2}$ = 2,5 V; $-I_O$ = 0,1 mA	V_{OH}	$V_{DD}-0,4$	–	–	V
	$V_{DD}-V_{SS2}$ = 4 to 6 V; $-I_O$ = 0,5 mA	V_{OH}	$V_{DD}-0,4$	–	–	V
Output voltage LOW	$V_{DD}-V_{SS2}$ = 2,5 V; I_O = 0,3 mA	V_{OL}	–	–	0,4	V
	$V_{DD}-V_{SS2}$ = 4 to 6 V; I_O = 1,6 mA	V_{OL}	–	–	0,4	V
Output SDA (n channel open drain)						
Output "ON"	I_O = 3 mA; $V_{DD}-V_{SS2}$ = 2,5 to 6 V	V_{OL}	–	–	0,4	V
Output "OFF" (leakage current)	$V_{DD}-V_{SS2}$ = 6 V; V_O = 6 V	I_O	–	–	1	μA
Internal threshold voltage						
Power failure detection		V_{TH1}	1	1,2	1,4	V
Power "ON" reset	$V_{SCL} = V_{SDA} = V_{DD}$	V_{TH2}	1,5	2,0	2,5	V
Rise and fall times of input signals						
Input EXTPF		t_r, t_f	–	–	1	μs
Input PFIN		t_r, t_f	–	–	∞	μs
Input signals except EXTPF and PFIN between V_{IL} and V_{IH} levels						
rise time		t_r	–	–	1	μs
fall time		t_f	–	–	0,3	μs

parameter	conditions	symbol	min.	typ.	max.	unit
Frequency at SCL	$V_{DD}-V_{SS2}$ = 4 to 6 V					
Pulse width LOW (Fig. 7)		t_{LOW}	4,7	–	–	μs
Pulse width HIGH (Fig. 7)		t_{HIGH}	4	–	–	μs
Noise suppression time constant at SCL and SDA input		T_I	0,25	1	2,5	μs
Input capacitance (SDA; SCL)		C_I	–	–	7	pF
Oscillator						
Integrated oscillator capacitance		C_{OUT}	–	40	–	pF
Oscillator feedback resistance		R_f	–	3	–	MΩ
Oscillator stability	$\Delta(V_{DD}-V_{SS1})$ = 100 mV; at $V_{DD}-V_{SS1}$ = 1,55 V; T_{amb} = 25 °C	f/f_{osc}	–	2×10^{-6}	–	–
Quartz crystal parameters	f = 32,768 kHz					
Series resistance		R_S	–	–	40	kΩ
Parallel capacitance		C_L	–	9	–	pF
Trimmer capacitance		C_T	5	–	25	pF

APPLICATION INFORMATION

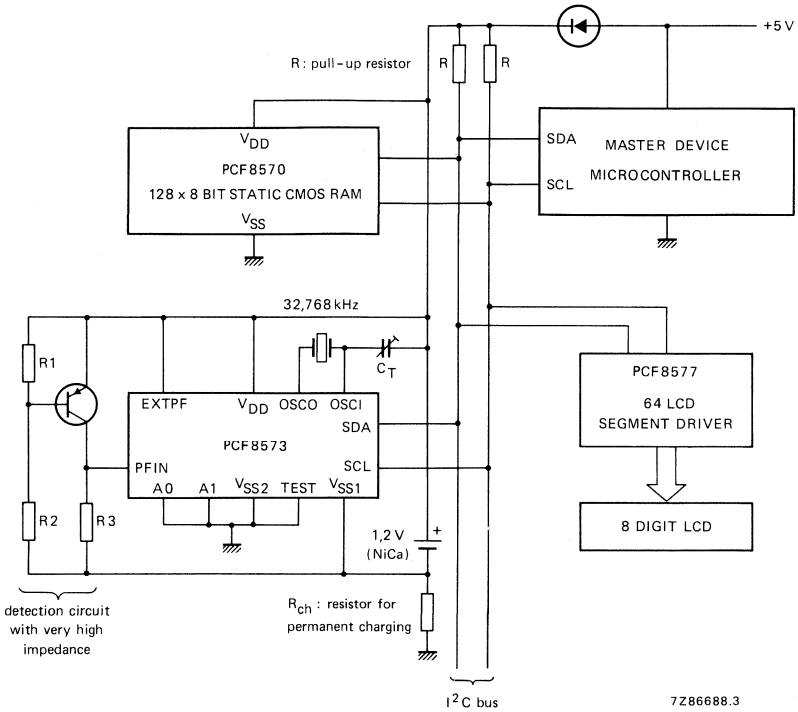


Fig. 13 Application example of the PCF8573 clock/calendar.

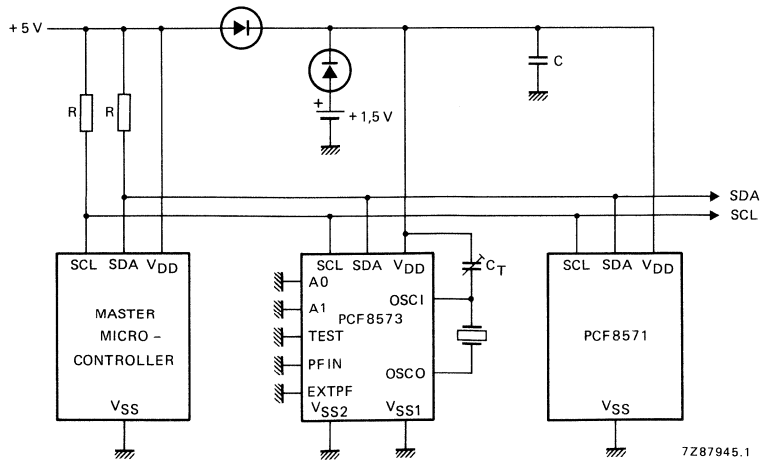


Fig. 14 Application example of the PCF8573 with common V_{SS1} and V_{SS2} supply.

REMOTE 8-BIT I/O EXPANDER FOR I²C BUS

GENERAL DESCRIPTION

The PCF8574 is a single-chip silicon gate CMOS circuit. It provides remote I/O expansion for the MAB8400 and PCF84CXX microcontroller families via the two-line serial bidirectional bus (I²C).
It can also interface microcomputers without a serial interface to the I²C bus (as a slave function only).
The device consists of an 8-bit quasi-bidirectional port and an I²C interface.
The PCF8574 has low current consumption and includes latched outputs with high current drive capability for directly driving LEDs. It also possesses an interrupt line (INT) which is connected to the interrupt logic of the microcomputer on the I²C bus. By sending an interrupt signal on this line, the remote I/O can inform the microcomputer if there is incoming data on its ports without having to communicate via the I²C bus. This means that the PCF8574 can remain a simple slave device.

The PCF8574 and the PCF8574A versions differ only in their slave address as shown in Fig. 10.

Features

- Operating supply voltage 2,5 V to 6 V
- Low stand-by current consumption max. 10 μA
- Bidirectional expander
- Open drain interrupt output
- 8-bit remote I/O port for the I²C bus
- Peripheral for the MAB8400 and PCF84CXX microcontroller families
- Latched outputs with high current drive capability for directly driving LEDs
- Address by 3 hardware address pins for use of up to 8 devices (up to 16 with PCF8574A)

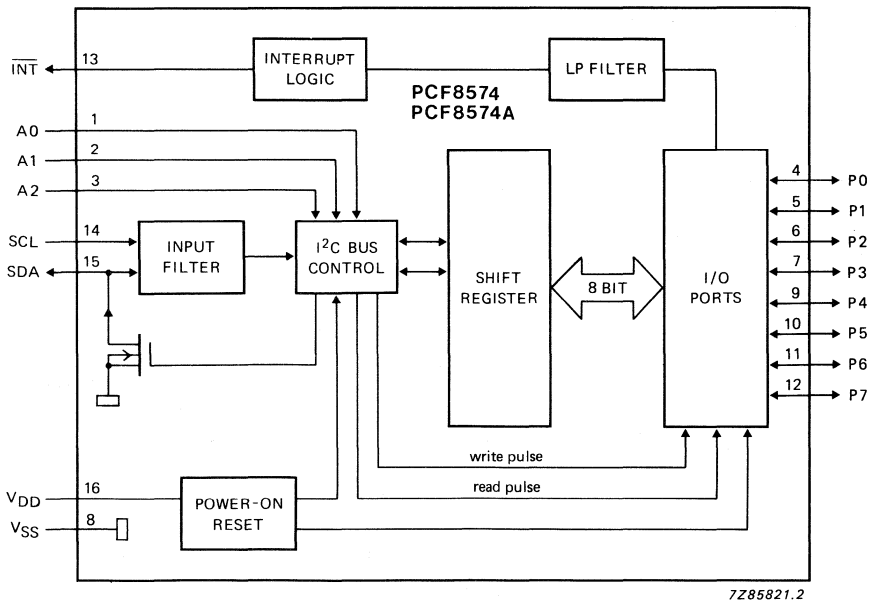


Fig. 1 Block diagram.

PACKAGE OUTLINES

PCF8574P, PCF8574AP: 16-lead DIL; plastic (SOT-38).
PCF8574T, PCF8574AT: 16-lead mini-pack; plastic (SO-16L; SOT-162A).

PINNING

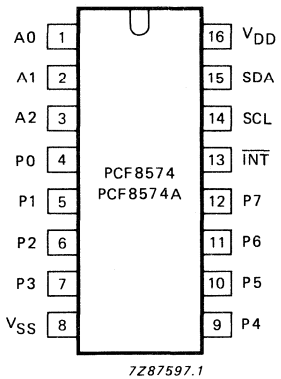


Fig. 2 Pinning diagram.

1 to 3	A0 to A2	address inputs
4 to 7 9 to 12	P0 to P3 P4 to P7	8-bit quasi-bidirectional I/O port
8	V_{SS}	negative supply
13	$\overline{INT}$	interrupt output
14	SCL	serial clock line
15	SDA	serial data line
16	V_{DD}	positive supply

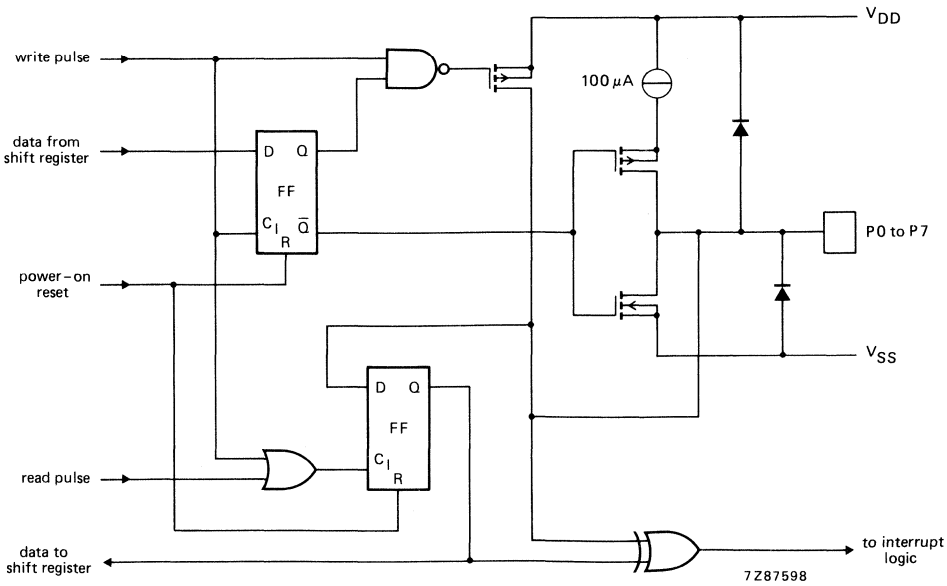


Fig. 3 Simplified schematic diagram of each port.

CHARACTERISTICS OF THE I²C BUS

The I²C bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals.

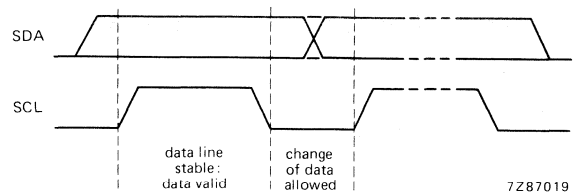


Fig. 4 Bit transfer.

Start and stop conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the stop condition (P).

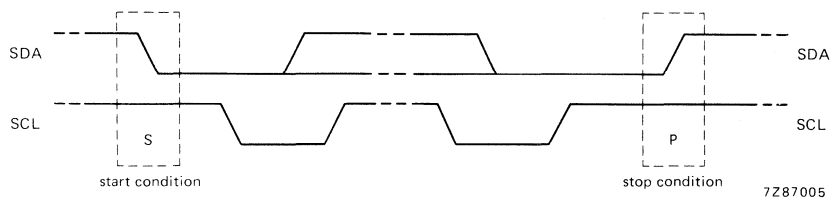


Fig. 5 Definition of start and stop conditions.

System configuration

A device generating a message is a "transmitter", a device receiving a message is the "receiver". The device that controls the message is the "master" and the devices which are controlled by the master are the "slaves".

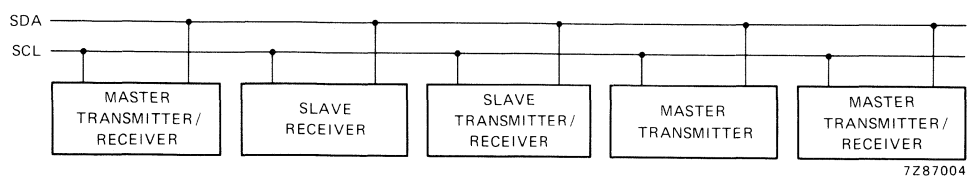


Fig. 6 System configuration.

CHARACTERISTICS OF THE I²C BUS (continued)

Acknowledge

The number of data bytes transferred between the start and stop conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter whereas the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse, set up and hold times must be taken into account. A master receiver must signal an end of data to the transmitter by *not* generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

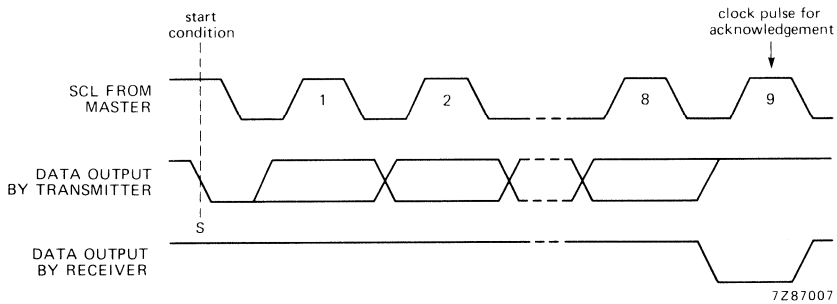


Fig. 7 Acknowledgement on the I²C bus.

Timing specifications

Masters generate a bus clock with a maximum frequency of 100 kHz. Detailed timing is shown in Fig. 8.

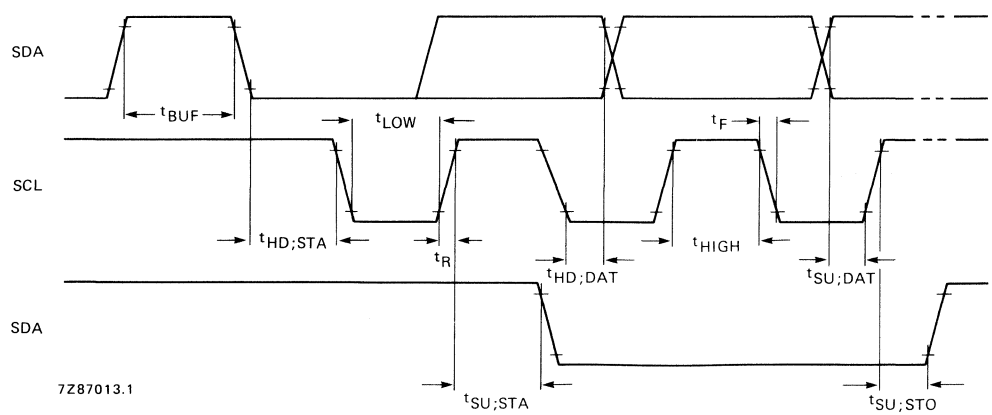


Fig. 8 I²C bus timing.

Where:

t_{BUF}	$t \geqslant t_{LOWmin}$	The minimum time the bus must be free before a new transmission can start
$t_{HD;STA}$	$t \geqslant t_{HIGHmin}$	Start condition hold time
t_{LOWmin}	4,7 μs	Clock LOW period
$t_{HIGHmin}$	4 μs	Clock HIGH period
$t_{SU;STA}$	$t \geqslant t_{LOWmin}$	Start condition set-up time, only valid for repeated start code
$t_{HD;DAT}$	$t \geqslant 0$ μs	Data hold time
$t_{SU;DAT}$	$t \geqslant 250$ ns	Data set-up time
t_R	$t \leqslant 1$ μs	Rise time of both the SDA and SCL line
t_F	$t \leqslant 300$ ns	Fall time of both the SDA and SCL line
$t_{SU;STO}$	$t \geqslant t_{LOWmin}$	Stop condition set-up time

Note

All the values refer to V_{IH} and V_{IL} levels with a voltage swing of V_{SS} to V_{DD}.

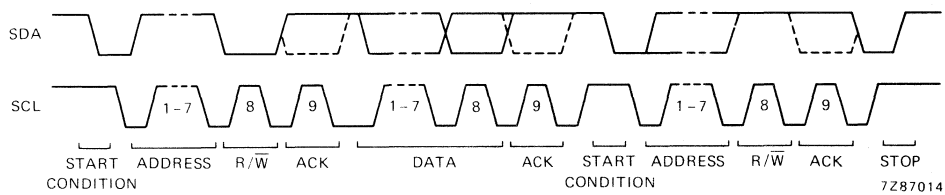


Fig. 9 Complete data transfer.

Where:

Clock t_{LOWmin} 4,7 μs

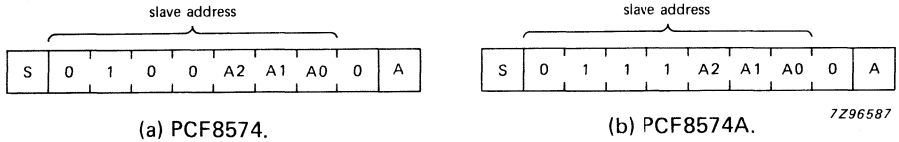
$t_{HIGHmin}$ 4 μs

The dashed line is the acknowledgement of the receiver

Max. number of bytes	unrestricted
Premature termination of transfer	allowed by generation of STOP condition
Acknowledge clock bit	must be provided by the master

FUNCTIONAL DESCRIPTION

Addressing (see Figs 10, 11 and 12)



(a) PCF8574. (b) PCF8574A.

Fig. 10 PCF8574 and PCF8574A slave addresses.

Each bit of the PCF8574 I/O port can be independently used as an input or an output. Input data is transferred from the port to the microcomputer by the READ mode. Output data is transmitted to the port by the WRITE mode.

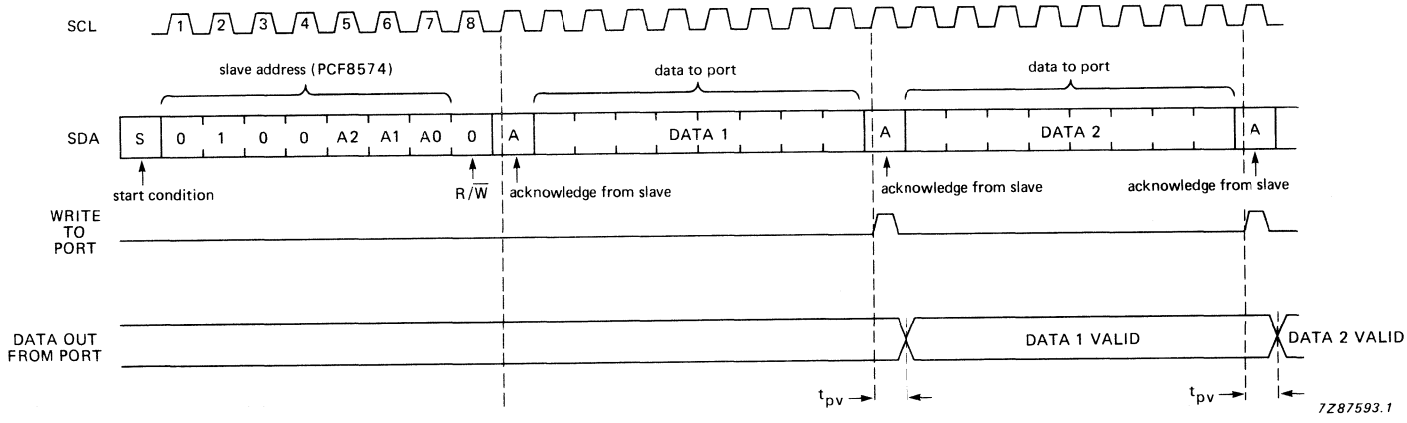


Fig. 11 WRITE mode (output port).

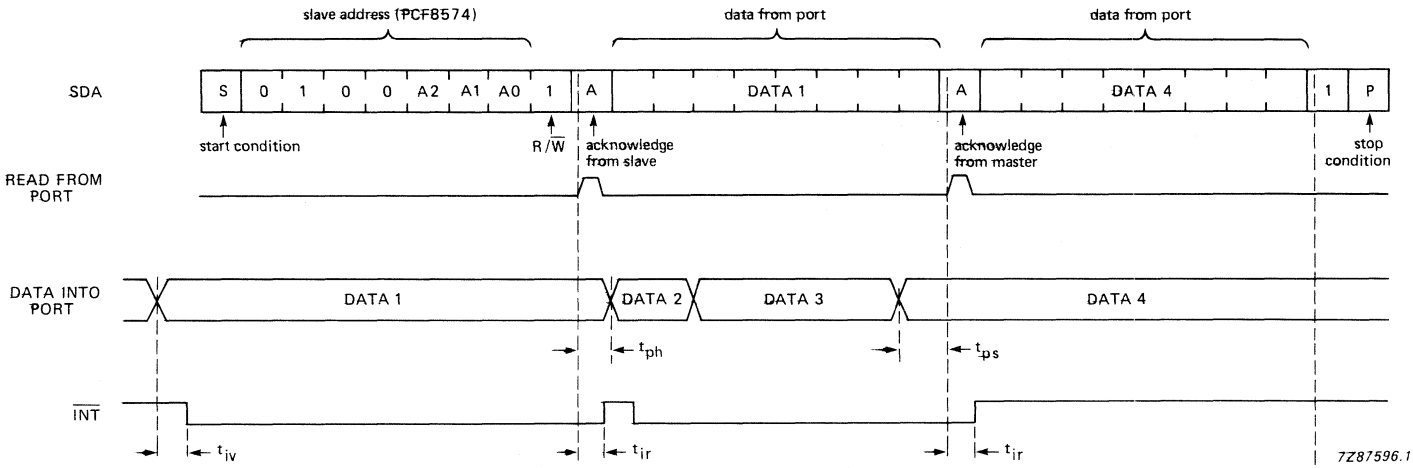


Fig. 12 READ mode (input port).

Note

A LOW-to-HIGH transition of SDA, while SCL is HIGH is defined as the stop condition (P). Transfer of data can be stopped at any moment by a stop condition. When this occurs, data present at the last acknowledge phase is valid (output mode). Input data is lost.

Interrupt (see Figs 13 and 14)

The PCF8574/PCF8574A provides an open drain output ($\overline{INT}$) which can be fed to a corresponding input of the microcomputer. This gives these chips a type of master function which can initiate an action elsewhere in the system.

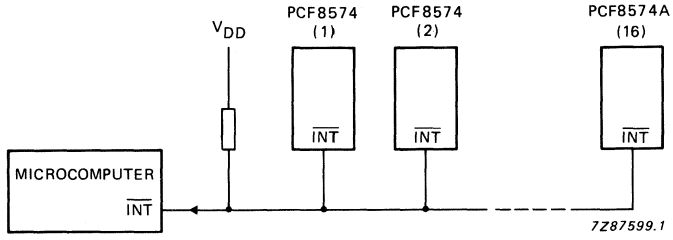


Fig. 13 Application of multiple PCF8574s with interrupt.

An interrupt is generated by any rising or falling edge of the port inputs in the input mode. After time t_{iv} the signal $\overline{INT}$ is valid.
Resetting and reactivating the interrupt circuit is achieved when data on the port is changed to the original setting or data is read from or written to the port which has generated the interrupt.
Resetting occurs as follows:

- In the READ mode at the acknowledge bit after the rising edge of the SCL signal.
- In the WRITE mode at the acknowledge bit after the HIGH to LOW transition of the SCL signal.

Each change of the ports after the resettings will be detected and after the next rising clock edge, will be transmitted as $\overline{INT}$.
Reading from or writing to another device does not affect the interrupt circuit.

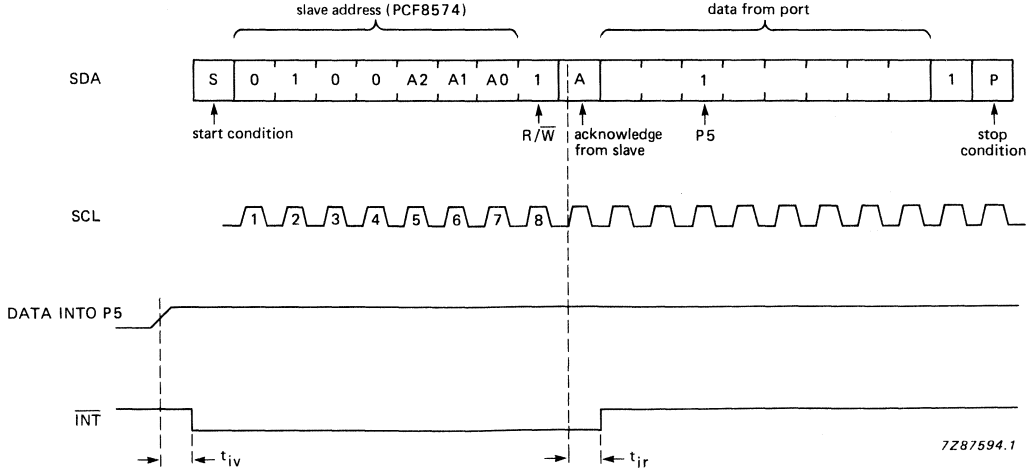


Fig. 14 Interrupt generated by a change of input to port P5.

FUNCTIONAL DESCRIPTION (continued)

Quasi-bidirectional I/O ports (see Fig. 15)

A quasi-bidirectional port can be used as an input or output without the use of a control signal for data direction. The bit designated as an input must first be loaded with a logic 1. In this mode only a current source to V_{DD} is active. An additional strong pull-up to V_{DD} allows fast rising edges into heavily loaded outputs. These devices turn on when an output changes from LOW to HIGH, and are switched off by the negative edge of SCL. SCL should not remain HIGH when a short-circuit to V_{SS} is allowed (input mode).

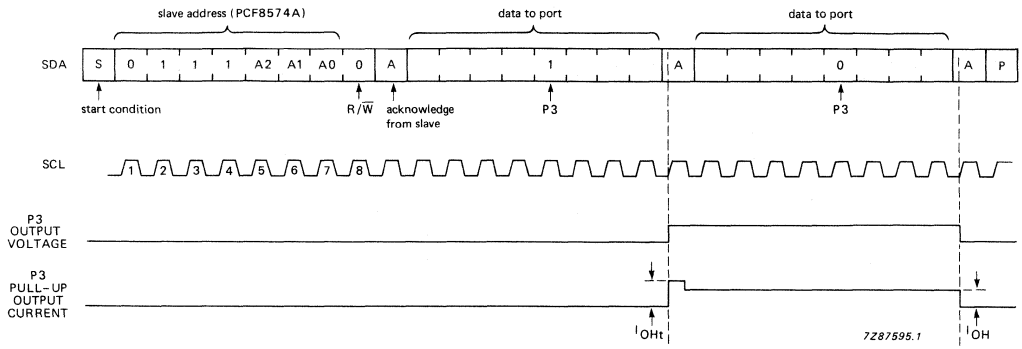


Fig. 15 Transient pull-up current I_{OHt} while P3 changes from LOW-to-HIGH and back to LOW.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range	V_{DD}		−0,5 to + 7	V
Input voltage range (any pin)	V_I		V_{SS}−0,5 to V_{DD} + 0,5	V
D.C. current into any input	$\pm I_I$	max.	20	mA
D.C. current into any output	$\pm I_O$	max.	25	mA
V_{DD} or V_{SS} current	$\pm I_{DD}$; I_{SS}	max.	100	mA
Total power dissipation	P_{tot}	max.	400	mW
Power dissipation per output	P_o	max.	100	mW
Storage temperature range	T_{stg}		−65 to + 150	°C
Operating ambient temperature range	T_{amb}		−40 to + 85	°C

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see 'Handling MOS Devices').

CHARACTERISTICS

V_{DD} = 2,5 to 6 V; V_{SS} = 0 V; T_{amb} = −40 to + 85 °C unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply (pin 16)					
Supply voltage	V_{DD}	2,5	–	6	V
Supply current					
at V_{DD} = 6 V; no load, inputs at V_{DD}, V_{SS}					
operating; (SCL = 100 kHz)	I_{DD}	–	40	100	μA
standby	I_{DDO}	–	1,5	10	μA
Power-on reset voltage level (note 1)	V_{REF}	–	1,3	2,4	V
Input SCL; input/output SDA (pins 14; 15)					
Input voltage LOW	V_{IL}	−0,5 V	–	$0,3V_{DD}$	V
Input voltage HIGH	V_{IH}	$0,7V_{DD}$	–	V_{DD} + 0,5 V	V
Output current LOW					
at V_{OL} = 0,4 V	I_{OL}	3	–	–	mA
Input/Output leakage current	$\|I_L\|$	–	–	100	nA
Clock frequency (see Fig. 8)	f_{SCL}	–	–	100	kHz
Tolerable spike width					
at SCL and SDA input	t_s	–	–	100	ns
Input capacitance (SCL, SDA)					
at $V_I = V_{SS}$	C_I	–	–	7	pF
I/O ports (pins 4 to 7; 9 to 12)					
Input voltage LOW	V_{IL}	−0,5 V	–	$0,3V_{DD}$	V
Input voltage HIGH	V_{IH}	$0,7V_{DD}$	–	V_{DD} + 0,5 V	V
Maximum allowed input current through protection diode					
at $V_I \geqslant V_{DD}$ or $\leqslant V_{SS}$	$\pm I_{IHL}$	–	–	400	μA
Output current LOW					
at V_{OL} = 1 V; V_{DD} = 5 V	I_{OL}	10	30	–	mA
Output current HIGH					
at $V_{OH} = V_{SS}$ (current source only)	$-I_{OH}$	30	100	300	μA
Transient pull-up current HIGH during acknowledge (see Fig. 16)					
at $V_{OH} = V_{SS}$	$-I_{OHt}$	–	0,5	–	mA
Input/Output capacitance	$C_{I/O}$	–	–	10	pF
Port timing; $C_L \leqslant 100$ pF (see Figs 12 and 13)					
Output data valid	t_{pv}	–	–	4	μs
Input data set-up	t_{ps}	0	–	–	μs
Input data hold	t_{ph}	4	–	–	μs

parameter	symbol	min.	typ.	max.	unit
Interrupt $\overline{INT}$ (pin 13)					
Output current LOW at V_{OL} = 0,4 V	I_{OL}	1,6	–	–	mA
Output current HIGH at $V_{OH} = V_{DD}$	$\|I_{OH}\|$	–	–	100	nA
$\overline{INT}$ timing; $C_L \leqslant 100$ pF (see Fig. 13)					
Input data valid	t_{iv}	–	–	4	μs
Reset delay	t_{ir}	–	–	4	μs
Select inputs A0, A1, A2 (pins 1 to 3)					
Input voltage LOW	V_{IH}	−0,5 V	–	$0{,}3V_{DD}$	V
Input voltage HIGH	V_{IH}	$0{,}7V_{DD}$	–	V_{DD} + 0,5 V	V
Input leakage current at $V_I = V_{DD}$ or V_{SS}	$\|I_L\|$	–	–	100	nA

Note 1

The power-on reset circuit resets the I²C bus logic with $V_{DD} < V_{REF}$ and sets all ports to logic 1 (input mode with current source to V_{DD}).

FOR DETAILED INFORMATION SEE RELEVANT DATA BOOK OR DATA SHEET

UNIVERSAL LCD DRIVER FOR LOW MULTIPLEX RATES

GENERAL DESCRIPTION

The PCF8576 is a peripheral device which interfaces to almost any liquid crystal display (LCD) having low multiplex rates. It generates the drive signals for any static or multiplexed LCD containing up to four backplanes and up to 40 segments and can easily be cascaded for larger LCD applications. The PCF8576 is compatible with most microprocessors/microcontrollers and communicates via a two-line bidirectional bus (I^2C). Communication overheads are minimized by a display RAM with auto-incremented addressing, by hardware subaddressing and by display memory switching (static and duplex drive modes).

Features

- Single-chip LCD controller/driver
- Selectable backplane drive configuration: static or 2/3/4 backplane multiplexing
- Selectable display bias configuration: static, 1/2 or 1/3
- Internal LCD bias generation with voltage-follower buffers
- 40 segment drives: up to twenty 8-segment numeric characters; up to ten 15-segment alphanumeric characters; or any graphics of up to 160 elements
- 40 x 4-bit RAM for display data storage
- Auto-incremented display data loading across device subaddress boundaries
- Display memory bank switching in static and duplex drive modes
- Versatile blinking modes
- LCD and logic supplies may be separated
- Wide power supply range: from 2 V for low-threshold LCDs and up to 9 V for guest-host LCDs and high-threshold (automobile) twisted nematic LCDs
- Low power consumption
- Power-saving mode for extremely low power consumption in battery-operated and telephone applications
- I^2C bus interface
- TTL/CMOS compatible
- Compatible with any 4-bit, 8-bit or 16-bit microprocessors/microcontrollers
- May be cascaded for large LCD applications (up to 2560 segments possible)
- Cascadable with the 24 segment LCD driver PCF8566
- Optimized pinning for single plane wiring in both single and multiple PCF8576 applications
- Space-saving 56-lead plastic mini-pack (VSO-56)
- Very low external component count (at most one resistor, even in multiple device applications)
- Compatible with chip-on-glass technology
- Manufactured in silicon gate CMOS process

PACKAGE OUTLINES

PCF8576T: 56-lead mini-pack; plastic (VSO-56; SOT-190).
PCF8576U: uncased chip in tray
PCF8576U/10: chip-on-film frame carrier (FFC)

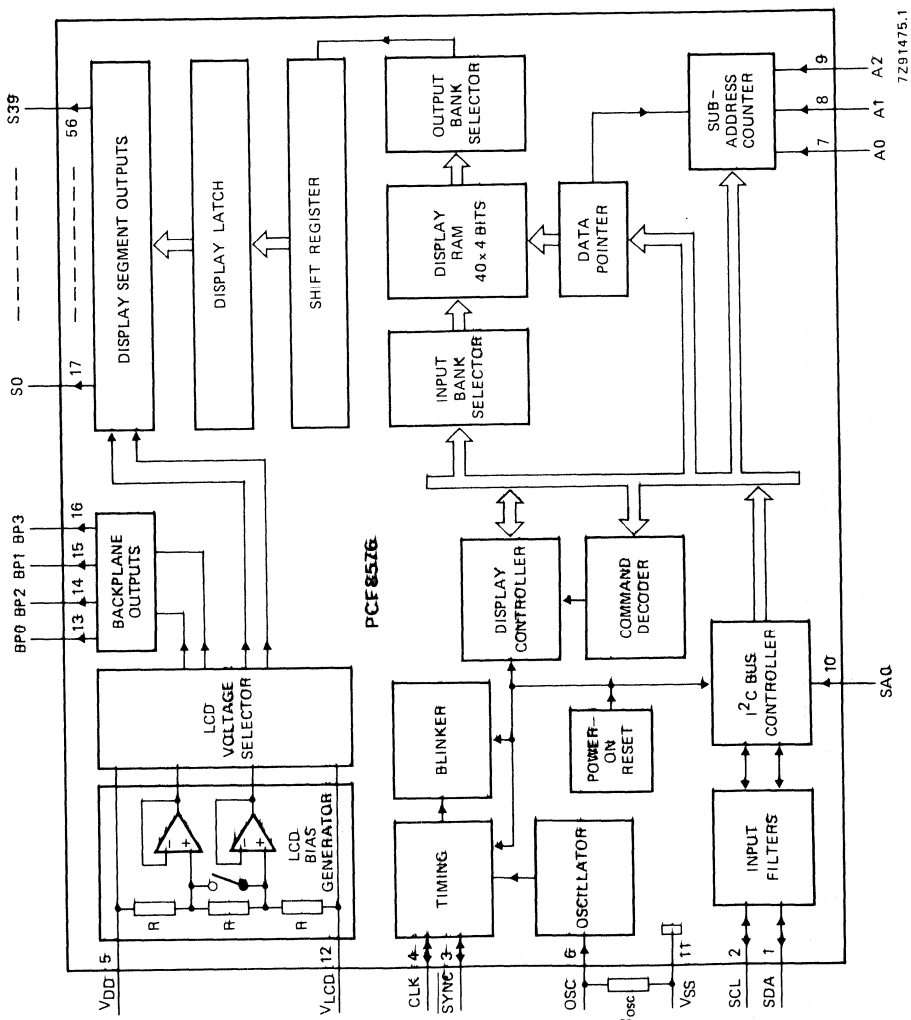


Fig. 1 Block diagram.

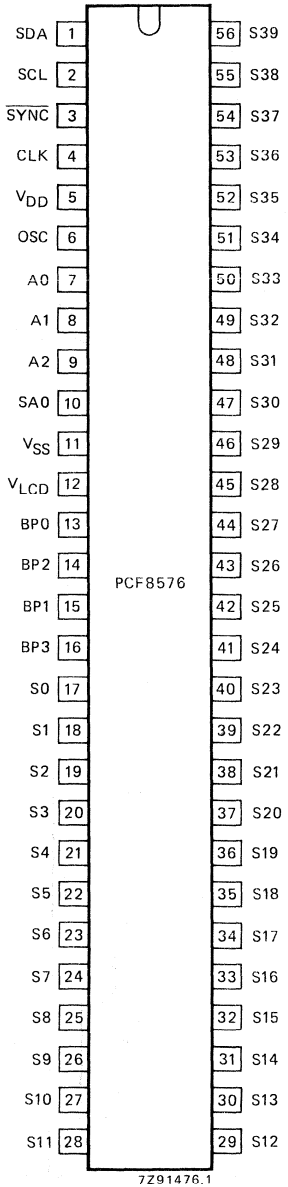


Fig. 2 Pinning diagram.

PINNING

1	SDA	I^2C bus data input/output
2	SCL	I^2C bus clock input/output
3	$\overline{SYNC}$	cascade synchronization input/output
4	CLK	external clock input/output
5	V_{DD}	positive supply voltage
6	OSC	oscillator input
7	A0	I^2C bus subaddress inputs
8	A1	
9	A2	
10	SA0	I^2C bus slave address bit 0 input
11	V_{SS}	logic ground
12	V_{LCD}	LCD supply voltage
13	BP0	LCD backplane outputs
14	BP2	
15	BP1	
16	BP3	
17 to 56	S0 to S39	LCD segment outputs

FUNCTIONAL DESCRIPTION

The PCF8576 is a versatile peripheral device designed to interface any microprocessor/microcontroller to a wide variety of LCDs. It can directly drive any static or multiplexed LCD containing up to four backplanes and up to 40 segments. The display configurations possible with the PCF8576 depend on the number of active backplane outputs required; a selection of display configurations is given in Table 1.

Table 1 Selection of display configurations

active backplane outputs	no. of segments	7-segment numeric	14-segment alphanumeric	dot matrix
4	160	20 digits + 20 indicator symbols	10 characters + 20 indicator symbols	160 dots (4 x 40)
3	120	15 digits + 15 indicator symbols	8 characters + 8 indicator symbols	120 dots (3 x 40)
2	80	10 digits + 10 indicator symbols	5 characters + 10 indicator symbols	80 dots (2 x 40)
1	40	5 digits + 5 indicator symbols	2 characters + 12 indicator symbols	40 dots

All of the display configurations given in Table 1 can be implemented in the typical system shown in Fig. 3. The host microprocessor/microcontroller maintains the 2-line I²C bus communication channel with the PCF8576. A resistor connected between OSC (pin 6) and V_{SS} (pin 11) controls the device clock frequency. The appropiate biasing voltages for the multiplexed LCD waveforms are generated internally. The only other connections required to complete the system are to the power supplies (V_{DD}, V_{SS} and V_{LCD}) and to the LCD panel chosen for the application.

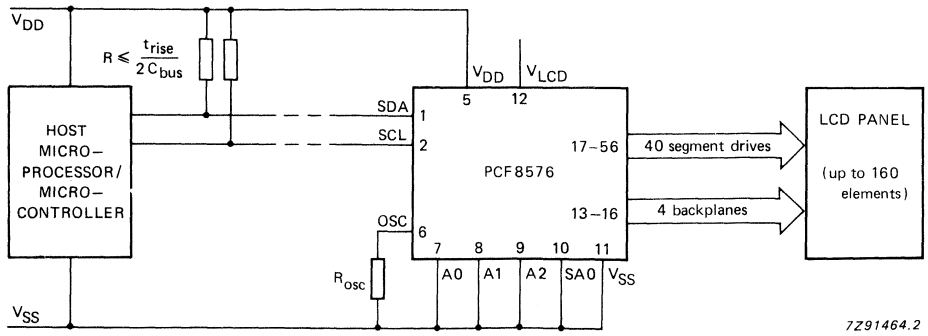


Fig. 3 Typical system configuration.

Power-on reset

At power-on the PCF8576 resets to a defined starting condition as follows:

1. All backplane outputs are set to V_{DD}.
2. All segment outputs are set to V_{DD}.
3. The drive mode '1 : 4 multiplex with 1/3 bias' is selected.
4. Blinking is switched off.
5. Input and output bank selectors are reset (as defined in Table 5).
6. The I^2C bus interface is initialized.
7. The data pointer and the subaddress counter are cleared.

Data transfers on the I^2C bus should be avoided for 1 ms following power-on to allow completion of the reset action.

LCD bias generator

The full-scale LCD voltage (V_{op}) is obtained from $V_{DD} - V_{LCD}$. The LCD voltage may be temperature compensated externally through the V_{LCD} supply to pin 12. Fractional LCD biasing voltages are obtained from an internal voltage divider of three series resistors connected between V_{DD} and V_{LCD}. The centre resistor can be switched out of circuit to provide a ½ bias voltage level for the 1 : 2 multiplex configuration.

LCD voltage selector

The LCD voltage selector coordinates the multiplexing of the LCD according to the selected LCD drive configuration. The operation of the voltage selector is controlled by MODE SET commands from the command decoder. The biasing configurations that apply to the preferred modes of operation, together with the biasing characteristics as functions of $V_{op} = V_{DD} - V_{LCD}$ and the resulting discrimination ratios (D), are given in Table 2.

Table 2 Preferred LCD drive modes: summary of characteristics

LCD drive mode	LCD bias configuration	$\frac{V_{off(rms)}}{V_{op}}$	$\frac{V_{on\ (rms)}}{V_{op}}$	$D = \frac{V_{on(rms)}}{V_{off(rms)}}$
static (1 BP)	static (2 levels)	0	1	∞
1 : 2 MUX (2 BP)	1/2 (3 levels)	$\sqrt{2}/4 = 0{,}354$	$\sqrt{10}/4 = 0{,}791$	$\sqrt{5} = 2{,}236$
1 : 2 MUX (2 BP)	1/3 (4 levels)	$1/3 = 0{,}333$	$\sqrt{5}/3 = 0{,}745$	$\sqrt{5} = 2{,}236$
1 : 3 MUX (3 BP)	1/3 (4 levels)	$1/3 = 0{,}333$	$\sqrt{33}/9 = 0{,}638$	$\sqrt{33}/3 = 1{,}915$
1 : 4 MUX (4 BP)	1/3 (4 levels)	$1/3 = 0{,}333$	$\sqrt{3}/3 = 0{,}577$	$\sqrt{3} = 1{,}732$

LCD voltage selector (continued)

A practical value for V_{op} is determined by equating $V_{off(rms)}$ with a defined LCD threshold voltage (V_{th}), typically when the LCD exhibits approximately 10% contrast. In the static drive mode a suitable choice is $V_{op} \gtrapprox 3\,V_{th}$.
Multiplex drive ratios of 1 : 3 and 1 : 4 with 1/2 bias are possible but the discrimination and hence the contrast ratios are smaller ($\sqrt{3} = 1{,}732$ for 1 : 3 multiplex or $\sqrt{21}/3 = 1{,}528$ for 1 : 4 multiplex).
The advantage of these modes is a reduction of the LCD full scale voltage V_{op} as follows:

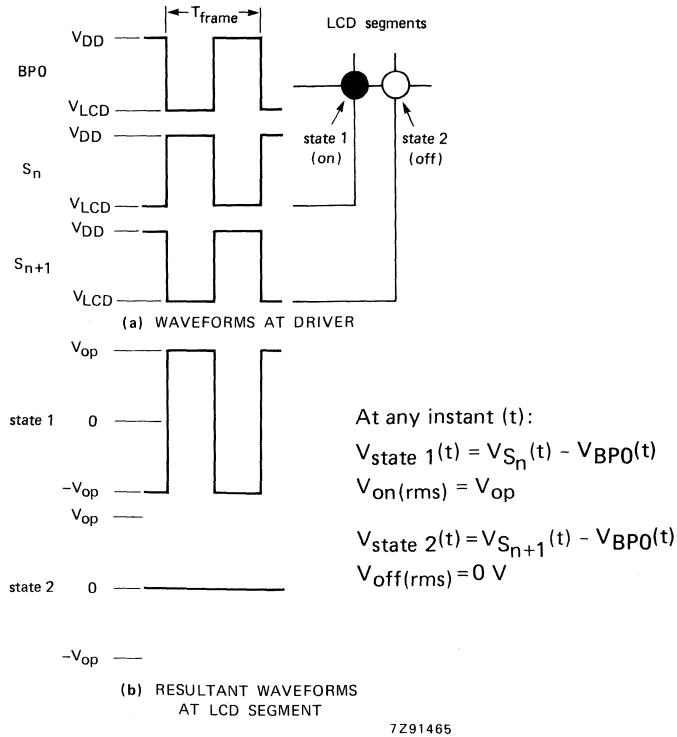
1 : 3 multiplex (1/2 bias) : $V_{op} = \sqrt{6}\,V_{off(rms)} = 2{,}449\,V_{off(rms)}$

1 : 4 multiplex (1/2 bias) : $V_{op} = 4\sqrt{3}/3\,V_{off(rms)} = 2{,}309\,V_{off(rms)}$

These compare with $V_{op} = 3\,V_{off(rms)}$ when 1/3 bias is used.

LCD drive mode waveforms

The static LCD drive mode is used when a single backplane is provided in the LCD. Backplane and segment drive waveforms for this mode are shown in Fig. 4.



At any instant (t):

$V_{state\ 1}(t) = V_{S_n}(t) - V_{BP0}(t)$

$V_{on(rms)} = V_{op}$

$V_{state\ 2}(t) = V_{S_{n+1}}(t) - V_{BP0}(t)$

$V_{off(rms)} = 0\ V$

Fig. 4 Static drive mode waveforms: $V_{op} = V_{DD} - V_{LCD}$.

When two backplanes are provided in the LCD the 1 : 2 multiplex drive mode applies. The PCF8576 allows use of 1/2 or 1/3 bias in this mode as shown in Figs 5 and 6.

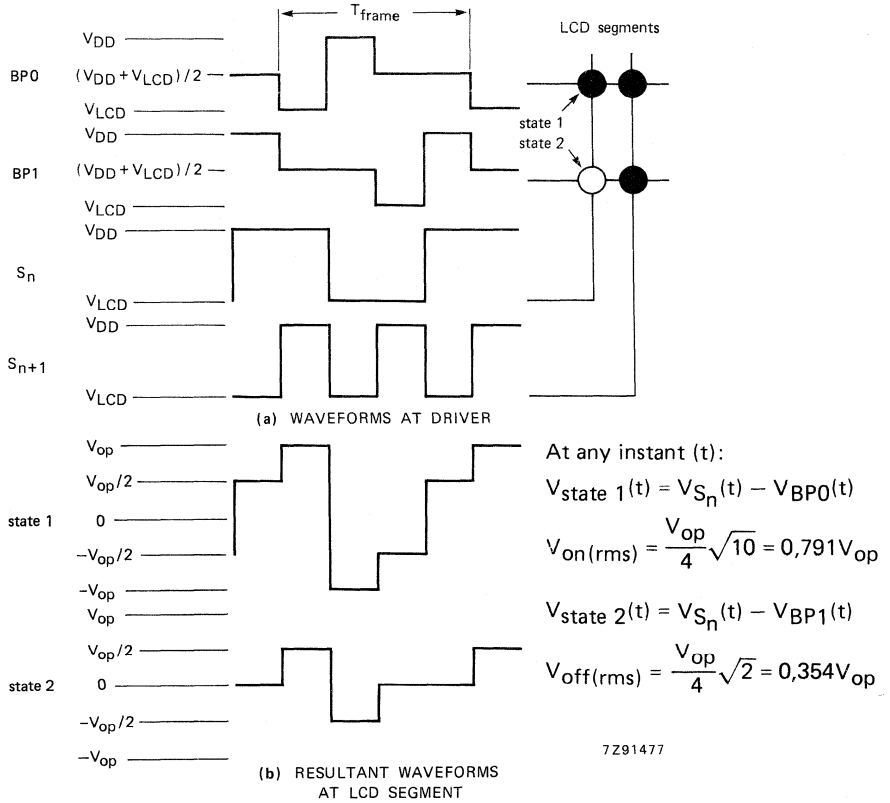


Fig. 5 Waveforms for 1 : 2 multiplex drive mode with 1/2 bias: $V_{op} = V_{DD} - V_{LCD}$.

LCD drive mode waveforms (continued)

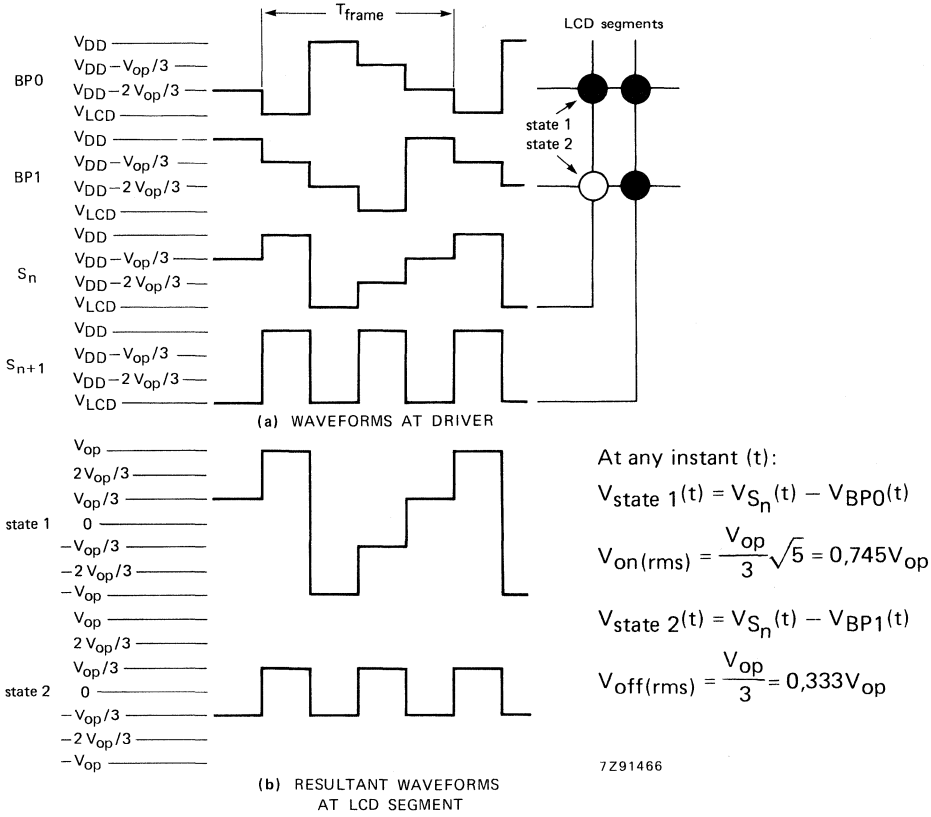


Fig. 6 Waveforms for 1 : 2 multiplex drive mode with 1/3 bias: $V_{op} = V_{DD} - V_{LCD}$.

The backplane and segment drive waveform for the 1 : 3 multiplex drive mode (three LCD backplanes) and for the 1 : 4 multiplex drive mode (four LCD backplanes) are shown in Figs 7 and 8 respectively.

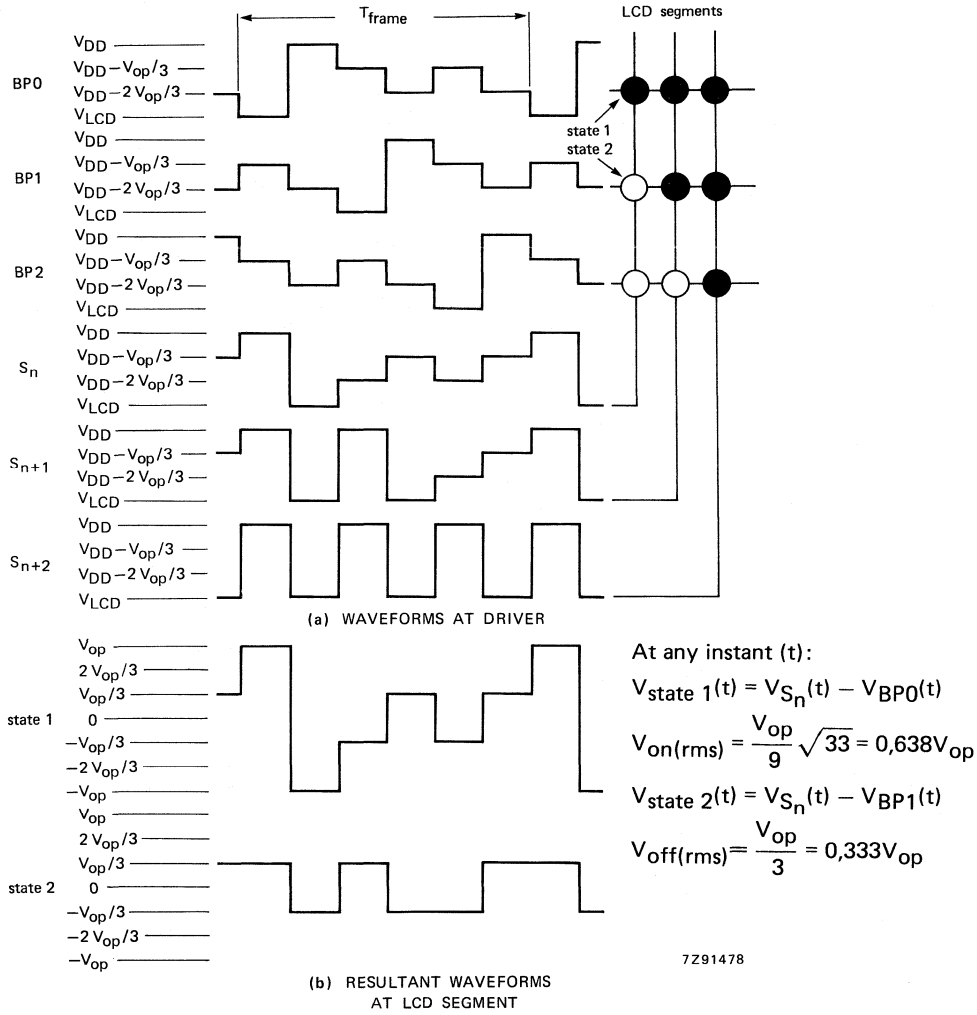


Fig. 7 Waveforms for 1 : 3 multiplex drive mode: $V_{op} = V_{DD} - V_{LCD}$.

LCD drive mode waveforms (continued)

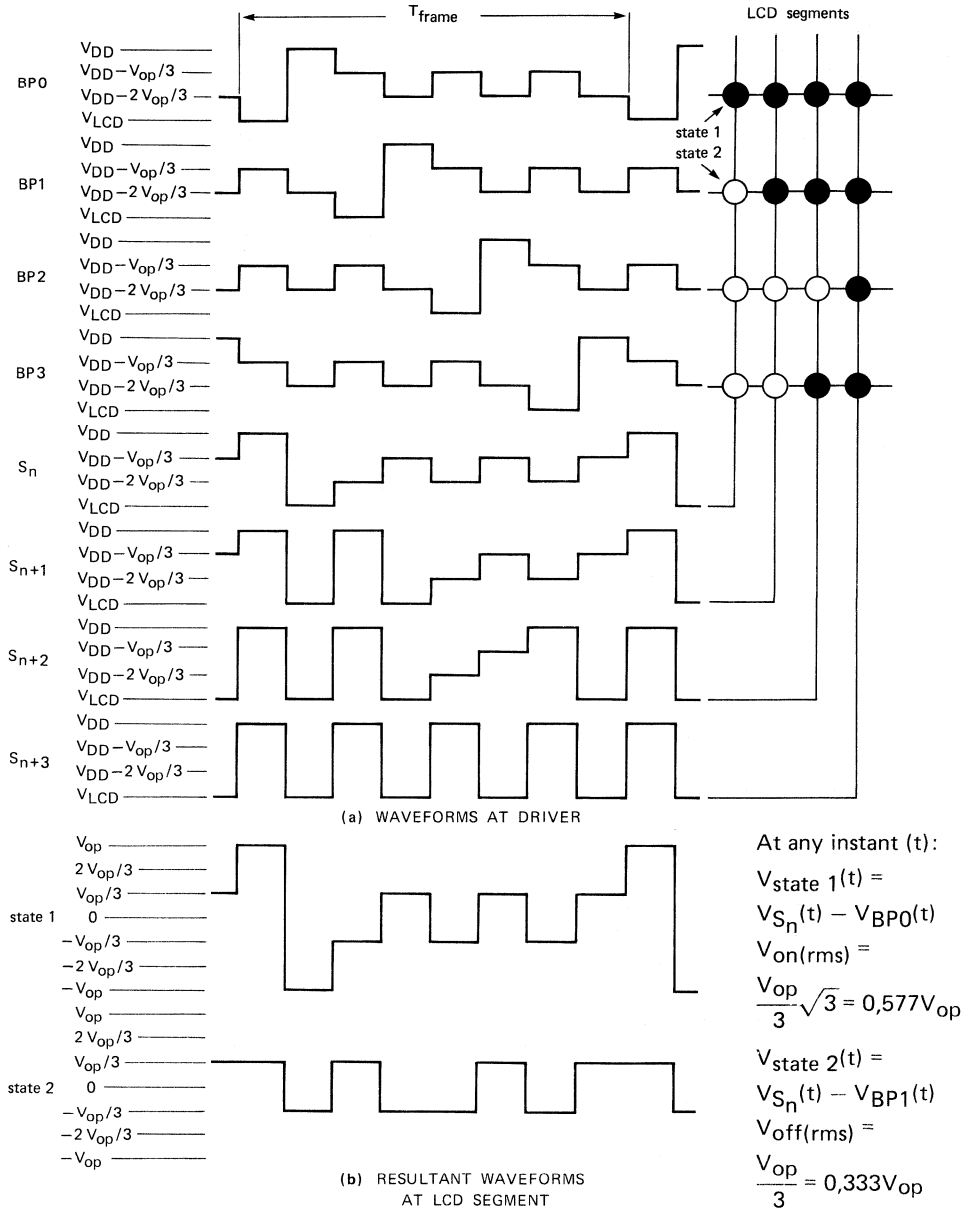


Fig. 8 Waveforms for 1 : 4 multiplex drive mode: $V_{op} = V_{DD} - V_{LCD}$.

Oscillator

Internal clock

The internal logic and the LCD drive signals of the PCF8576 are timed either by the built-in oscillator or from an external clock. When the internal oscillator is used, frequency control is performed by a single resistor connected between OSC (pin 6) and V_{SS} (pin 11) as shown in Fig. 9. In this case, the output from CLK (pin 4) provides the clock signal for cascaded PCF8576s in the system.

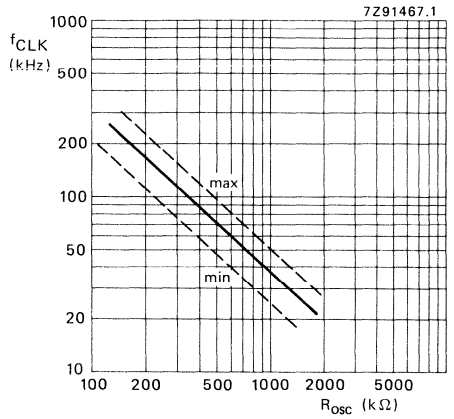


Fig. 9 Oscillator frequency as a function of R_{osc}: $f_{CLK} \approx (3{,}4 \times 10^7 / R_{osc})$ kHz·Ω.

External clock

The condition for external clock is made by tying OSC (pin 6) to V_{DD}; CLK (pin 4) then becomes the external clock input.

The clock frequency (f_{CLK}) determines the LCD frame frequency and the maximum rate for data reception from the I^2C bus. To allow I^2C bus transmissions at their maximum data rate of 100 kHz, f_{CLK} should be chosen to be above 125 kHz.

A clock signal must always be supplied to the device; removing the clock may freeze the LCD in a d.c. state.

Timing

The timing of the PCF8576 organizes the internal data flow of the device. This includes the transfer of display data from the display RAM to the display segment outputs. In cascaded applications, the synchronization signal $\overline{SYNC}$ maintains the correct timing relationship between the PCF8576s in the system. The timing also generates the LCD frame frequency which it derives as an integer multiple of the clock frequency (Table 3). The frame frequency is set by the choice of value for R_{osc} when internal clock is used, or by the frequency applied to pin 4 when external clock is used.

Table 3 LCD frame frequencies

PCF8576 mode	recommended R_{osc} (kΩ)	f_{frame}	nominal f_{frame} (Hz)
normal mode	180	$f_{CLK}/2880$	64
power-saving mode	1200	$f_{CLK}/480$	64

Timing (continued)

The ratio between the clock frequency and the LCD frame frequency depends on the mode in which the device is operating. In the normal mode, R_{OSC} = 180 kΩ will result in the nominal frame frequency. In the power-saving mode the reduction ratio is six times smaller; this allows the clock frequency to be reduced by a factor of six and for the same frame frequency R_{OSC} will be 1,2 MΩ. The reduced clock frequency and the increased value of R_{OSC} together contribute to a significant reduction in power dissipation. The lower clock frequency has the disadvantage of increasing the response time when large amounts of display data are transmitted on the I^2C bus. When a device is unable to 'digest' a display data byte before the next one arrives, it holds the SCL line LOW until the first display data byte is stored. This slows down the transmission rate of the I^2C bus but no data loss occurs.

Display latch

The display latch holds the display data while the corresponding multiplex signals are generated. There is a one-to-one relationship between the data in the display latch, the LCD segment outputs and one column of the display RAM.

Shift register

The shift register serves to transfer display information from the display RAM to the display latch while previous data are displayed.

Segment outputs

The LCD drive section includes 40 segment outputs S0 to S39 (pins 17 to 56) which should be connected directly to the LCD. The segment output signals are generated in accordance with the multiplexed backplane signals and with the data resident in the display latch. When less than 40 segment outputs are required the unused segment outputs should be left open.

Backplane outputs

The LCD drive section includes four backplane outputs BP0 to BP3 which should be connected directly to the LCD. The backplane output signals are generated in accordance with the selected LCD drive mode. If less than four backplane outputs are required the unused outputs can be left open. In the 1 : 3 multiplex drive mode BP3 carries the same signal as BP1, therefore these two adjacent outputs can be tied together to give enhanced drive capabilities. In the 1 : 2 multiplex drive mode BP0 and BP2, BP1 and BP3 respectively carry the same signals and may also be paired to increase the drive capabilities. In the static drive mode the same signal is carried by all four backplane outputs and they can be connected in parallel for very high drive requirements.

Display RAM

The display RAM is a static 40 x 4-bit RAM which stores LCD data. A logic 1 in the RAM bit-map indicates the 'on' state of the corresponding LCD segment; similarly, a logic 0 indicates the 'off' state. There is a one-to-one correspondence between the RAM addresses and the segment outputs, and between the individual bits of a RAM word and the backplane outputs. The first RAM column corresponds to the 40 segments operated with respect to backplane BP0 (Fig. 10). In multiplexed LCD applications the segment data of the second, third and fourth column of the display RAM are time-multiplexed with BP1, BP2 and BP3 respectively.

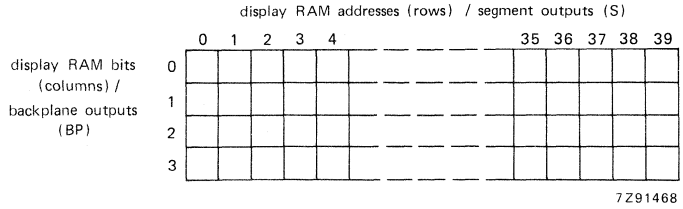


Fig. 10 Display RAM bit-map showing direct relationship between display RAM addresses and segment outputs, and between bits in a RAM word and backplane outputs.

When display data are transmitted to the PCF8576 the display bytes received are stored in the display RAM according to the selected LCD drive mode. To illustrate the filling order, an example of a 7-segment numeric display showing all drive modes is given in Fig. 11; the RAM filling organization depicted applies equally to other LCD types.

With reference to Fig. 11, in the static drive mode the eight transmitted data bits are placed in bit 0 of eight successive display RAM addresses. In the 1 : 2 multiplex drive mode the eight transmitted data bits are placed in bits 0 and 1 of four successive display RAM addresses. In the 1 : 3 multiplex drive mode these bits are placed in bits 0, 1 and 2 of three successive addresses, with bit 2 of the third address left unchanged. This last bit may, if necessary, be controlled by an additional transfer to this address but care should be taken to avoid overriding adjacent data because full bytes are always transmitted. In the 1 : 4 multiplex drive mode the eight transmitted data bits are placed in bits 0, 1, 2 and 3 of two successive display RAM addresses.

Data pointer

The addressing mechanism for the display RAM is realized using the data pointer. This allows the loading of an individual display data byte, or a series of display data bytes, into any location of the display RAM. The sequence commences with the initialization of the data pointer by the LOAD DATA POINTER command. Following this, an arriving data byte is stored starting at the display RAM address indicated by the data pointer thereby observing the filling order shown in Fig. 11. The data pointer is automatically incremented according to the LCD configuration chosen. That is, after each byte is stored, the contents of the data pointer are incremented by eight (static drive mode), by four (1 : 2 multiplex drive mode), by three (1 : 3 multiplex drive mode) or by two (1 : 4 multiplex drive mode).

Subaddress counter

The storage of display data is conditioned by the contents of the subaddress counter. Storage is allowed to take place only when the contents of the subaddress counter agree with the hardware subaddress applied to A0, A1 and A2 (pins 7, 8, and 9). The subaddress counter value is defined by the DEVICE SELECT command. If the contents of the subaddress counter and the hardware subaddress do not agree then data storage is inhibited but the data pointer is incremented as if data storage had taken place. The subaddress counter is also incremented when the data pointer overflows.

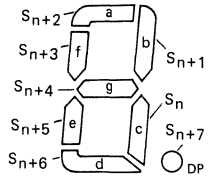
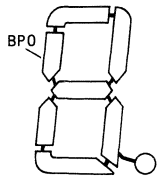
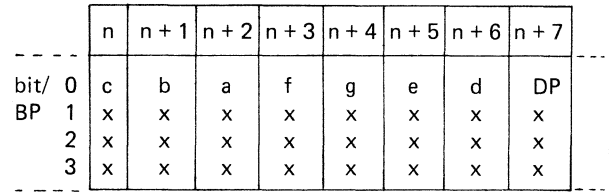
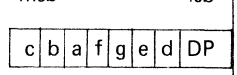
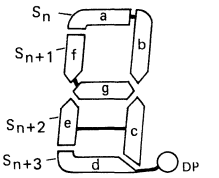
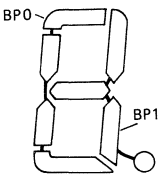
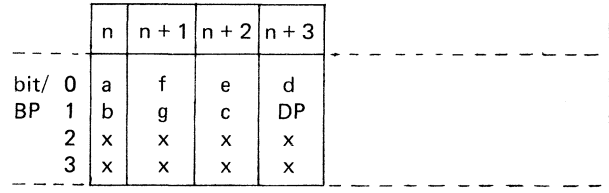
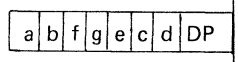
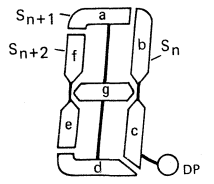
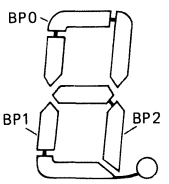
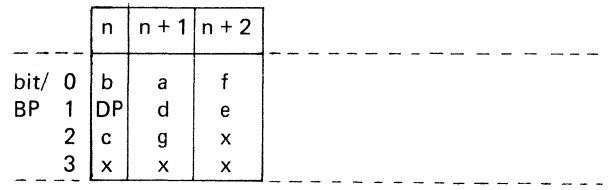
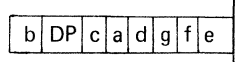
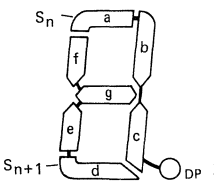
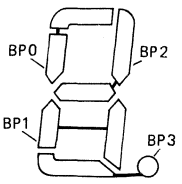
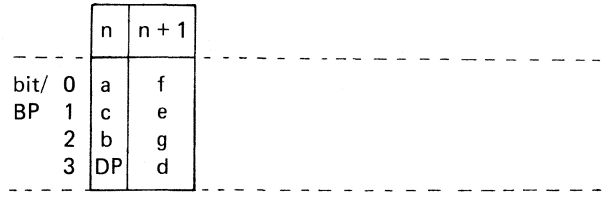
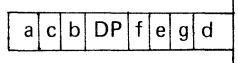
drive mode	LCD segments	LCD backplanes	display RAM filling order	transmitted display byte
static				
1 : 2 multiplex				
1 : 3 multiplex				
1 : 4 multiplex				

Fig. 11 Relationships between LCD layout, drive mode, display RAM filling order and display data transmitted over the I²C bus (x = data bit unchanged).

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Subaddress counter (continued)

The storage arrangements described lead to extremely efficient data loading in cascaded applications. When a series of display bytes are being sent to the display RAM, automatic wrap-over to the next PCF8576 occurs when the last RAM address is exceeded. Subaddressing across device boundaries is successful even if the change to the next device in the cascade occurs within a transmitted character (such as during the 14th display data byte transmitted in 1 : 3 multiplex mode).

Output bank selector

This selects one of the four bits per display RAM address for transfer to the display latch. The actual bit chosen depends on the particular LCD drive mode in operation and on the instant in the multiplex sequence. In 1 : 4 multiplex, all RAM addresses of bit 0 are the first to be selected, these are followed by the contents of bit 1, bit 2 and then bit 3. Similarly in 1 : 3 multiplex, bits 0, 1 and 2 are selected sequentially. In 1 : 2 multiplex, bits 0 then 1 are selected and, in the static mode, bit 0 is selected.

The PCF8576 includes a RAM bank switching feature in the static and 1 : 2 multiplex drive modes. In the static drive mode, the BANK SELECT command may request the contents of bit 2 to be selected for display instead of bit 0 contents. In the 1 : 2 drive mode, the contents of bits 2 and 3 may be selected instead of bits 0 and 1. This gives the provision for preparing display information in an alternative bank and to be able to switch to it once it is assembled.

Input bank selector

The input bank selector loads display data into the display RAM according to the selected LCD drive configuration. Display data can be loaded in bit 2 in static drive mode or in bits 2 and 3 in 1 : 2 drive mode by using the BANK SELECT command. The input bank selector functions independently of the output bank selector.

Blinker

The display blinking capabilities of the PCF8576 are very versatile. The whole display can be blinked at frequencies selected by the BLINK command. The blinking frequencies are integer multiples of the clock frequency; the ratios between the clock and blinking frequencies depend on the mode in which the device is operating, as shown in Table 4.

An additional feature is for an arbitrary selection of LCD segments to be blinked. This applies to the static and 1 : 2 LCD drive modes and can be implemented without any communication overheads. By means of the output bank selector, the displayed RAM banks are exchanged with alternate RAM banks at the blinking frequency. This mode can also be specified by the BLINK command.

In the 1 : 3 and 1 : 4 multiplex modes, where no alternate RAM bank is available, groups of LCD segments can be blinked by selectively changing the display RAM data at fixed time intervals.

If the entire display is to be blinked at a frequency other than the nominal blinking frequency, this can be effectively performed by resetting and setting the display enable bit E at the required rate using the MODE SET command.

Blinker (continued)

Table 4 Blinking frequencies

blinking mode	normal operating mode ratio	power-saving mode ratio	nominal blinking frequency f_{blink} (Hz)
off	—	—	blinking off
2 Hz	$f_{CLK}/92160$	$f_{CLK}/15360$	2
1 Hz	$f_{CLK}/184320$	$f_{CLK}/30720$	1
0,5 Hz	$f_{CLK}/368640$	$f_{CLK}/61440$	0,5

CHARACTERISTICS OF THE I²C BUS

The I²C bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals.

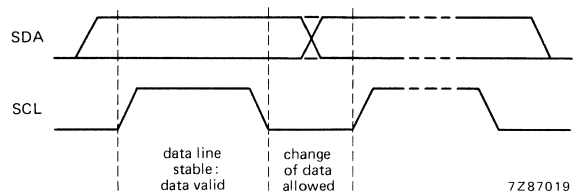


Fig. 12 Bit transfer.

Start and stop conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line while the clock is HIGH is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the stop condition (P).

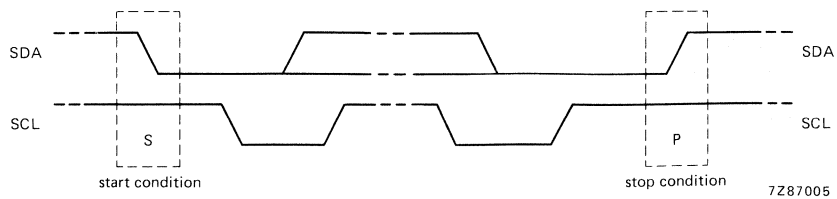


Fig. 13 Definition of start and stop conditions.

System configuration

A device generating a message is a "transmitter", a device receiving a message is a "receiver". The device that controls the message is the "master" and the devices which are controlled by the master are the "slaves".

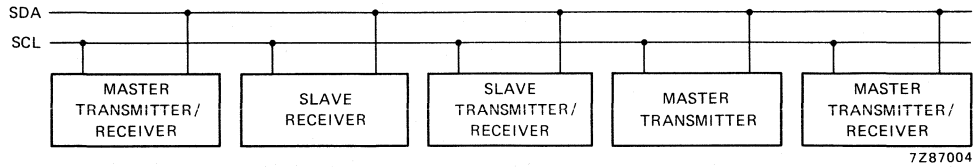


Fig. 14 System configuration.

Acknowledge

The number of data bytes transferred between the start and stop conditions from transmitter to receiver is not limited. Each byte is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter whereas the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse, set up and hold times must be taken into account. A master receiver must signal an end of data to the transmitter by *not* generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

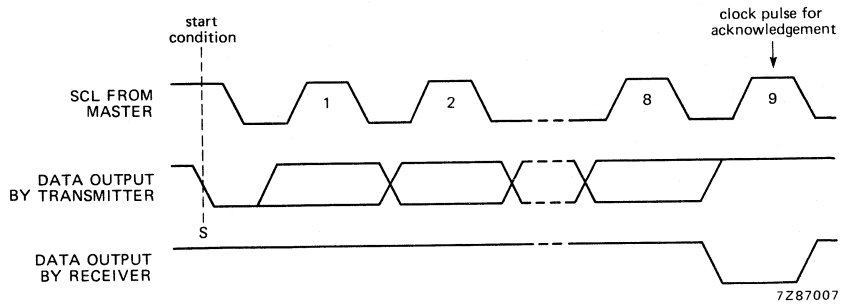


Fig. 15 Acknowledgement on the I^2C bus.

Note

The general characteristics and detailed specification of the I^2C bus are described in a separate data sheet (serial data buses) in handbook: ICs for digital systems in radio, audio and video equipment.

PCF8576 I²C bus controller

The PCF8576 acts as an I²C slave receiver. It does not initiate I²C bus transfers or transmit data to an I²C master receiver. The only data output from the PCF8576 are the acknowledge signals of the selected devices. Device selection depends on the I²C bus slave address, on the transferred command data and on the hardware subaddress.

In single device applications, the hardware subaddress inputs A0, A1 and A2 are normally tied to V_{SS} which defines the hardware subaddress 0. In multiple device applications A0, A1 and A2 are tied to V_{SS} or V_{DD} according to a binary coding scheme such that no two devices with a common I²C slave address have the same hardware subaddress.

In the power-saving mode it is possible that the PCF8576 is not able to keep up with the highest transmission rates when large amounts of display data are transmitted. If this situation occurs, the PCF8576 forces the SCL line LOW until its internal operations are completed. This is known as the 'clock synchronization feature' of the I²C bus and serves to slow down fast transmitters. Data loss does not occur.

Input filters

To enhance noise immunity in electrically adverse environments, RC low-pass filters are provided on the SDA and SCL lines.

I²C bus protocol

Two I²C bus slave addresses (0111000 and 0111001) are reserved for PCF8576. The least-significant bit of the slave address that a PCF8576 will respond to is defined by the level tied at its input SA0 (pin 10). Therefore, two types of PCF8576 can be distinguished on the same I²C bus which allows:

(a) up to 16 PCF8576s on the same I²C bus for very large LCD applications;

(b) the use of two types of LCD multiplex on the same I²C bus.

The I²C bus protocol is shown in Fig. 16. The sequence is initiated with a start condition (S) from the I²C bus master which is followed by one of the two PCF8576 slave addresses available. All PCF8576s with the corresponding SA0 level acknowledge in parallel the slave address but all PCF8576s with the alternative SA0 level ignore the whole I²C bus transfer. After acknowledgement, one or more command bytes (m) follow which define the status of the addressed PCF8576s. The last command byte is tagged with a cleared most-significant bit, the continuation bit C. The command bytes are also acknowledged by all addressed PCF8576s on the bus.

After the last command byte, a series of display data bytes (n) may follow. These display data bytes are stored in the display RAM at the address specified by the data pointer and the subaddress counter. Both data pointer and subaddress counter are automatically updated and the data are directed to the intended PCF8576 device. The acknowledgement after each byte is made only by the (A0, A1, A2) addressed PCF8576. After the last display byte, the I²C bus master issues a stop condition (P).

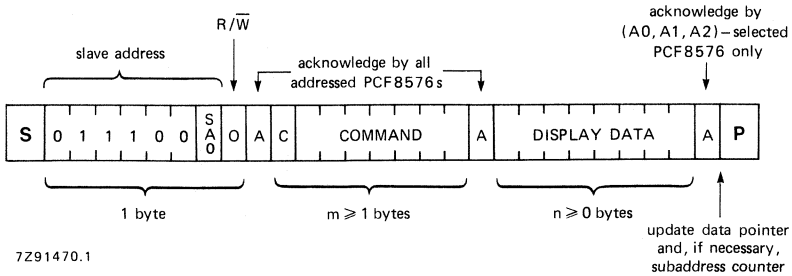


Fig. 16 I²C bus protocol.

Command decoder

The command decoder identifies command bytes that arrive on the I²C bus. All available commands carry a continuation bit C in their most-significant bit position (Fig. 17). When this bit is set, it indicates that the next byte of the transfer to arrive will also represent a command. If the bit is reset, it indicates the last command byte of the transfer. Further bytes will be regarded as display data.

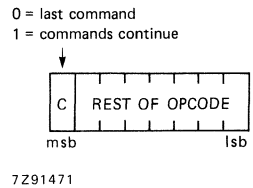


Fig. 17 General format of command byte.

The five commands available to the PCF8576 are defined in Table 5.

Command decoder (continued)

Table 5 Definition of PCF8576 commands

command/opcode	options	description
MODE SET C 1 0 LP E B M1 M0	LCD drive mode: bits M1 M0 static (1 BP): 0 1 1 : 2 MUX (2 BP): 1 0 1 : 3 MUX (3 BP): 1 1 1 : 4 MUX (4 BP): 0 0 LCD bias: bit B 1/3 bias: 0 1/2 bias: 1 display status: bit E disabled (blank): 0 enabled: 1 mode: bit LP normal mode: 0 power-saving mode: 1	Defines LCD drive mode Defines LCD bias configuration Defines display status The possibility to disable the display allows implementation of blinking under external control Defines power dissipation mode
LOAD DATA POINTER C 0 P5 P4 P3 P2 P1 P0	bits P5 P4 P3 P2 P1 P0 6-bit binary value of 0 to 39	Six bits of immediate data, bits P5 to P0, are transferred to the data pointer to define one of forty display RAM addresses
DEVICE SELECT C 1 1 0 0 A2 A1 A0	bits A0 A1 A2 3-bit binary value of 0 to 7	Three bits of immediate data, bits A0 to A2, are transferred to the subaddress counter to define one of eight hardware subaddresses

<table>
<tr><th>command/opcode</th><th>options</th><th>description</th></tr>
<tr><td>BANK SELECT

C 1 1 1 1 0 I O</td><td>
<table>
<tr><td>static</td><td>1 : 2 MUX</td><td>bit I</td></tr>
<tr><td>RAM bit 0
RAM bit 2</td><td>RAM bits 0, 1
RAM bits 2, 3</td><td>0
1</td></tr>
</table>
<table>
<tr><td>static</td><td>1 : 2 MUX</td><td>bit O</td></tr>
<tr><td>RAM bit 0
RAM bit 2</td><td>RAM bits 0, 1
RAM bits 2, 3</td><td>0
1</td></tr>
</table>
</td><td>Defines input bank selection (storage of arriving display data)

Defines output bank selection (retrieval of LCD display data)

The BANK SELECT command has no effect in 1 : 3 and 1 : 4 multiplex drive modes</td></tr>
<tr><td>BLINK

C 1 1 1 0 A BF1 BF0</td><td>
<table>
<tr><td>blink frequency</td><td>bits BF1</td><td>BF0</td></tr>
<tr><td>off</td><td>0</td><td>0</td></tr>
<tr><td>2 Hz</td><td>0</td><td>1</td></tr>
<tr><td>1 Hz</td><td>1</td><td>0</td></tr>
<tr><td>0,5 Hz</td><td>1</td><td>1</td></tr>
</table>
<table>
<tr><td>blink mode</td><td>bit A</td></tr>
<tr><td>normal blinking
alternation blinking</td><td>0
1</td></tr>
</table>
</td><td>Defines the blinking frequency

Selects the blinking mode; normal operation with frequency set by bits BF1, BF0, or blinking by alternation of display RAM banks. Alternation blinking does not apply in 1 : 3 and 1 : 4 multiplex drive modes</td></tr>
</table>

Display controller

The display controller executes the commands identified by the command decoder. It contains the status registers of the PCF8576 and coordinates their effects. The controller is also responsible for loading display data into the display RAM as required by the filling order.

Cascaded operation

In large display configurations, up to 16 PCF8576s can be distinguished on the same I^2C bus by using the 3-bit hardware subaddress (A0, A1, A2) and the programmable I^2C slave address (SA0). It is also possible to cascade up to 16 PCF8576s. When cascaded, several PCF8576s are synchronized so that they can share the backplane signals from one of the devices in the cascade. Such an arrangement is cost-effective in large LCD applications since the backplane outputs of only one device need to be through-plated to the backplane electrodes of the display. The other PCF8576s of the cascade contribute additional segment outputs but their backplane outputs are left open (Fig. 18).

The $\overline{SYNC}$ line is provided to maintain the correct synchronization between all cascaded PCF8576s. This synchronization is guaranteed after the power-on reset. The only time that $\overline{SYNC}$ is likely to be needed is if synchronization is accidently lost (e.g. by noise in adverse electrical environments; or by the definition of a multiplex mode when PCF8576s with differing SA0 levels are cascaded). $\overline{SYNC}$ is organized as an input/output pin; the output section being realized as an open-drain driver with an internal pull-up resistor. A PCF8576 asserts the $\overline{SYNC}$ line at the onset of its last active backplane signal and monitors the $\overline{SYNC}$ line at all other times. Should synchronization in the cascade be lost, it will be restored by the first PCF8576 to assert $\overline{SYNC}$. The timing relationships between the backplane waveforms and the $\overline{SYNC}$ signal for the various drive modes of the PCF8576 are shown in Fig. 19.

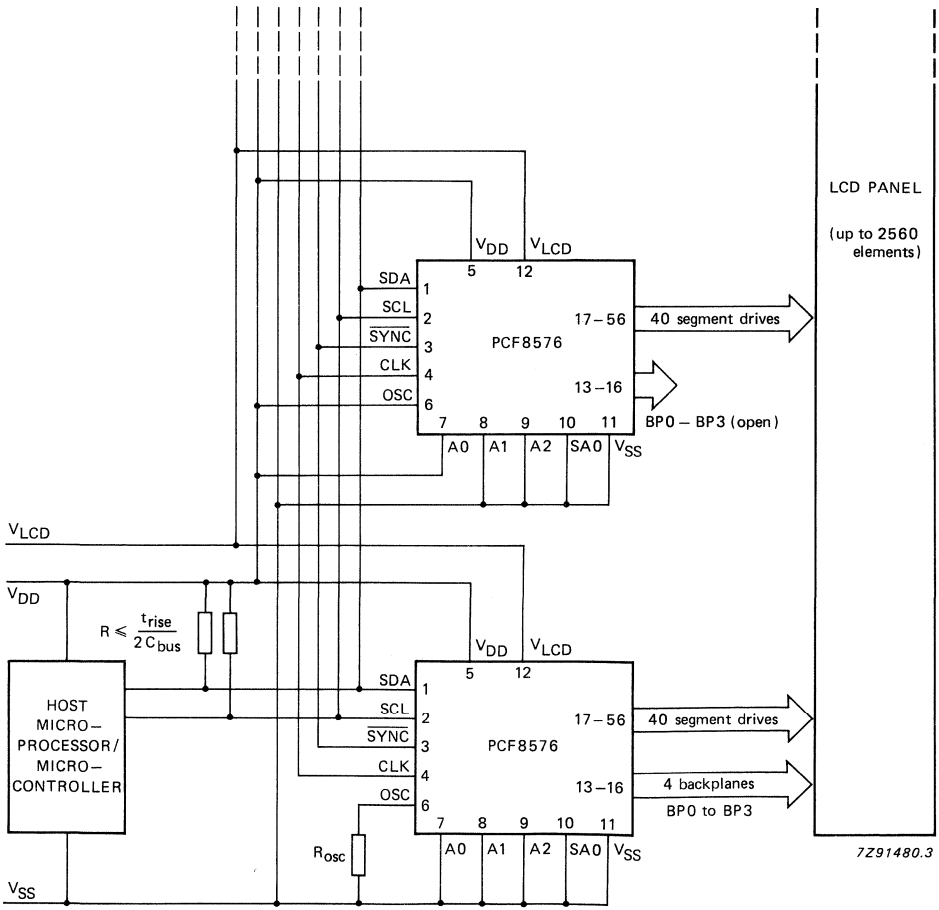
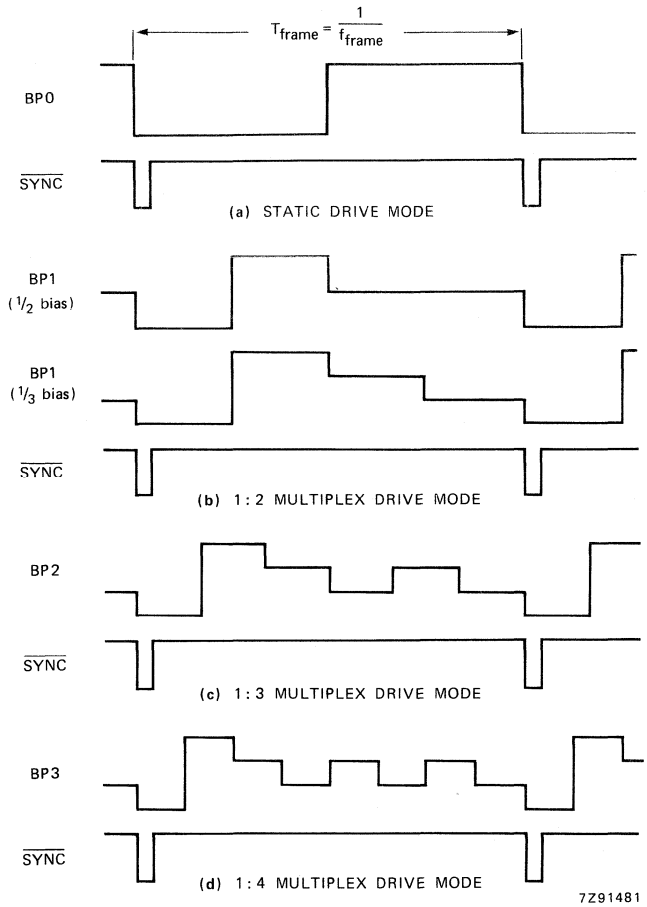


Fig. 18 Cascaded PCF8576 configuration.



Note

Excessive capacitive coupling between SCL or CLK and $\overline{SYNC}$ may cause erroneous synchronization. If this proves to be a problem, the capacitance of the $\overline{SYNC}$ line should be increased (e.g. by an external capacitor between $\overline{SYNC}$ and V_{DD}). Degradation of the positive edge of the $\overline{SYNC}$ pulse may be countered by an external pull-up resistor.

Fig. 19 Synchronization of the cascade for the various PCF8576 drive modes.

For single plane wiring of packaged PCF8576s and chip-on-glass cascading, see 'APPLICATION INFORMATION'.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range	V_{DD}		−0,5 to + 11 V
LCD supply voltage range	V_{LCD}		V_{DD}−11 to V_{DD} V
Input voltage range (SCL; SDA; A0 to A2; OSC; CLK; $\overline{SYNC}$; SA0)	V_I		V_{SS} −0,5 to V_{DD} + 0,5 V
Output voltage range (S0 to S39; BP0 to BP3)	V_O		V_{LCD}−0,5 to V_{DD} + 0,5 V
D.C. input current	$\pm I_I$	max.	20 mA
D.C. output current	$\pm I_O$	max.	25 mA
V_{DD}, V_{SS} or V_{LCD} current	$\pm I_{DD}$, $\pm I_{SS}$, $\pm I_{LCD}$	max.	50 mA
Power dissipation per package	P_{tot}	max.	400 mW
Power dissipation per output	P_O	max.	100 mW
Storage temperature range	T_{stg}		−65 to + 150 °C

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see 'Handling MOS Devices').

D.C. CHARACTERISTICS

V_{SS} = 0 V; V_{DD} = 2 to 9 V; V_{LCD} = V_{DD}−2 to V_{DD}−9 V;
T_{amb} = −40 to + 85 °C; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Operating supply voltage	V_{DD}	2	—	9	V
LCD supply voltage (note 1)	V_{LCD}	V_{DD}−9	—	V_{DD}−2	V
Operating supply current (normal mode) at f_{CLK} = 200 kHz (note 2)	I_{DD}	—	—	180	μA
Power-saving mode supply current at V_{DD} = 3,5 V; V_{LCD} = 0 V; f_{CLK} = 35 kHz (note 2)	I_{LP}	—	—	60	μA
Logic					
Input voltage LOW	V_{IL}	V_{SS}	—	0,3 V_{DD}	V
Input voltage HIGH	V_{IH}	0,7 V_{DD}	—	V_{DD}	V
Output voltage LOW at I_O = 0 mA	V_{OL}	—	—	0,05	V
Output voltage HIGH at I_O = 0 mA	V_{OH}	V_{DD}−0,05	—	—	V
Output current LOW (CLK, $\overline{SYNC}$) at V_{OL} = 1,0 V; V_{DD} = 5 V	I_{OL1}	1	—	—	mA
Output current HIGH (CLK) at V_{OH} = 4,0 V; V_{DD} = 5 V	I_{OH}	—	—	−1	mA
Output current LOW (SDA; SCL) at V_{OL} = 0,4 V; V_{DD} = 5 V	I_{OL2}	3	—	—	mA
Leakage current (SA0; A0 to A2; CLK; SCL; SDA) at V_I = V_{SS} or V_{DD}	$\pm I_{L1}$	—	—	1	μA

parameter	symbol	min.	typ.	max.	unit
Leakage current (OSC) at $V_I = V_{DD}$	$\pm I_{L2}$	–	–	1	μA
Pull-up resistor ($\overline{SYNC}$)	R_{SYNC}	20	50	150	kΩ
Power-on reset level (note 3)	V_{REF}	–	1,0	1,6	V
Tolerable spike width on bus	t_{sw}	–	–	100	ns
Input capacitance (note 4)	C_I	–	–	7	pF
LCD outputs					
D.C. voltage component (BP0 to BP3) at C_{BP} = 35 nF	$\pm V_{BP}$	–	20	–	mV
D.C. voltage component (S0 to S39) at C_S = 5 nF	$\pm V_S$	–	20	–	mV
Output impedance (BP0 to BP3) at $V_{LCD} = V_{DD}-5$ V (note 5)	R_{BP}	–	–	5	kΩ
Output impedance (S0 to S39) at $V_{LCD} = V_{DD}-5$ V (note 5)	R_S	–	–	7,0	kΩ

A.C. CHARACTERISTICS (note 6)

V_{SS} = 0 V; V_{DD} = 2 to 9 V; $V_{LCD} = V_{DD}-2$ to $V_{DD}-9$ V;
$T_{amb} = -40$ to + 85 °C; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Oscillator frequency (normal mode) at V_{DD} = 5 V; R_{osc} = 180 kΩ (note 7)	f_{CLK}	125	185	288	kHz
Oscillator frequency (power-saving mode) at V_{DD} = 3,5 V; R_{osc} = 1,2 MΩ	f_{CLKLP}	21	31	48	kHz
CLK HIGH time	t_{CLKH}	1	–	–	μs
CLK LOW time	t_{CLKL}	1	–	–	μs
$\overline{SYNC}$ propagation delay	t_{PSYNC}	–	–	400	ns
$\overline{SYNC}$ LOW time	t_{SYNCL}	1	–	–	μs
Driver delays with test loads at $V_{LCD} = V_{DD}-5$ V	t_{PLCD}	–	–	30	μs

A.C. CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
I²C bus					
Bus free time	t_{BUF}	4,7	—	—	μs
Start condition hold time	$t_{HD;STA}$	4	—	—	μs
SCL LOW time	t_{LOW}	4,7	—	—	μs
SCL HIGH time	t_{HIGH}	4	—	—	μs
Start condition set-up time (repeated start code only)	$t_{SU;STA}$	4,7	—	—	μs
Data hold time	$t_{HD;DAT}$	0	—	—	μs
Data set-up time	$t_{SU;DAT}$	250	—	—	ns
Rise time	t_R	—	—	1	μs
Fall time	t_F	—	—	300	ns
Stop condition set-up time	$t_{SU;STO}$	4,7	—	—	μs

Notes to characteristics

1. $V_{LCD} \leqslant V_{DD}-3$ V for 1/3 bias.
2. Outputs open; inputs at V_{SS} or V_{DD}; external clock with 50% duty factor; I²C bus inactive.
3. Resets all logic when $V_{DD} < V_{REF}$.
4. Periodically sampled, not 100% tested.
5. Outputs measured one at a time.
6. All timing values referred to V_{IH} and V_{IL} levels with an input voltage swing of V_{SS} to V_{DD}.
7. At $f_{CLK} < 125$ kHz, I²C bus maximum transmission speed is derated.

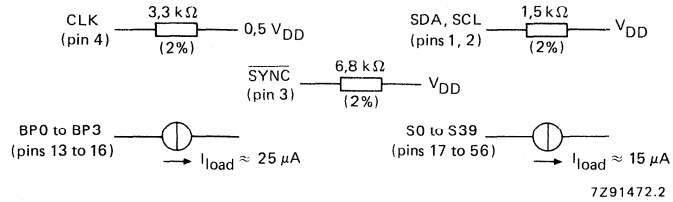


Fig. 20 Test loads.

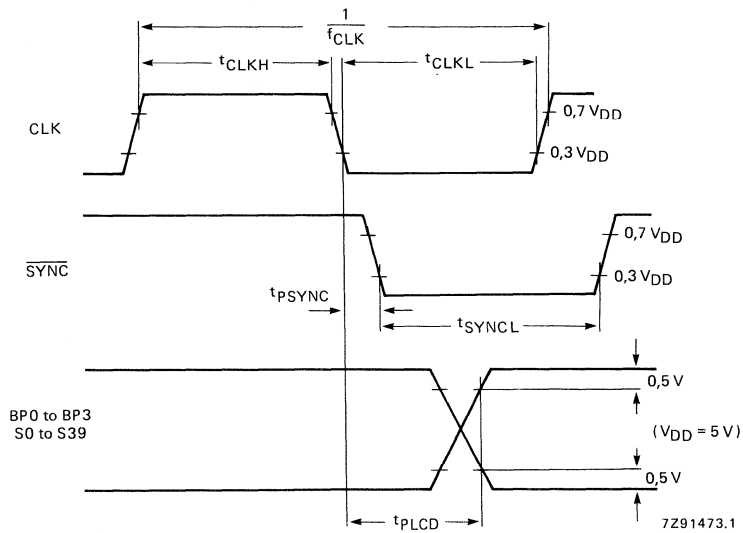


Fig. 21 Driver timing waveforms.

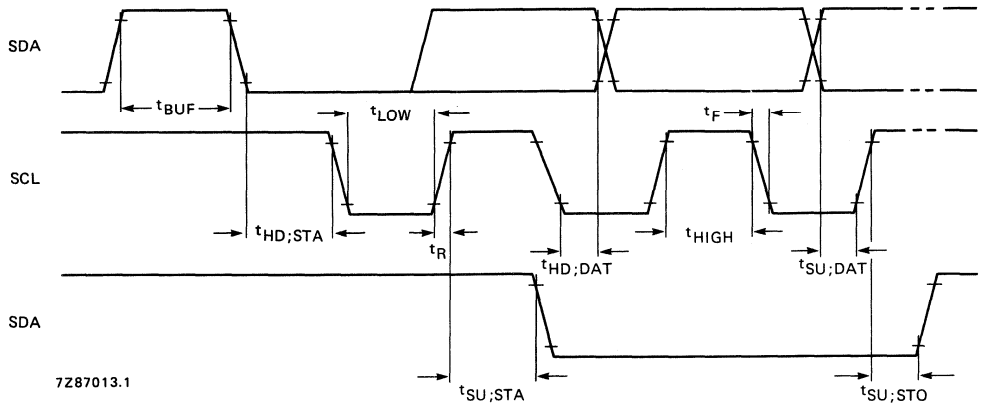
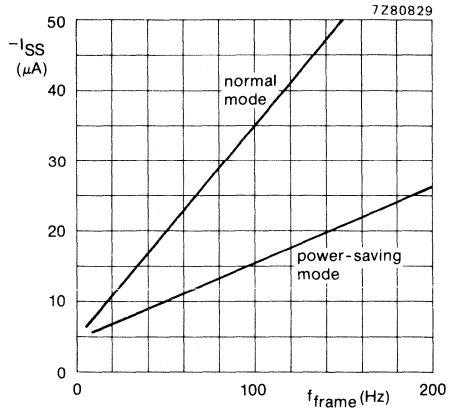
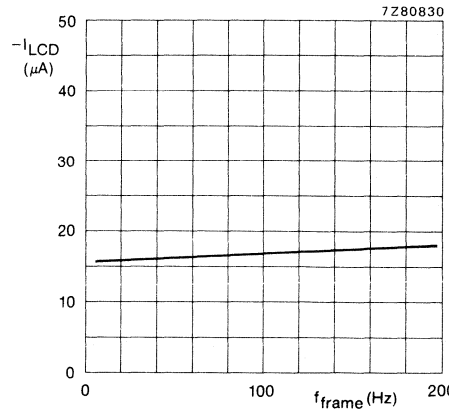


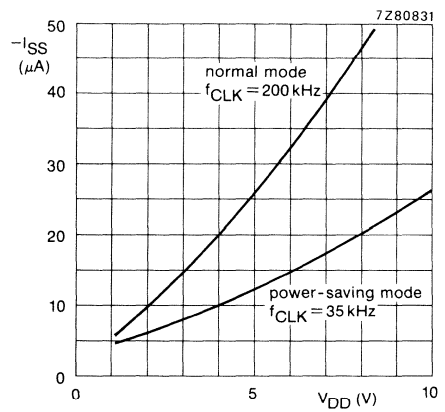
Fig. 22 I²C bus timing waveforms.



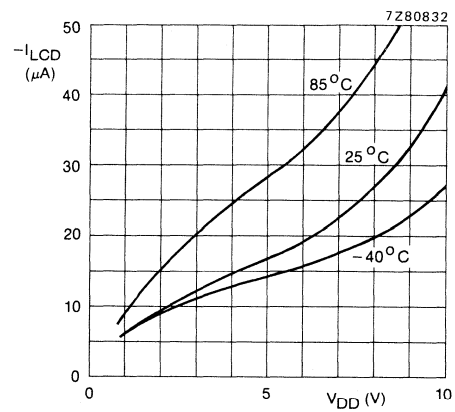
(a) V_{DD} = 5 V; V_{LCD} = 0 V; T_{amb} = 25 °C.



(b) V_{DD} = 5 V; V_{LCD} = 0 V; T_{amb} = 25 °C.

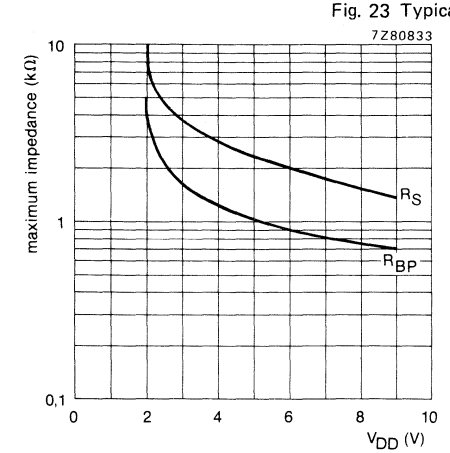


(c) V_{LCD} = 0 V; external clock; T_{amb} = −40 to + 85 °C.

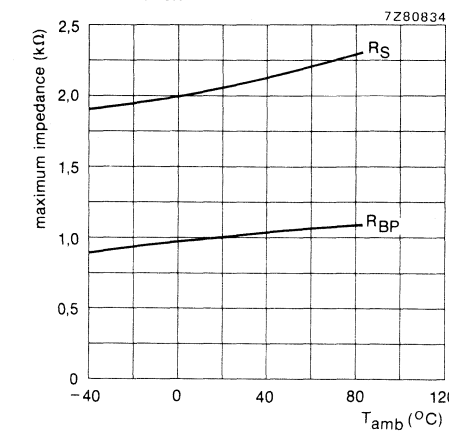


(d) V_{LCD} = 0 V; external clock; f_{CLK} = nominal frequency.

Fig. 23 Typical supply current characteristics.



(a) V_{LCD} = 0 V; T_{amb} = 25 °C.



(b) V_{DD} = 5 V; V_{LCD} = 0 V.

Fig. 24 Typical characteristics of LCD outputs.

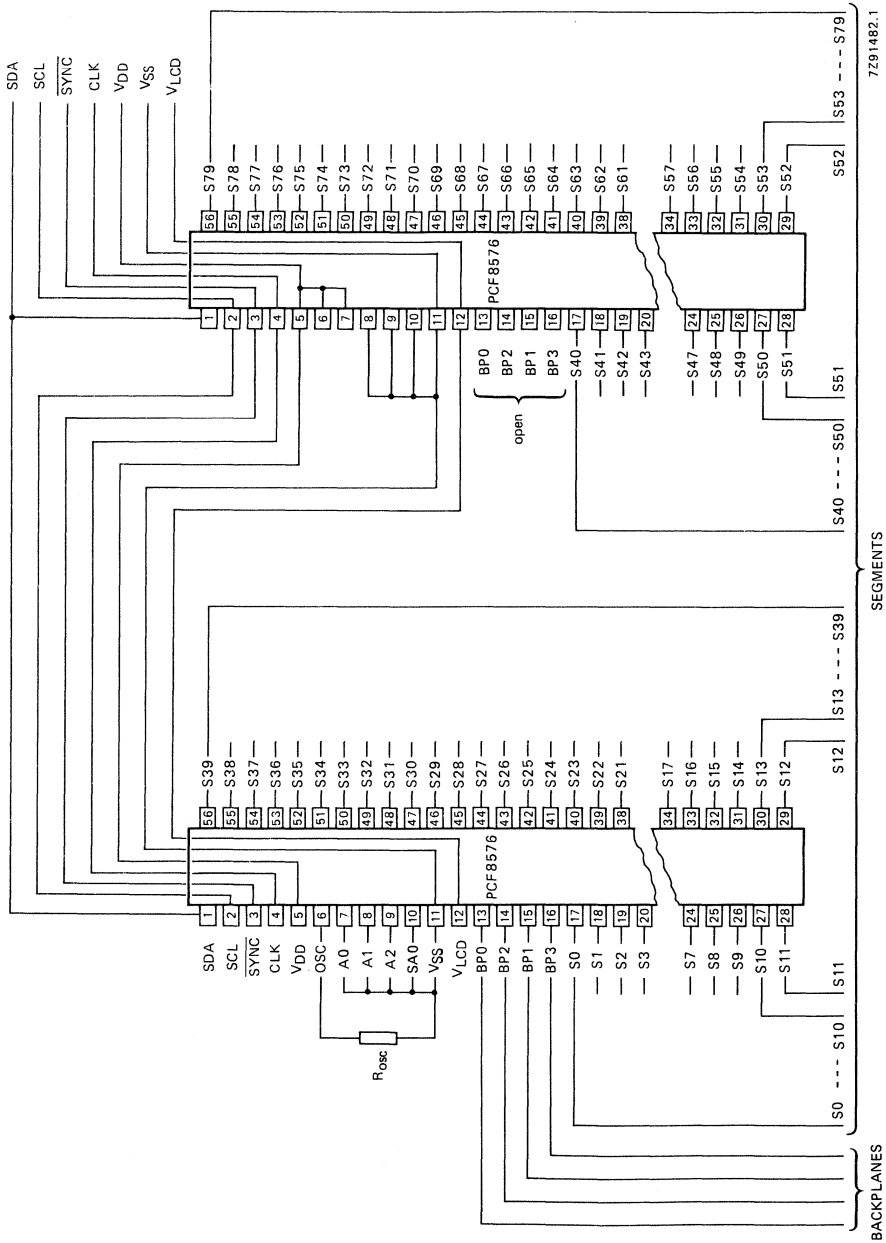


Fig. 25 Single plane wiring of packaged PCF8576s.

APPLICATION INFORMATION

Chip-on-glass cascadability in single plane

In chip-on-glass technology, where driver devices are bonded directly onto the glass of the LCD, it is important that the devices may be cascaded without the crossing of conductors, but the paths of conductors can be continued on the glass under the chip. All of this is facilitated by the PCF8576 bonding pad layout (Fig. 26). Pads needing bus interconnection between all PCF8576s of the cascade are V_{DD}, V_{SS}, V_{LCD}, CLK, SCL, SDA and $\overline{SYNC}$. These lines may be led to the corresponding pads of the next PCF8576 through the wide opening between the V_{LCD} pad and the backplane output pads. The only bussed line that does not require a second opening to lead through to the next PCF8576 is V_{LCD}, being the cascade centre. The placing of V_{LCD} adjacent to V_{SS} allows the two supplies to be tied together.

Fig. 27 shows the connection diagram for a cascaded PCF8576 application with single plane wiring. Note the use of the open space between the V_{LCD} pad and the backplane output pads to route V_{DD}, V_{SS}, CLK, SCL, SDA and $\overline{SYNC}$. The external connections may be made to either end of the cascade, wherever most convenient for the connector.

When an external clocking source is to be used, OSC of all devices should be tied to V_{DD}. The pads OSC, A0, A1, A2 and SA0 have been placed between V_{SS} and V_{DD} to facilitate wiring of oscillator, hardware subaddress and slave address.

APPLICATION INFORMATION (continued)

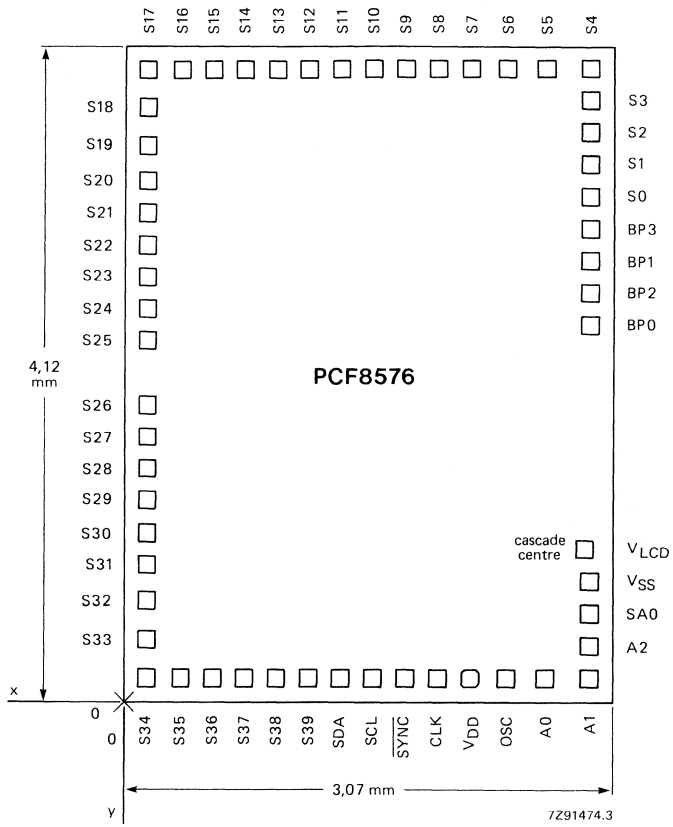


Fig. 26 PCF8576 bonding pad locations.

Bonding pad locations

All x/y coordinates are referenced to left-hand bottom corner (0/0, Fig. 26).

Dimensions in μm

pad	x	y	
S34	160	160	bottom
S35	380	↑	↑
S36	580		
S37	780		
S38	980		
S39	1180		
SDA	1380		
SCL	1580		
$\overline{\text{SYNC}}$	1780		
CLK	1980		
V_{DD}	2180		
OSC	2400		
A0	2640	↓	↓
A1	2910	160	bottom
S17	160	3960	top
S16	380	↑	↑
S15	580		
S14	780		
S13	980		
S12	1180		
S11	1380		
S10	1580		
S9	1780		
S8	1980		
S7	2180		
S6	2400		
S5	2640	↓	↓
S4	2910	3960	top

pad	x	y	
S33	160	400	left
S32	↑	640	↑
S31		860	
S30		1060	
S29		1260	
S28		1460	
S27		1660	
S26		1860	
S25		2260	
S24		2460	
S23		2660	
S22		2860	
S21		3060	
S20		3260	
S19		3480	
S18	160	3720	left
A2	2910	360	right
SA0	↕	560	↑
V_{SS}	2910	760	
V_{LCD}	2880	960	
BP0	2910	2360	
BP2	↑	2560	
BP1		2760	
BP3		2960	
S0		3160	
S1		3360	
S2		3560	
S3	2910	3760	right

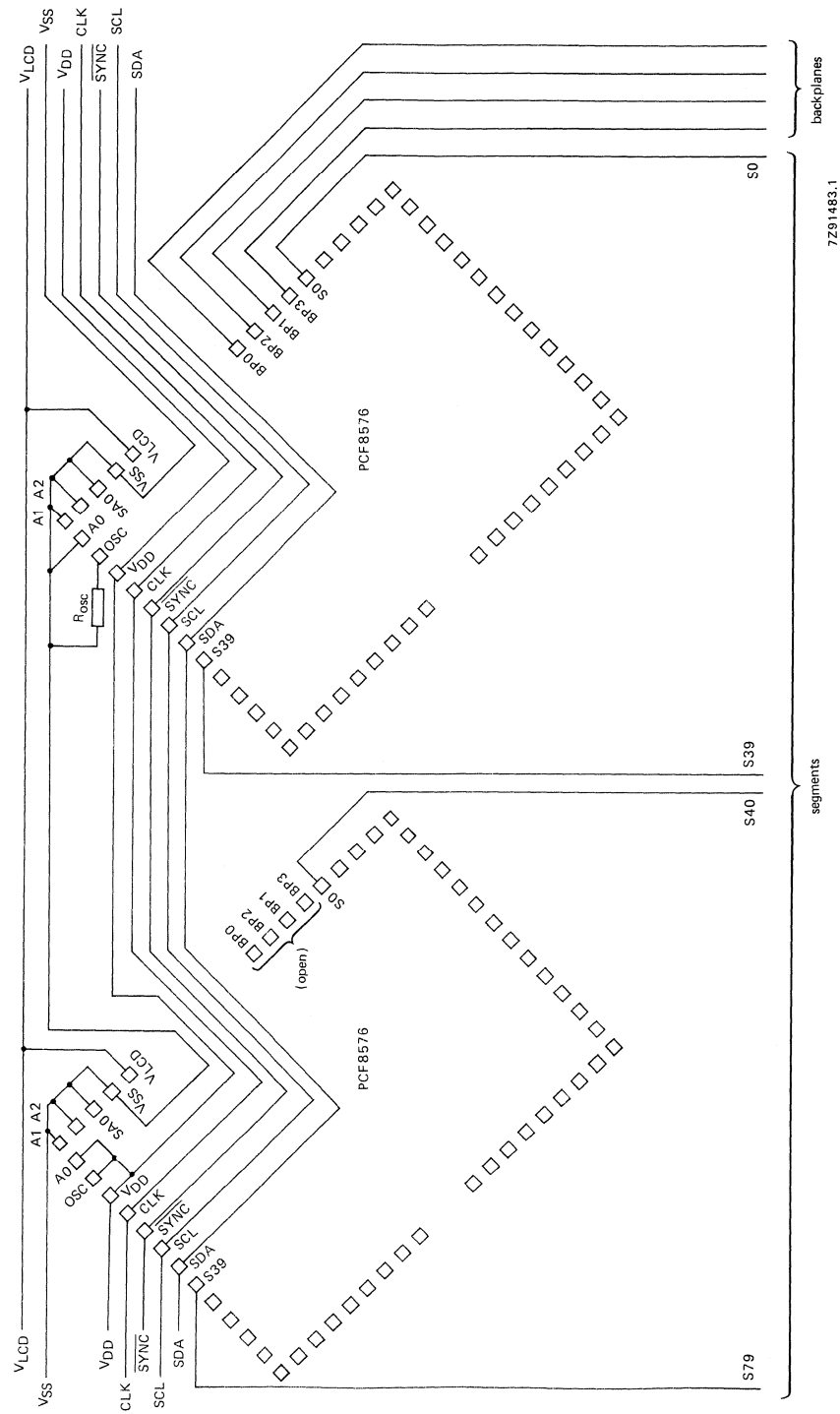


Fig. 27 Chip-on-glass application; cascaded PCF8576s with single-plane wiring (viewed from back of chip).

LCD DIRECT/DUPLEX DRIVER WITH I²C BUS INTERFACE

GENERAL DESCRIPTION

The PCF8577 is a single chip, silicon gate CMOS circuit. It is designed to drive liquid crystal displays with up to 32 segments directly, or 64 segments in a duplex manner.

The two-line I²C bus interface substantially reduces wiring overheads in remote display applications. Bus traffic is minimized in multiple IC applications by automatic address incrementing, hardware sub-addressing and display memory switching (direct drive mode).

The PCF8577 and PCF8577A differ only in their slave address.

Features

- Direct/duplex drive modes with up to 32/64 LCD-segment drive capability per device
- Operating supply voltage: 2,5 to 9 V
- Low power consumption
- I²C bus interface
- Optimized pinning for single plane wiring
- Single-pin built-in oscillator
- Auto-incremented loading across device sub-address boundaries
- Display memory switching in direct drive mode
- May be used for I²C bus output expander
- System expansion up to 256 segments (512 segments with PCF8577A)
- Power-on-reset sets all segments off (to blank)

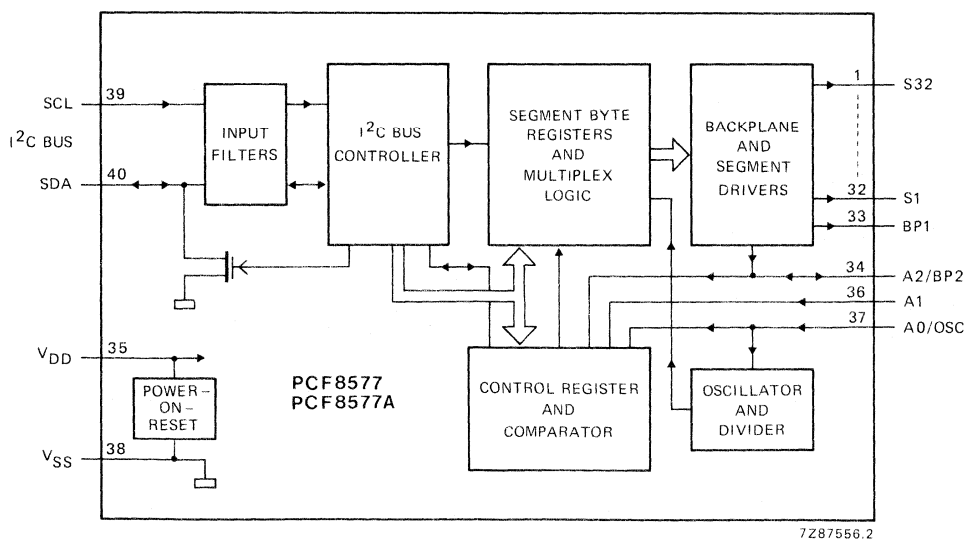


Fig. 1 Block diagram.

PACKAGE OUTLINES

PCF8577P, PCF8577AP: 40-lead DIL; plastic (SOT-129).
PCF8577T, PCF8577AT: 40-lead mini-pack; plastic (VSO-40; SOT-158A).

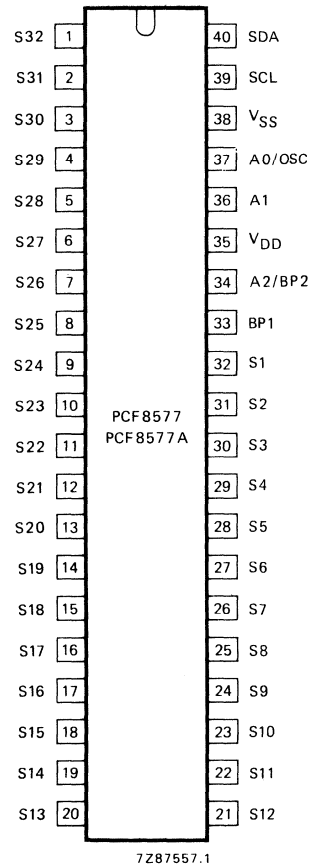


Fig. 2 Pinning diagram.

PINNING

Supply

35	V_{DD}	positive supply
38	V_{SS}	negative supply

I^2C bus

40	SDA	I^2C bus data line
39	SCL	I^2C bus clock line

Inputs

36	A1	hardware address line
37	A0/OSC	hardware address line/oscillator pin

Outputs

1 – 32	S1 – S32	segment outputs

Input – Output

34	A2/BP2	harware address line/cascade sync input/backplane output
33	BP1	cascade sync input/backplane output

FUNCTIONAL DESCRIPTION

Hardware sub-address A0, A1, A2

The hardware sub-address lines A0, A1, A2 are used to program the device sub-address for each PCF8577 on the bus. Lines A0 and A2 are shared with OSC and BP2 respectively to reduce pin-out requirements.

A0/OSC Line A0 is defined as LOW (logic 0) when this pin is used for the local oscillator or when connected to V_{SS}. Line A0 is defined as HIGH (logic 1) when connected to V_{DD}.

A1 Line A1 must be defined as LOW (logic 0) or as HIGH (logic 1) by connection to V_{SS} or V_{DD} respectively.

A2/BP2 In the direct drive mode the second backplane signal BP2 is not used and the A2/BP2 pin is exclusively the A2 input. Line A2 is defined as LOW (logic 0) when connected to V_{SS} or, if this is not possible, by leaving it unconnected (internal pull-down). Line A2 is defined as HIGH (logic 1) when connected to V_{DD}.

In the duplex drive mode the second backplane signal BP2 is required and the A2 signal is undefined. In this mode device selection is made exclusively from lines A0 and A1.

Oscillator A0/OSC

The PCF8577 has a single-pin built-in oscillator which provides the modulation for the LCD segment driver outputs. One external resistor and one external capacitor are connected to the A0/OSC pin to form the oscillator. In an expanded system containing more than one PCF8577 the backplane signals are usually common to all devices and only one oscillator is needed. The devices which are not used for the oscillator are put into the expansion mode by connecting the A0/OSC pin to either V_{DD} or V_{SS} depending on the required state for A0. In the expansion mode each PCF8577 is synchronized from the backplane signal(s).

User-accessible registers

There are nine user-accesible 1-byte registers. The first is a control register which is used to control the loading of data into the segment byte registers and to select display options. The other eight are segment byte registers, split into two banks of storage, which store the segment data. The set of even numbered segment byte registers is called BANK A. Odd numbered segment byte registers are called BANK B.

There are two slave addresses, one for PCF8577, and one for PCF8577A (see Fig. 14). All addressed devices load the second byte into the control register and each device maintains an identical copy of the control byte in the control register at all times (see I²C bus protocol Fig. 15).

The control register is shown in more detail in Fig. 3. The least-significant bits select which device and which segment byte register are loaded next. This part of the register is therefore called the Segment Byte Vector (SBV).

The upper three bits of the SBV (V5 to V3) are compared with the hardware sub-address input signals A2, A1 and A0. If they are the same then the device is enabled for loading, if not the device ignores incoming data but remains active.

The three least-significant bits of the SBV (V2 to V0) address one of the segment byte registers within the enabled chip for loading segment data.

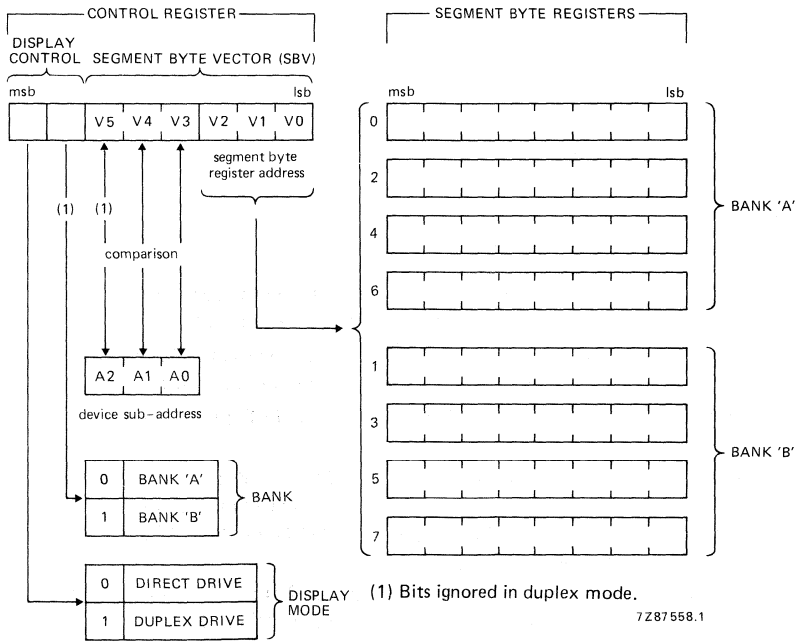


Fig. 3 PCF8577 register organization.

FUNCTIONAL DESCRIPTION (continued)

The control register also has two display control bits. These bits are named MODE and BANK. The MODE bit selects whether the display outputs are configured for direct or duplex drive displays. The BANK bit allows the user to display BANK A or BANK B.

Auto-incremented loading

After each segment byte is loaded the SBV is incremented automatically, thus auto-incremented loading occurs if more than one segment byte is received in a data transfer.

Since the SBV addresses both device and segment registers, auto-incremented loading may proceed across device boundaries provided that the hardware sub-addresses are arranged contiguously.

Direct drive mode

The PCF8577 is set to the direct drive mode by loading the MODE control bit with logic 0. In this mode only four bytes are needed to store the data for the 32 segment drivers. Setting the BANK bit to logic 0 selects even bytes (BANK A); setting the BANK bit to logic 1 selects odd bytes (BANK B).

In the direct drive mode the SBV is auto-incremented by two after the loading of each segment byte register. This means that auto-incremented loading of BANK A or BANK B is possible. Either bank may be completely or partially loaded irrespective of which bank is being displayed. Direct drive output waveforms are shown in Fig. 4.

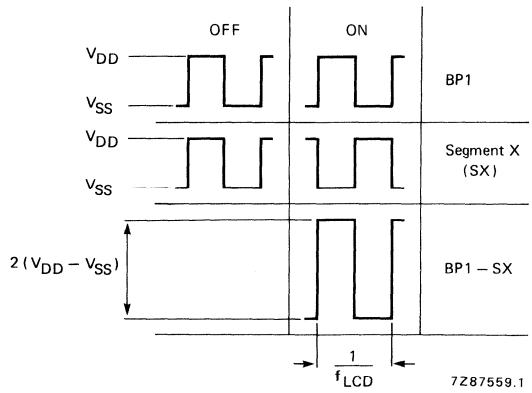


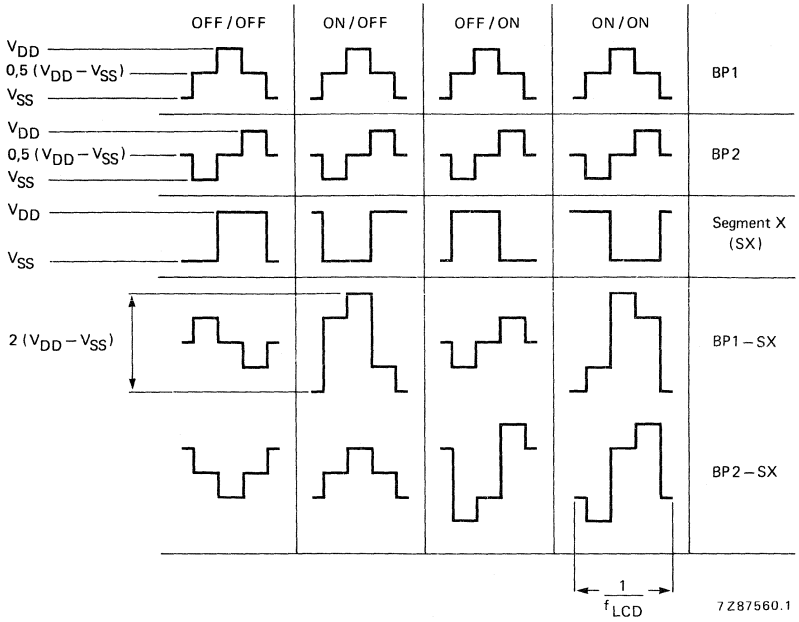
Fig. 4 Direct drive mode display output waveforms.

Duplex mode

The PCF8577 is set to the duplex mode by loading the MODE bit with logic 1. In this mode a second backplane signal (BP2) is needed and pin A2/BP2 is used for this; therefore A2 and its equivalent SBV bit V5 are undefined. The SBV auto-increments by one between loaded bytes.

All of the segment bytes are needed to store data for the 32 segment drivers and the BANK bit is ignored.

Duplex mode output waveforms are shown in Fig. 5.



$V_{ON} = 0{,}79\ (V_{DD} - V_{SS})$

$V_{OFF} = 0{,}35\ (V_{DD} - V_{SS})$

$\frac{V_{ON}}{V_{OFF}} = 2{,}26$

Fig. 5 Duplex mode display output waveforms.

DEVELOPMENT DATA

CHARACTERISTICS OF THE I²C BUS

The I²C bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals.

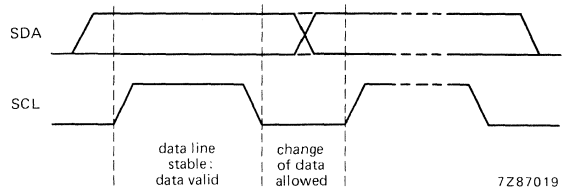


Fig. 6 Bit transfer.

Start and stop conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the stop condition (P).

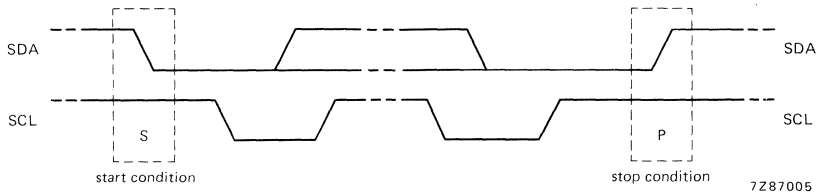


Fig. 7 Definition of start and stop conditions.

System configuration

A device generating a message is a "transmitter", a device receiving a message is the "receiver". The device that controls the message is the "master" and the devices which are controlled by the master are the "slaves".

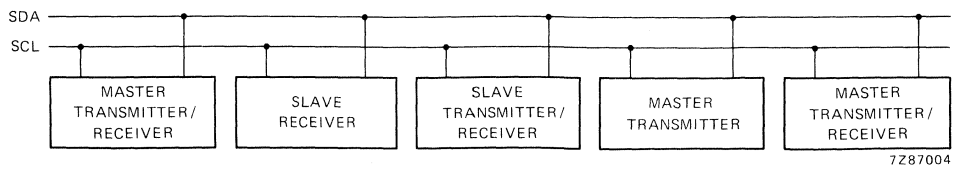


Fig. 8 System configuration.

Acknowledge

The number of data bytes transferred between the start and stop conditions from transmitter to receiver is not limited. Each byte is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter whereas the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse, set up and hold times must be taken into account. A master receiver must signal an end of data to the transmitter by *not* generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

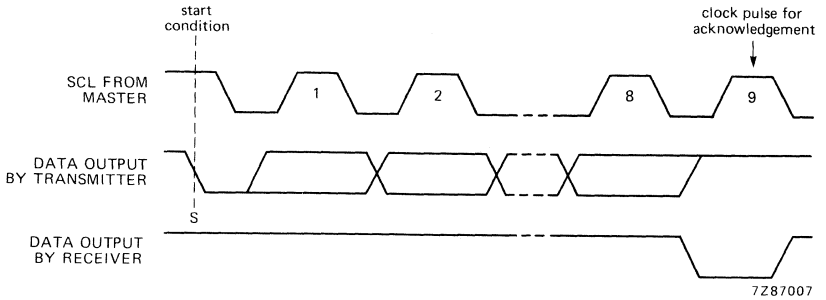


Fig. 9 Acknowledgement on the I²C bus.

Timing specifications

Within the I²C bus specifications a high-speed mode and a low-speed mode are defined. The PCF8577 operates in both modes and the timing requirements are as follows:

High-speed mode

Masters generate a bus clock with a maximum frequency of 100 kHz. Detailed timing is shown in Fig. 10.

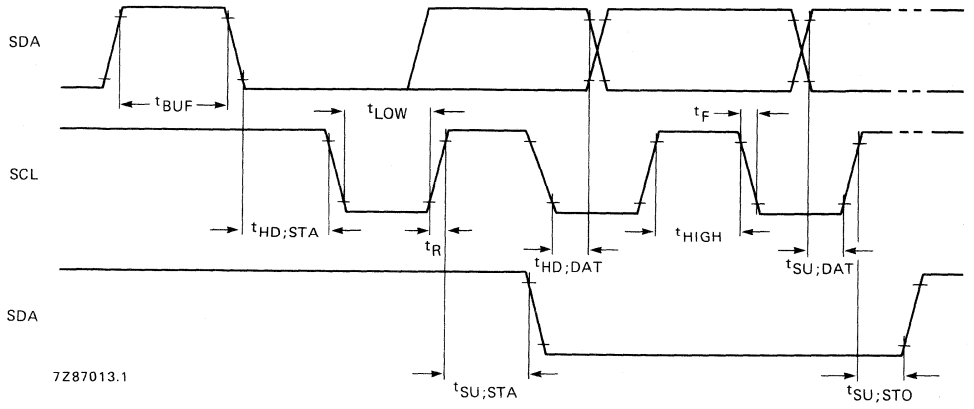


Fig. 10 Timing of the high-speed mode.

CHARACTERISTICS OF THE I^2C BUS (continued)

Where:

t_{BUF}	$t \geqslant t_{LOWmin}$	The minimum time the bus must be free before a new transmission can start
$t_{HD;STA}$	$t \geqslant t_{HIGHmin}$	Start condition hold time
t_{LOWmin}	4,7 μs	Clock LOW period
$t_{HIGHmin}$	4 μs	Clock HIGH period
$t_{SU;STA}$	$t \geqslant t_{LOWmin}$	Start condition set-up time, only valid for repeated start code
$t_{HD;DAT}$	$t \geqslant 0$ μs	Data hold time
$t_{SU;DAT}$	$t \geqslant 250$ ns	Data set-up time
t_R	$t \leqslant 1$ μs	Rise time of both the SDA and SCL line
t_F	$t \leqslant 300$ ns	Fall time of both the SDA and SCL line
$t_{SU;STO}$	$t \geqslant t_{LOWmin}$	Stop condition set-up time

Note

All the timing values referred to V_{IH} and V_{IL} levels with a voltage swing of V_{SS} to V_{DD}.

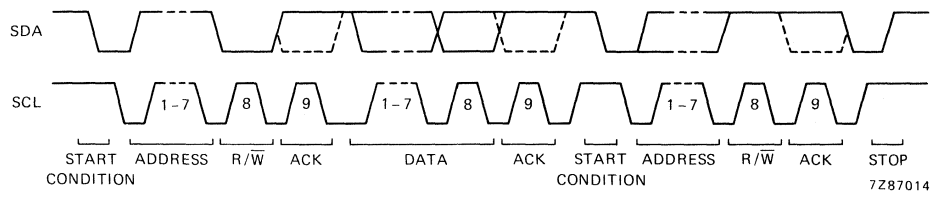


Fig. 11 Complete data transfer in the high-speed mode.

Where:

Clock t_{LOWmin}	4,7 μs
$t_{HIGHmin}$	4 μs
The dashed line is the acknowledgement of the receiver	
Mark-to-space ratio	1 : 1 (LOW-to-HIGH)
Max. number of bytes	unrestricted
Premature termination of transfer	allowed by generation of STOP condition
Acknowledge clock bit	must be provided by the master

Low-speed mode

Masters generate a bus clock with a maximum frequency of 2 kHz; a minimum LOW period of 105 μs and a minimum HIGH period of 365 μs. The mark-to-space ratio is 1 : 3 LOW-to-HIGH. Detailed timing is shown in Fig. 12.

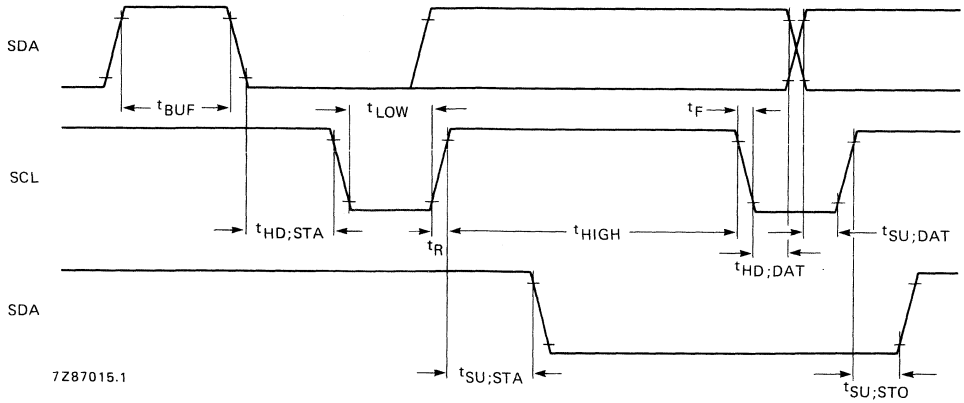


Fig. 12 Timing of the low-speed mode.

Where:

t_{BUF}	$t \geqslant 105\ \mu s$ (t_{LOWmin})
$t_{HD;STA}$	$t \geqslant 365\ \mu s$ ($t_{HIGHmin}$)
t_{LOW}	130 μs ± 25 μs
t_{HIGH}	390 μs ± 25 μs
$t_{SU;STA}$	130 μs ± 25 μs*
$t_{HD;DAT}$	$t \geqslant 0\ \mu s$
$t_{SU;DAT}$	$t \geqslant 250$ ns
t_R	$t \leqslant 1\ \mu s$
t_F	$t \leqslant 300$ ns
$t_{SU;STO}$	130 μs ± 25 μs

Note

All the timing values referred to V_{IH} and V_{IL} levels with a voltage swing of V_{SS} to V_{DD}, for definitions see high-speed mode.

* Only valid for repeated start code.

CHARACTERISTICS OF THE I²C BUS (continued)

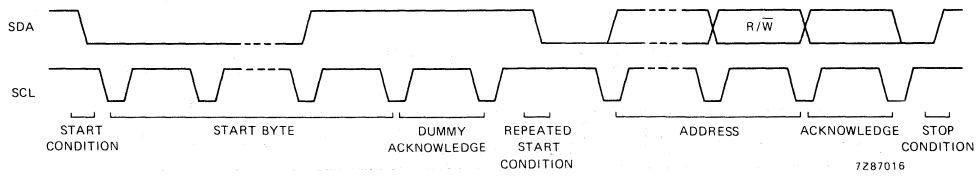


Fig. 13 Complete data transfer in the low-speed mode.

Where:

Clock t_{LOWmin}	130 μs ± 25 μs
$t_{HIGHmin}$	390 μs ± 25 μs
Mark-to-space ratio	1 : 3 (LOW-to-HIGH)
Start byte	0000 0001
Maximum number of bytes	6
Premature termination of transfer	not allowed
Acknowledge clock bit	must be provided by master

Note

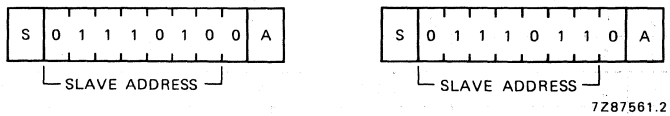
The general characteristics and detailed specification of the I²C bus are described in a separate data sheet (serial data buses) in handbook: ICs for digital systems in radio, audio and video equipment.

ADDRESSING

Before any data is transmitted on the I²C bus, the device which should respond is addressed first. The addressing is always done with the first byte transmitted after the start procedure.

Slave address

The slave address for PCF8577 and PCF8577A are shown in Fig. 14.



(a) PCF8577. (b) PCF8577A.

Fig. 14 PCF8577 and PCF8577A slave addresses.

I²C bus protocol

The PCF8577 I²C bus protocol is shown in Fig. 15.

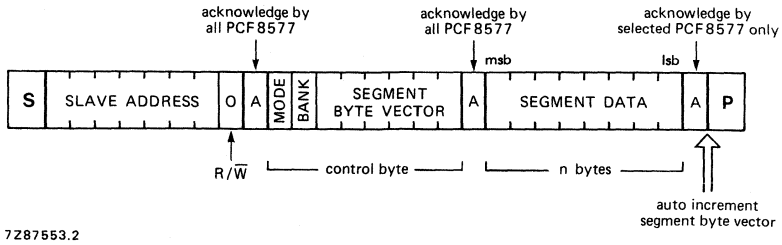


Fig. 15 I²C bus protocol.

The PCF8577 is a slave receiver and has a fixed slave address (Fig. 14). All PCF8577 on the same bus acknowledge the slave address in parallel. The second byte is always the control byte and is loaded into the control register of each PCF8577 on the bus. Subsequent data bytes are loaded into the segment registers of the selected device. Any number of data bytes may be loaded in one transfer and in an expanded system rollover of the SBV from 111 111 to 000 000 is allowed. If a stop (P) condition is given after the control byte acknowledge the segment data remains unchanged. This allows the BANK bit to be toggled without changing the segment register contents. During loading of segment data only the selected PCF8577 gives an acknowledge. Loading is terminated by generating a stop (P) condition.

DEVELOPMENT DATA

DISPLAY MEMORY MAPPING

The mapping between the eight segment registers and the segment outputs S1 to S32 is shown in Tables 1 and 2.

Since only one register bit per segment is needed in the direct drive mode, the BANK bit allows swapping of display information. If BANK is set to logic 0 even bytes (BANK A) are displayed; if BANK is set to logic 1 odd bytes (BANK B) are displayed. BP1 is always used for the backplane output in the direct drive mode.

Table 1 Segment byte — segment driver mapping in the direct drive mode.

MODE	BANK	V2	V1	V0	SEGMENT REGISTER / BIT	MSB 7	6	5	4	3	2	1	LSB 0	BACKPLANE
0	0	0	0	0	0	S8	S7	S6	S5	S4	S3	S2	S1	BP1
0	1	0	0	1	1	S8	S7	S6	S5	S4	S3	S2	S1	BP1
0	0	0	1	0	2	S16	S15	S14	S13	S12	S11	S10	S9	BP1
0	1	0	1	1	3	S16	S15	S14	S13	S12	S11	S10	S9	BP1
0	0	1	0	0	4	S24	S23	S22	S21	S20	S19	S18	S17	BP1
0	1	1	0	1	5	S24	S23	S22	S21	S20	S19	S18	S17	BP1
0	0	1	1	0	6	S32	S31	S30	S29	S28	S27	S26	S25	BP1
0	1	1	1	1	7	S32	S31	S30	S29	S28	S27	S26	S25	BP1

Mapping example: bit 0 of register 7 controls the LCD segment S25 if BANK bit is a logic 1.

DISPLAY MEMORY MAPPING (continued)

Even bytes (BANK A) correspond to backplane 1 (BP1) and odd bytes (BANK B) correspond to backplane 2 (BP2).

Table 2 Segment byte — segment driver mapping in the duplex mode.

MODE	BANK	V2	V1	V0	SEGMENT REGISTER / BIT	M S B 7	6	5	4	3	2	1	L S B 0	BACKPLANE
1	x	0	0	0	0	S8	S7	S6	S5	S4	S3	S2	S1	**BP1**
1	x	0	0	1	1	S8	S7	S6	S5	S4	S3	S2	S1	**BP2**
1	x	0	1	0	2	S16	S15	S14	S13	S12	S11	S10	S9	**BP1**
1	x	0	1	1	3	S16	S15	S14	S13	S12	S11	S10	S9	**BP2**
1	x	1	0	0	4	S24	S23	S22	S21	S20	S19	S18	S17	**BP1**
1	x	1	0	1	5	S24	S23	S22	S21	S20	S19	S18	S17	**BP2**
1	x	1	1	0	6	S32	S31	S30	S29	S28	S27	S26	S25	**BP1**
1	x	1	1	1	7	S32	S31	S30	S29	S28	S27	S26	S25	**BP2**

X = don't care.

Mapping example: bit 7 of register 5 controls the LCD segment S24/BP2.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range	V_{DD}	−0,5 to 11	V
Voltage on any pin	V_I	V_{SS} − 0,8 to V_{DD} + 0,8	V
D.C. input current	$\pm I_I$	max. 20	mA
D.C. output current	$\pm I_O$	max. 25	mA
V_{DD} or V_{SS} current	$\pm I_{DD}$, I_{SS}	max. 50	mA
Power dissipation per package	P_{tot}	max. 500*	mW
Power dissipation per output	P	max. 100	mW
Operating ambient temperature range	T_{amb}	−40 to +85	°C
Storage temperature range	T_{stg}	−65 to +150	°C

* Derate 7,7 mW/K when $T_{amb} > 60$ °C.

DEVELOPMENT DATA

CHARACTERISTICS

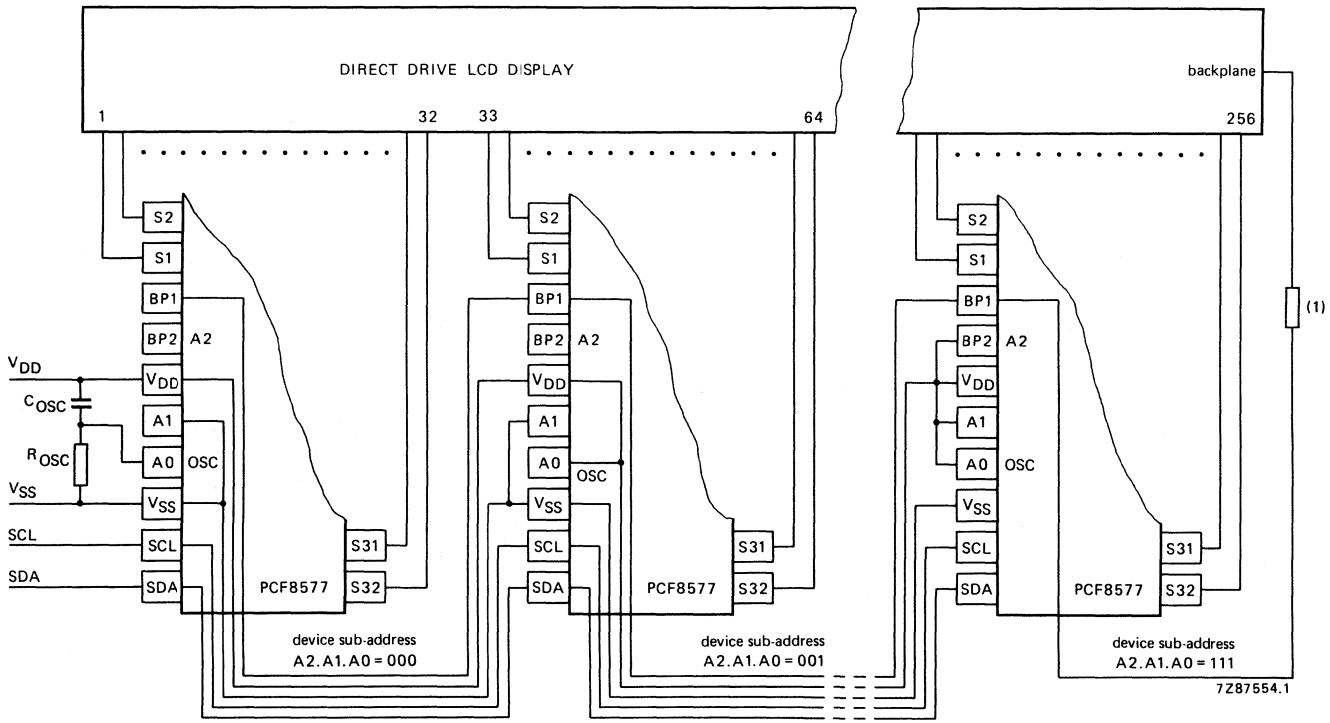
V_{DD} = 2,5 to 9 V; V_{SS} = 0 V; T_{amb} = −40 to + 85 °C unless otherwise specified

parameter	symbol	min.	typ.*	max.	unit
Supply voltage	V_{DD}	2,5	–	9,0	V
Supply current					
f_{SCL} = 100 kHz; no load; R_{OSC} = 1 MΩ	I_{DD}	–	80	250	μA
f_{SCL} = 0; no load; R_{OSC} = 1 MΩ; V_{DD} = 5 V; T_{amb} = 25 °C	I_{DD}	–	35	70	μA
Power-on-reset level**	V_{REF}	–	1,1	2,0	V
Input SCL; input/output SDA					
input voltage LOW	V_{IL}	0	–	0,8	V
input voltage HIGH	V_{IH}	2,0	–	9,0	V
output current LOW at V_{OL} = 0,4 V	I_{OL}	3,0	–	–	mA
output leakage current HIGH at V_{OH} = V_{DD}	I_{OH}	–	–	250	nA
tolerable spike width on bus	t_{sw}	–	–	100	ns
input capacitance at V_I = V_{SS}	C_I	–	–	7	pF
A1 input leakage current at V_I = V_{SS} or V_{DD}	I_I	–	–	250	nA
A2/BP2 input current at V_I = V_{DD}	I_I	–	2,0	–	μA
A0/OSC input current at V_I = V_{SS} or V_{DD}	$\pm I_I$	–	5,0	–	μA
DC component of LCD driver	$\pm V_{BP}$	–	20	–	mV
Segment loads	C_{SX}	–	–	5	nF
	R_{SX}	1	–	–	MΩ
Segment output current					
at V_{OL} = 0,4 V; V_{DD} = 5 V	I_{OL}	0,3	–	–	mA
Segment output current					
at V_{OH} = V_{DD} − 0,4 V; V_{DD} = 5 V	$-I_{OH}$	0,3	–	–	mA
Backplane load (direct drive)	C_{BP}	–	–	50	nF
	R_{BP}	100	–	–	kΩ
Backplane loads (duplex drive)	C_{BP}	–	–	35	nF
	R_{BP}	100	–	–	kΩ
Rise and fall times (V_{BP} − V_{SX})					
at maximum load	t_r, t_f	–	–	200	μs
Display frequency					
at C_{OSC} = 680 pF; R_{OSC} = 1 MΩ	f_{LCD}	65	90	120	Hz

* V_{DD} = 5 V; T_{amb} = 25 °C.

** The power-on-reset circuit resets the I²C bus logic with $V_{DD} < V_{REF}$.

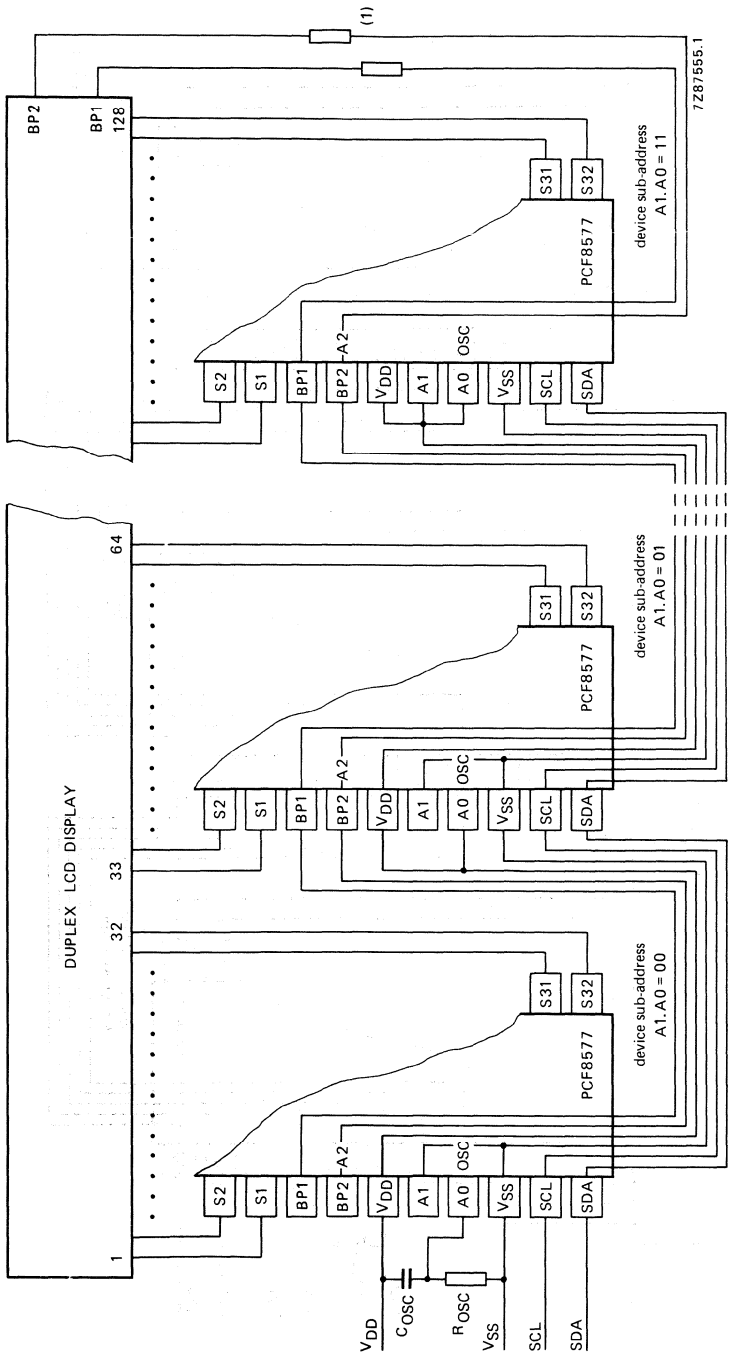
APPLICATION INFORMATION



(1) The series resistance of the display backplane must be greater than 1 Ω.

Fig. 16 Direct drive display; expansion to 256 segments using eight PCF8577.

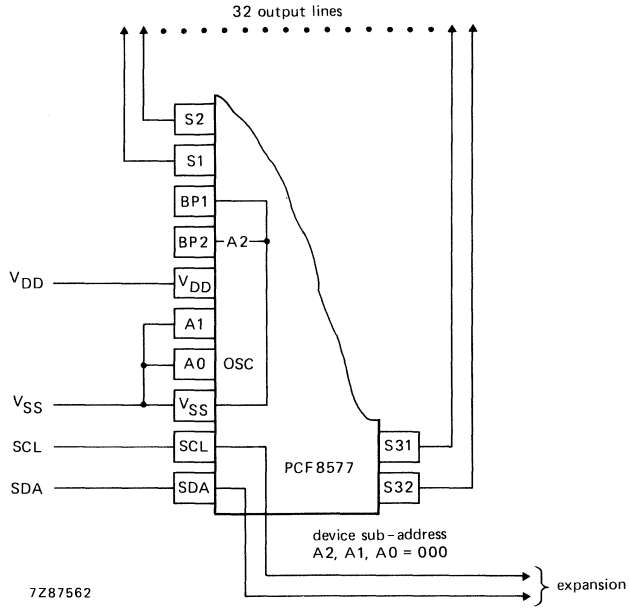
DEVELOPMENT DATA



(1) The series resistances of the display backplanes must be greater than 1 kΩ.

Fig. 17 Duplex display; expansion to 2 x 128 segments using four PCF8577.

APPLICATION INFORMATION (continued)



Notes

1. MODE bit must always be set to 0 (direct drive)
2. BANK switching is permitted
3. BP1 must always be connected to V_{SS} and A0/OSC must be connected to either V_{DD} or V_{SS} (no LCD modulation)

Fig. 18 Use of PCF8577 as 32-bit output expander in I^2C bus application.

LCD ROW/COLUMN DRIVER FOR DOT MATRIX GRAPHIC DISPLAYS

GENERAL DESCRIPTION

The PCF8578 is a low power CMOS LCD row/column driver, designed to drive dot matrix graphic displays at multiplex rates of 1 : 8, 1 : 16, 1 : 24 or 1 : 32. The device has 40 outputs, of which 24 are programmable, configurable as 32/8, 24/16, 16/24 or 8/32 rows/columns. The PCF8578 can function as a stand-alone LCD controller/driver for use in small systems, or, for larger systems can be used in conjunction with up to 32 PCF8579s for which it has been optimized. Together these two devices form a general LCD dot matrix driver chip set, capable of driving displays of up to 40,960 dots.
The PCF8578 is compatible with most microcontrollers and communicates via a two-line bidirectional bus (I^2C). Communication overheads are minimized by a display RAM with auto-incremented addressing and display bank switching.

Features

- Single chip LCD controller/driver
- Stand-alone or may be used with up to 32 PCF8579s (possible 40,960 dots)
- 40 driver outputs, configurable as 32/8, 24/16, 16/24 or 8/32 rows/columns
- Selectable row multiplex rates; 1 : 8, 1 : 16, 1 : 24 or 1 : 32
- Externally selectable bias configuration, 5 or 6 levels
- 1280-bit RAM for display data storage and scratch pad
- Display memory bank switching
- Auto-incremented data loading across hardware subaddress boundaries (with PCF8579)
- Provides display synchronization for PCF8579
- On-chip oscillator, requires only 1 external resistor
- Power-on reset blanks display
- Logic voltage supply range 2,5 V to 6,0 V
- Maximum LCD supply voltage 9 V
- Low power consumption
- I^2C bus interface
- TTL/CMOS compatible
- Compatible with most microcontrollers
- Optimized pinning for single plane wiring in multiple device applications (with PCF8579)
- Space saving 56-lead plastic mini-pack
- Compatible with chip-on-glass technology

APPLICATIONS

- Automotive information systems
- Telecommunication systems
- Point-of-sale terminals
- Computer terminals
- Instrumentation

PACKAGE OUTLINES

PCF8578T: 56-lead mini-pack; plastic (VSO-56; SOT-190).
PCF8578U: uncased chip-in-tray.

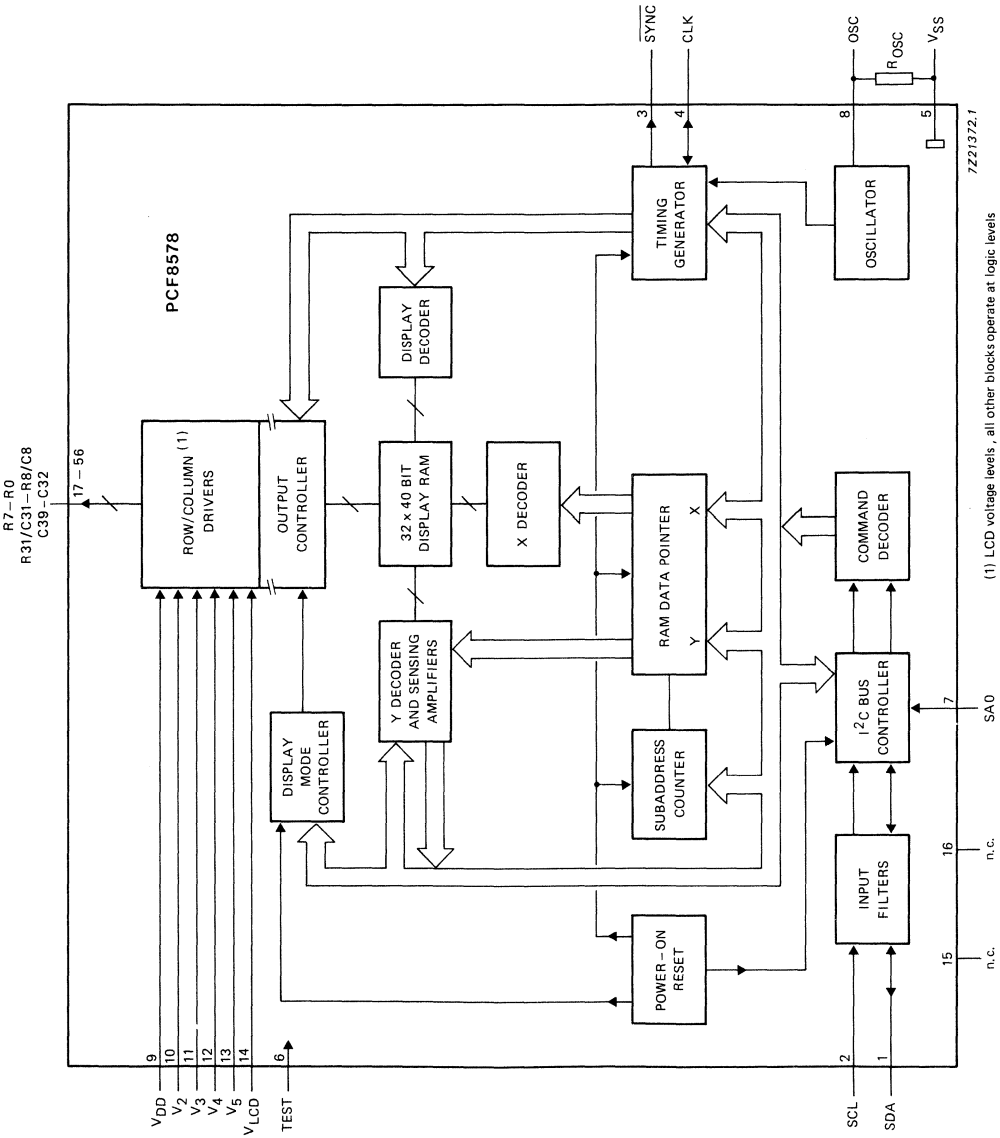


Fig. 1 Block diagram.

DEVELOPMENT DATA

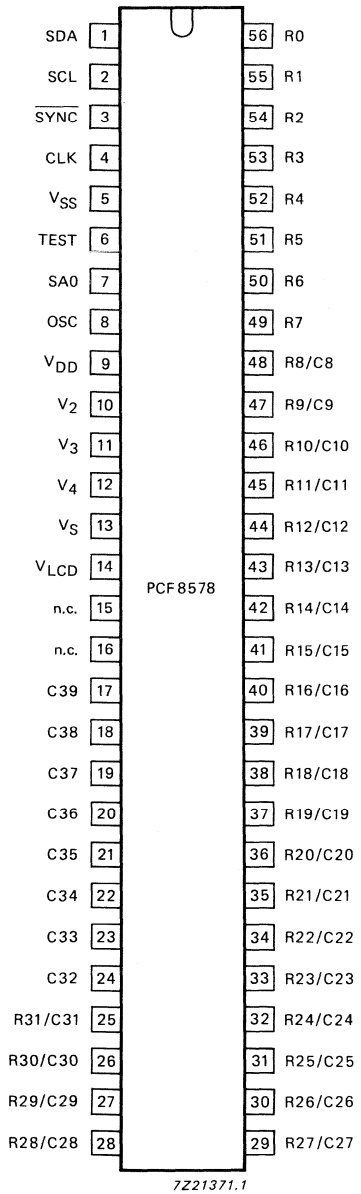


Fig. 2 Pinning diagram.

PINNING

1	SDA	Data input/output (I²C bus)
2	SCL	Clock input (I²C bus)
3	$\overline{SYNC}$	Cascade synchronization output
4	CLK	External clock input/output
5	V_{SS}	Ground (logic)
6	TEST	Test pin (connect to V_{SS})
7	SA0	I²C bus slave address input (bit 0)
8	OSC	Oscillator input
9	V_{DD}	Positive supply voltage
10	V_2	LCD bias voltage inputs
11	V_3	LCD bias voltage inputs
12	V_4	LCD bias voltage inputs
13	V_5	LCD bias voltage inputs
14	V_{LCD}	LCD supply voltage
15	n.c.	Not connected
16	n.c.	Not connected
17 to 24	C39 to C32	LCD column driver outputs
25 to 48	R31/C31 to R8/C8	LCD row/column driver outputs
49 to 56	R7 to R0	LCD row driver outputs

FUNCTIONAL DESCRIPTION

The PCF8578 row/column driver is designed for use in one of three ways:

- Stand-alone row/column driver for small displays (mixed mode)
- Row/column driver with cascaded PCF8579s (mixed mode)
- Row driver with cascaded PCF8579s (row mode)

In mixed mode, the device functions as both a row and column driver. It can be used in small stand-alone applications or for larger displays with up to 15 PCF8579s (31 when two slave addresses are used). See Table 1 for common display configurations.

In row mode, the device functions as a row driver with up to 32 row outputs and provides the clock and synchronization signals for the PCF8579. Up to 16 PCF8579s can normally be cascaded (32 when two slave addresses are used).

Table 1 Common display configurations

application	multiplex rate	mixed mode		row mode		typical applications
		rows	columns	rows	columns	
stand-alone	1 : 8	8	32	–	–	small digital or alphanumeric displays
	1 : 16	16	24	–	–	
	1 : 24	24	16	–	–	
	1 : 32	32	8	–	–	
with PCF8579	1 : 8	8	632	8 x 4	640	alphanumeric displays and dot matrix graphic displays
	1 : 16	16	624	16 x 2	640	
	1 : 24	24	616	24	640	
	1 : 32	32	608	32	640	
		using 15 PCF8579s		using 16 PCF8579s		

Bias levels may be generated by an external potential divider with appropriate decoupling capacitors. For large displays bias sources with high driver capability should be used. A typical mixed mode system operating with up to 15 PCF8579s is shown in Fig. 3 (a stand-alone system would be identical but without PCF8579).

Table 2 Multiplex rates (see Fig. 3)

resistor	multiplex rate (n)	
	$n \leqslant 9$	$n \geqslant 9$
R1	R	R
R2	$(\sqrt{n}-2)$ R	R
R3	$(3-\sqrt{n})$ R	$(\sqrt{n}-3)$ R

DEVELOPMENT DATA

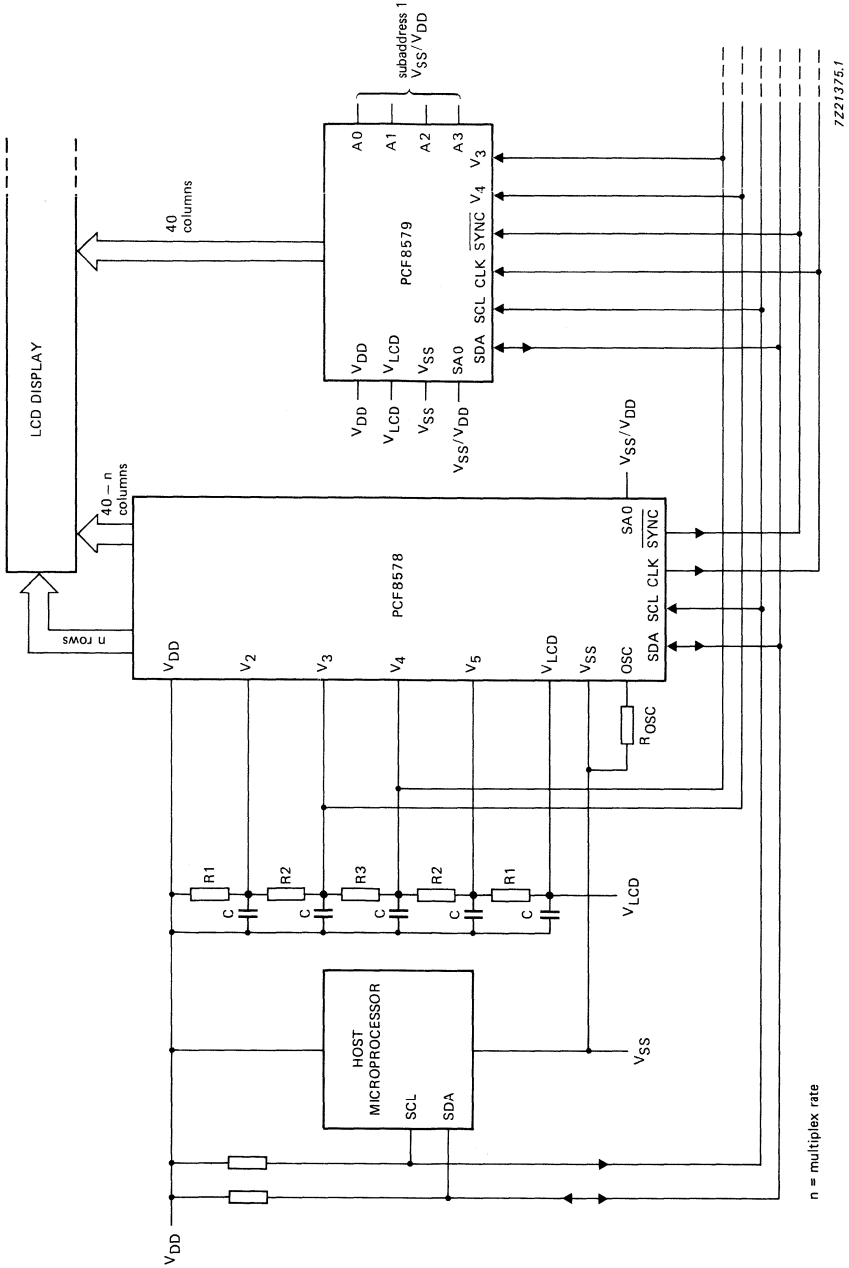


Fig. 3 Typical mixed mode configuration.

LCD COLUMN DRIVER FOR DOT MATRIX GRAPHIC DISPLAYS

GENERAL DESCRIPTION

The PCF8579 is a low power CMOS LCD column driver, designed to drive dot matrix graphic displays at multiplex rates of 1 : 8, 1 : 16, 1 : 24 or 1 : 32. The device has 40 outputs and can drive 32 x 40 dots in a 32 row multiplexed LCD. The device is optimized for use with the PCF8578 LCD row/column driver. Up to 32 PCF8579s can be cascaded and used on the same I^2C bus (using the two slave addresses). Together these two devices form a general LCD dot matrix driver chip set, capable of driving displays of up to 40,960 dots. The PCF8579 is compatible with most microcontrollers and communicates via a two-line bidirectional bus (I^2C). Communication overheads are minimized by a display RAM with auto-incremented addressing and display bank switching.

Features

- LCD column driver
- Used in conjunction with the PCF8578, this device forms part of a chip set capable of driving up to 40,960 dots
- 40 column outputs
- Selectable row multiplex rates; 1 : 8, 1 : 16, 1 : 24 or 1 : 32
- Externally selectable bias configuration, 5 or 6 levels
- Easily cascadable for large applications (up to 32 devices)
- 1280-bit RAM for display data storage
- Display memory bank switching
- Auto-incremented data loading across hardware subaddress boundaries
- Power-on reset blanks display
- Logic voltage supply range 2,5 V to 6,0 V
- Maximum LCD supply voltage 9 V
- Low power consumption
- I^2C bus interface
- TTL/CMOS compatible
- Compatible with most microcontrollers
- Optimized pinning for single plane wiring in multiple device applications
- Space saving 56-lead plastic mini-pack
- Compatible with chip-on-glass technology

APPLICATIONS

- Automotive information systems
- Telecommunication systems
- Point-of-sale terminals
- Computer terminals
- Instrumentation

PACKAGE OUTLINES

PCF8579T: 56-lead mini-pack; plastic (VSO-56; SOT-190).
PCF8579U: uncased chip-in-tray.

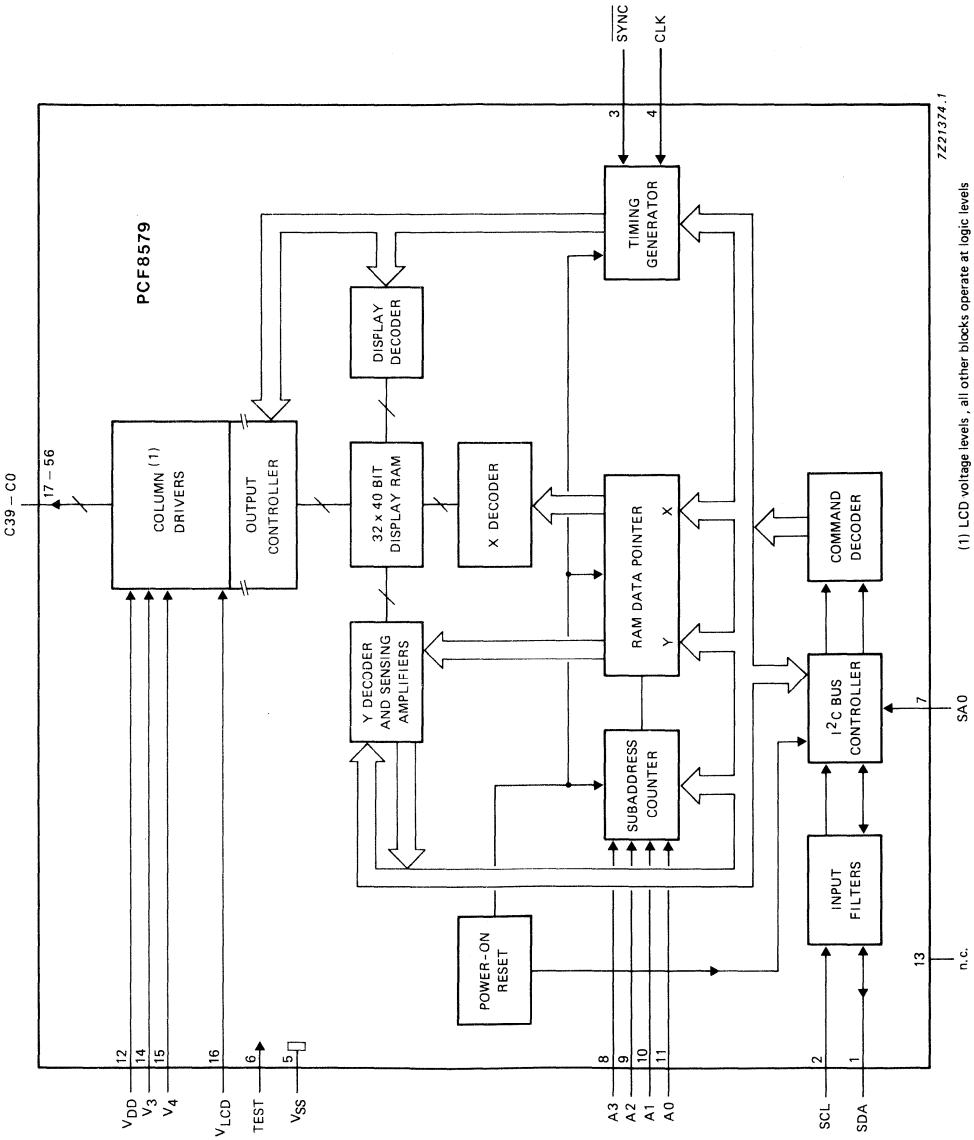


Fig. 1 Block diagram.

DEVELOPMENT DATA

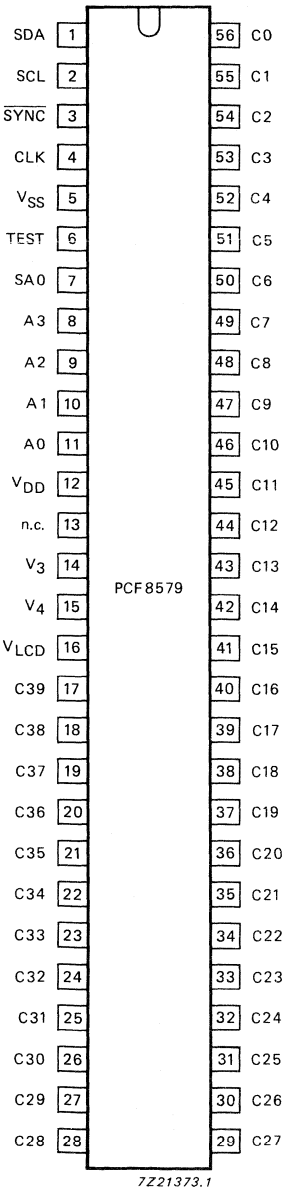


Fig. 2 Pinning diagram.

PINNING

1	SDA	Data input/output	I²C bus
2	SCL	Clock input	I²C bus
3	$\overline{SYNC}$	Cascade synchronization input	
4	CLK	External clock input	
5	V_{SS}	Ground (logic)	
6	TEST	Test pin (connect to V_{SS})	
7	SA0	I²C bus slave address input (bit 0)	
8	A3	I²C bus subaddress inputs	
9	A2	I²C bus subaddress inputs	
10	A1	I²C bus subaddress inputs	
11	A0	I²C bus subaddress inputs	
12	V_{DD}	Positive supply voltage	
13	n.c.	Not connected	
14	V_3	LCD bias voltage inputs	
15	V_4	LCD bias voltage inputs	
16	V_{LCD}	LCD supply voltage	
17 to 56	C39 to C0	LCD column driver outputs	

FUNCTIONAL DESCRIPTION

The PCF8579 column driver is designed for use with the PCF8578. Together they form a general purpose LCD dot matrix chip set.

The PCF8578 typically operates with up to 16 PCF8579s. Each of the PCF8579s is identified by a unique 4-bit hardware subaddress, set by pins A0 to A3. The PCF8578 can operate with up to 32 PCF8579s. This is achieved by setting the LSB of the I^2C bus slave address to 1 (V_{DD}) or 0 (V_{SS}) using input SA0.

Power-on reset

At power-on the PCF8579 resets to a defined starting condition as follows:

1. 1 : 32 multiplex rate
2. Display bank 0
3. Data pointer is set to X, Y address 0
4. Character mode
5. Subaddress counter is cleared
6. I^2C bus interface is initialized
7. Display blanked (by PCF8578)

Data transfers on the I^2C bus should be avoided for 1 ms following power-on to allow completion of the reset action.

Multiplexed LCD bias generation

The bias levels required to produce maximum contrast depend on the multiplex rate and the threshold voltage (V_{th}). V_{th} is typically defined as the r.m.s. voltage at which the LCD exhibits 10% contrast. Table 1 shows the optimum voltage bias levels for the PCF8578/PCF8579 as functions of V_{op} ($V_{op} = V_{DD} - V_{LCD}$), together with the discrimination ratios (D) for the different multiplex rates. A practical value for V_{op} is obtained by equating $V_{off(rms)}$ with V_{th}.

Table 1 Optimum LCD bias voltages

multiplex rate	$\frac{V_1}{V_{op}}$	$\frac{V_2}{V_{op}}$	$\frac{V_3}{V_{op}}$	$\frac{V_4}{V_{op}}$	$\frac{V_{off}}{V_{op}}$	$\frac{V_{on}}{V_{op}}$	$D = \frac{V_{on(rms)}}{V_{off(rms)}}$	$\frac{V_{op}}{V_{th}}$
1 : 8	0,739	0,522	0,478	0,261	0,297	0,430	1,477	3,37
1 : 16	0,800	0,600	0,400	0,200	0,245	0,316	1,291	4,08
1 : 24	0,830	0,661	0,339	0,170	0,214	0,263	1,230	4,68
1 : 32	0,850	0,700	0,300	0,150	0,193	0,230	1,196	5,19

Table 2 Multiplex rates (see Fig. 3)

resistor	multiplex rate (n)	
	$n \leqslant 9$	$n \geqslant 9$
R1	R	R
R2	$(\sqrt{n}-2)$ R	R
R3	$(3-\sqrt{n})$ R	$(\sqrt{n}-3)$ R

DEVELOPMENT DATA

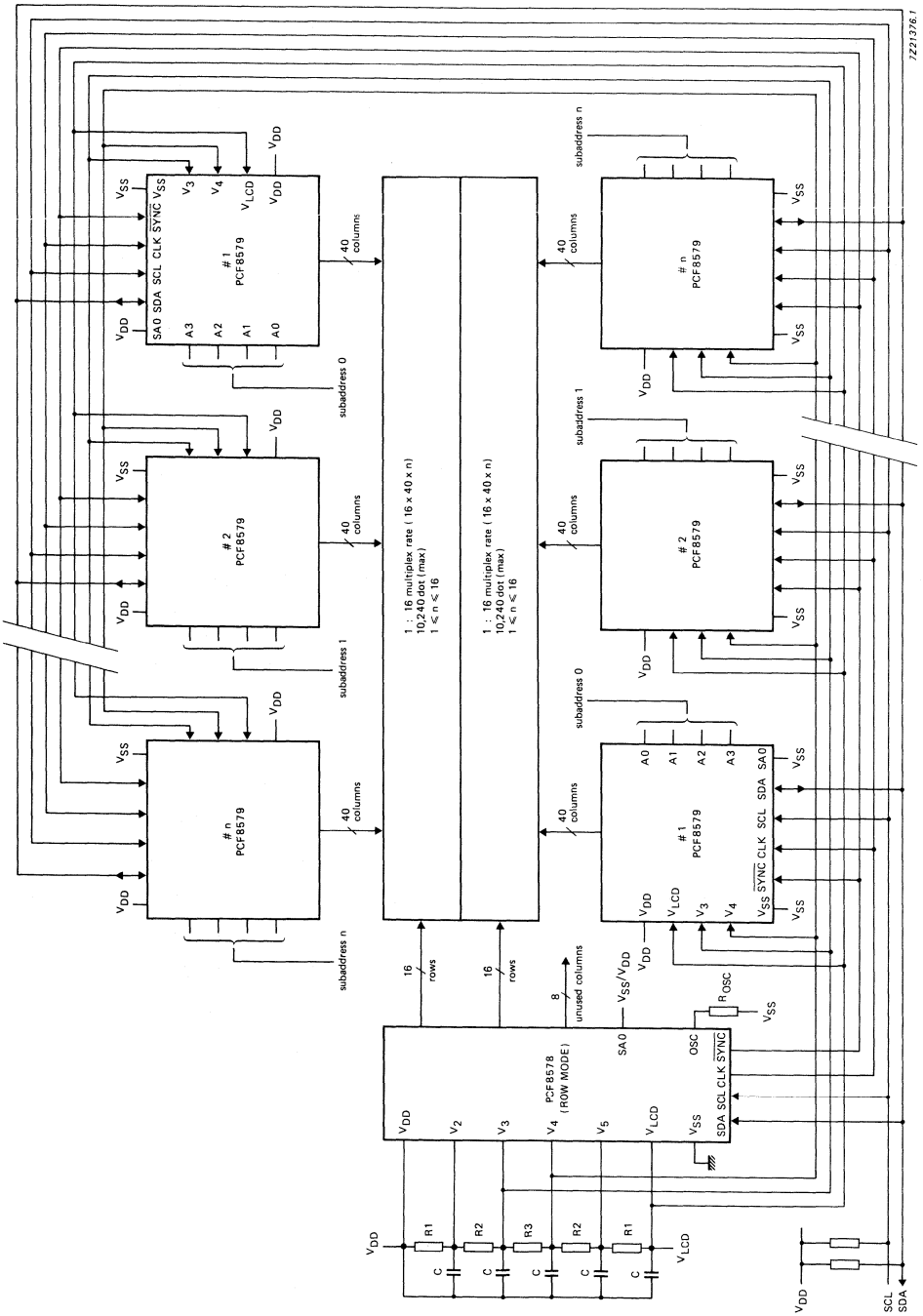


Fig. 3 Example of split screen application with 1 : 16 multiplex rate for improved contrast.

256 × 8-bit STATIC CMOS EEPROM WITH I²C BUS INTERFACE

GENERAL DESCRIPTION

The PCF8582 is a 2K-bit 5 V electrically erasable programmable read only memory (EEPROM) organized as 256 by 8 bits. It is designed in a floating gate CMOS technology.

As data bytes are received and transmitted via the serial I²C bus, an eight pin DIL package is sufficient. Up to eight PCF8582 devices may be connected to the I²C bus.

Chip select is accomplished by three address inputs.

Features

- Non-volatile storage of 2K-bit organized as 256 x 8
- Only one power supply required (5 V)
- On chip voltage multiplier for erase/write
- Serial input/output bus (I²C)
- Automatic word address incrementing
- Low power consumption
- One point erase/write timer
- Power on reset
- 10 000 erase/write cycles per byte
- 10 years non-volatile data retention
- Infinite number of read cycles
- Pin and address compatible to PCF8570, PCF8571 and PCD8572

PACKAGE OUTLINES

PCF8582P: 8-lead DIL; plastic (SOT-97).
PCF8582T: 16-lead mini pack plastic (SO-16L; SOT-162A).

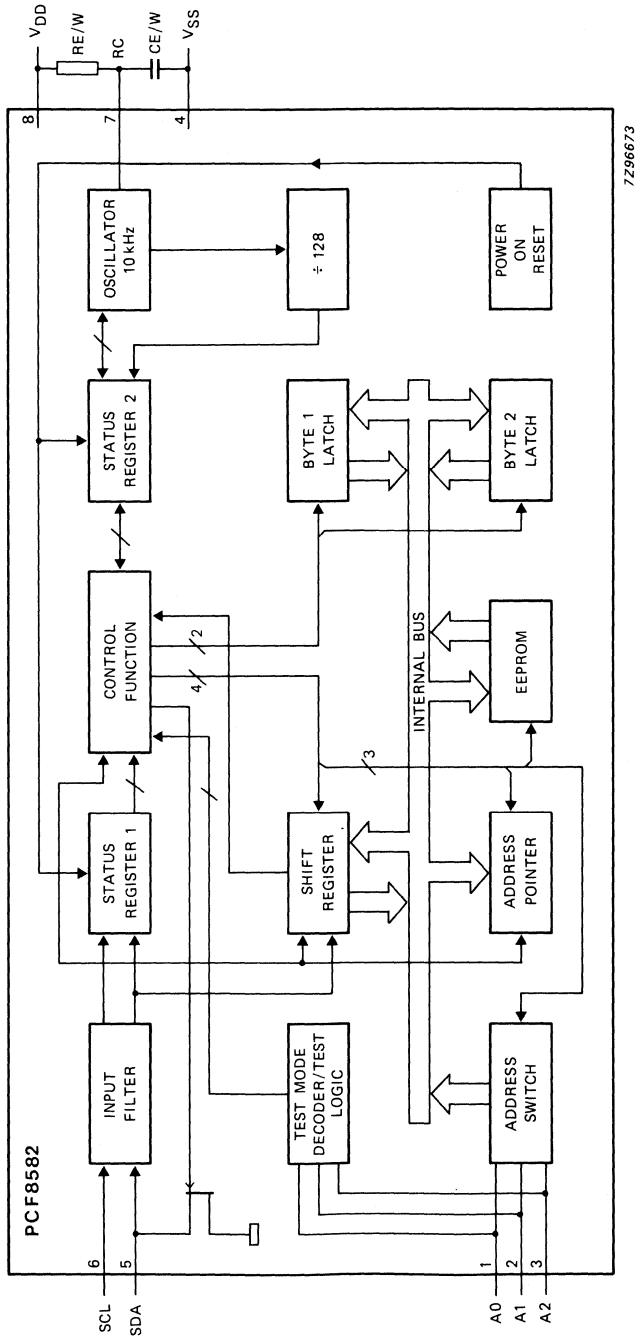


Fig. 1 Block diagram.

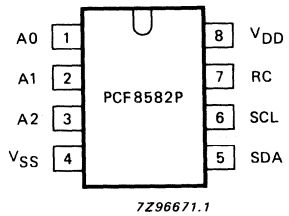


Fig. 2(a) Pinning diagram; PCF8582P.

PINNING

1	A0	
2	A1	address inputs/test
3	A2	mode select
4	V_{SS}	ground
5	SDA	I²C bus lines
6	SCL	
7	RC	input for timer constant
8	V_{DD}	positive supply

DEVELOPMENT DATA

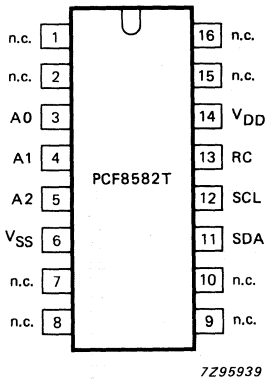


Fig. 2(b) Pinning diagram; PCF8582T.

1	NC	
2	NC	
3	A0	
4	A1	address inputs/test
5	A2	mode select
6	V_{SS}	ground
7	NC	
8	NC	
9	NC	
10	NC	
11	SDA	I²C bus lines
12	SCL	
13	RC	input for timer constant
14	V_{DD}	positive supply
15	NC	
16	NC	

FUNCTIONAL DESCRIPTION

Characteristics of the I^2C bus

The I^2C bus is intended for communication between different ICs. The serial bus consists of two bi-directional lines, one for data signals (SDA), and one for clock signals (SCL). Both the SDA and the SCL lines must be connected to a positive supply voltage via a pull-up resistor.

The following protocol has been defined:
Data transfer may be initiated only when the bus is not busy.
During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH will be interpreted as control signals.

Accordingly, the following bus conditions have been defined:
Bus not busy: both data and clock lines remain HIGH.
Start data transfer: a change in the state of the data line, from HIGH to LOW, while the clock is HIGH defines the start condition.
Stop data transfer: a change in the state of the data line, from LOW to HIGH, while the clock is HIGH, defines the stop condition.
Data valid: the state of the data line represents valid data when, after a start condition, the data line is stable for the duration of the HIGH period of the clock signal. The data on the line may be changed during the LOW period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a start condition and terminated with a stop condition; the number of the data bytes, transfered between the start and stop conditions is limited to two bytes in the ERASE/WRITE mode and unlimited in the READ mode. The information is transmitted in bytes and each receiver acknowledges with a ninth bit.

Within the I^2C bus specifications a low-speed mode (2 kHz clock rate) and a high-speed mode (100 kHz clock rate) are defined. The PCF8582 operates in both modes.
By definition a device that gives out a signal is called a "transmitter", and the device which receives the signal is called a "receiver". The device which controls the signal is called the "master". The devices that are controlled by the master are called "slaves".

Each word of eight bits is followed by one acknowledge bit. This acknowledge bit is a HIGH level put on the bus by the transmitter whereas the master generates an extra acknowledge related clock pulse.
A slave receiver which is addressed is obliged to generate an acknowledge after the reception of each byte.
Also, a master receiver must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter.
The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the high period of the acknowledge related clock pulse.
Set-up-and hold times must be taken into account. A master receiver must signal an end of data to the slave transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this case the transmitter must leave the data line HIGH to enable the master generation of the stop condition.

Note

The general characteristics and detailed specification of the I²C bus is available on request.

I²C bus protocol

The I²C bus configuration for different READ and WRITE cycles of the PCF8582 are shown in Fig. 3.

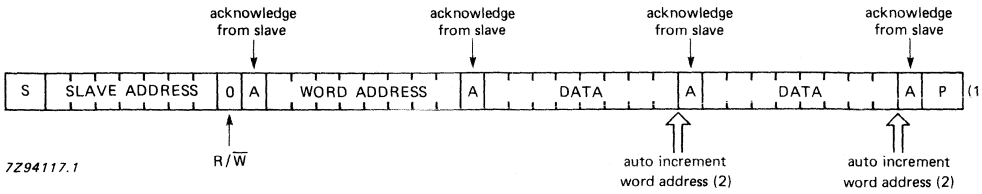


Fig. 3(a) Slave receiver ERASE/WRITE mode.

(1) After this stop condition the erase/write cycle starts and the bus is free for another transmission; the duration of the erase/write cycle is approximatly 30 ms if only one byte is written, and 60 ms, if two bytes are written. During the erase/write cycle the slave receiver does not send an acknowledge bit if addressed via I²C bus.

(2) The second data byte is voluntary. It is not allowed to erase/write more than two bytes.

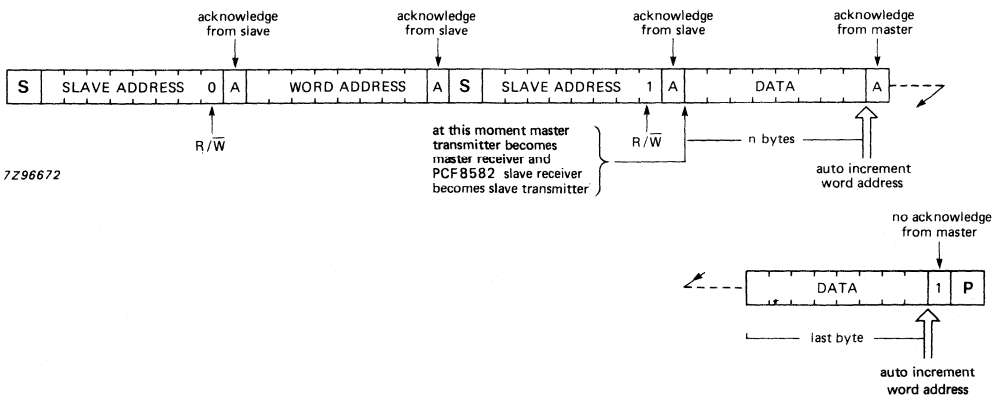


Fig. 3(b) Master reads PCF8582 slave after setting word address. (WRITE word address; READ data).

Note: The slave address is defined in accordance with the I²C bus specification as:

1	0	1	0	A2	A1	A0	R/$\overline{W}$

DEVELOPMENT DATA

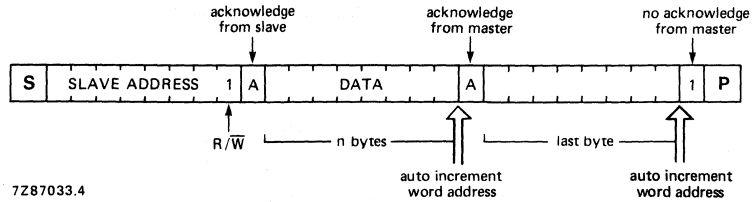


Fig. 3(c) Master reads PCF8582 slave immediately after first byte (READ mode).

I²C bus timing

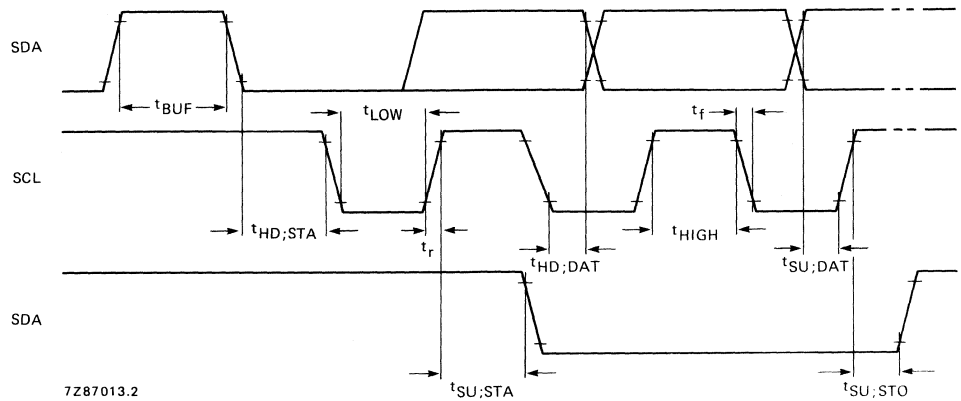


Fig. 4 I²C bus timing.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_{DD}	−0,3 to 7 V
Voltage, on any input pin (input impedance 500 Ω)	V_I	V_{SS}−0,8 to V_{DD} +0,8 V
Operating temperature range	T_{amb}	−40 to +85 °C
Storage temperature range	T_{stg}	−65 to +150 °C
Current into any input pin	I_I	1 mA
Output current	I_O	10 mA

DEVELOPMENT DATA

CHARACTERISTICS

V_{DD} = 5 V; V_{SS} = 0 V; T_{amb} = −40 to + 85 °C; unless otherwise specified.

parameter	symbol	min.	typ.	max.	unit
Operating supply voltage	V_{DD}	4,5	5	5,5	V
Operating supply current, READ (f_{SCL} = 100 kHz; $V_{DD\ max}$)	I_{DDR}	–	–	0,4	mA
Operating supply current, WRITE/ERASE($V_{DD\ max}$)	I_{DDW}	–	–	2,0	mA
Standby supply current ($V_{DD\ max}$)	I_{DDO}	–	–	10	μA
Input SCL and input/output SDA					
Input voltage LOW	V_{IL}	−0,3	–	1,5	V
Input voltage HIGH	V_{IH}	3	–	V_{DD}+0,8	V
Output voltage LOW (I_{OL} = 3 mA, V_{DD} = 4,5 V)	V_{OL}	–	–	0,4	V
Output leakage current HIGH (V_{OH} = V_{DD})	I_{OH}	–	–	1	μA
Input leakage current (A0,A1,A2,SCL), (note 1)	$\pm I_{IN}$	–	–	1	μA
Clock frequency	f_{SCL}	0	–	100	kHz
Input capacity (SCL,SDA)	C_I	–	–	7	pF
Time the bus must be free before a new transmission can start	t_{BUF}	4,7	–	–	μs
Hold time start condition. After this period the first clock pulse is generated	$t_{HD;STA}$	4	–	–	μs
The LOW period of the clock	t_{LOW}	4,7	–	–	μs
The HIGH period of the clock	t_{HIGH}	4	–	–	μs
Set-up time for start condition (only relevent for a repeated start condition)	$t_{SU;STA}$	4,7	–	–	μs
Hold time DATA for:					
I²C bus compatible masters	$t_{HD;DAT}$	5	–	–	μs
I²C devices (note 2)	$t_{HD;DAT}$	200	–	–	ns
Set-up time DATA	$t_{SU;DAT}$	500	–	–	ns
Rise time for both SDA and SCL lines	t_R	–	–	1	μs
Fall time for both SDA and SCL lines	t_F	–	–	300	ns
Set-up time for stop condition	$t_{SU;STO}$	4,7	–	–	μs
Erase/write timer constant (note 3)					
Erase/write cycle time	$t_{E/W}$	20	–	100	ms
Erase/write timing capacitor for erase/write cycle of 30 ms (± 10% tolerance)	$C_{E/W}$	–	3,3	–	nF
Erase/write timing resistor for erase/write cycle of 30 ms (± 5% tolerance)	$R_{E/W}$	–	56	–	kΩ
Data retention time (T_{amb} = +55 °C)	t_S	10	–	–	years

Notes to the characteristics

1. Selection of the chip address is done by connecting the A0, A1, and A2 inputs either to V_{SS} or V_{DD}.
2. A transmitter must internally provide a hold time to bridge the undefined region (maximum 300 ns) of the falling edge of SCL.
3. Endurance (number of erase/write cycles), NE/W, is 10^4 E/W cycles.

CLOCK CALENDAR WITH 256 × 8-BIT STATIC RAM

GENERAL DESCRIPTION

The PCF8583 is a low power 2048-bit static CMOS RAM organized as 256 words by 8-bits. Addresses and data are transferred serially via a two-line bidirectional bus (I^2C). The built-in word address register is incremented automatically after each written or read data byte. One address pin A0 is used for programming the hardware address, allowing the connection of two devices to the bus without additional hardware. The built-in 32,768 kHz oscillator circuit and the first 8 bytes of the RAM are used for the clock/calendar and counter functions. The next 8 bytes may be programmed as alarm registers or used as free RAM space.

Features

- I^2C bus interface operating supply voltage: 2,5 V to 6 V
- Clock operating supply voltage (0 to 70 °C): 1,0 V to 6 V
- Data retention voltage: 1,0 V to 6 V
- Operating current (f_{SCL} = 0 Hz): max. 50 μA
- Clock function with four year calendar
- 24 or 12 hour format
- 32,768 kHz or 50 Hz time base
- Serial input/output bus (I^2C)
- Automatic word address incrementing
- Programmable alarm, timer and interrupt function

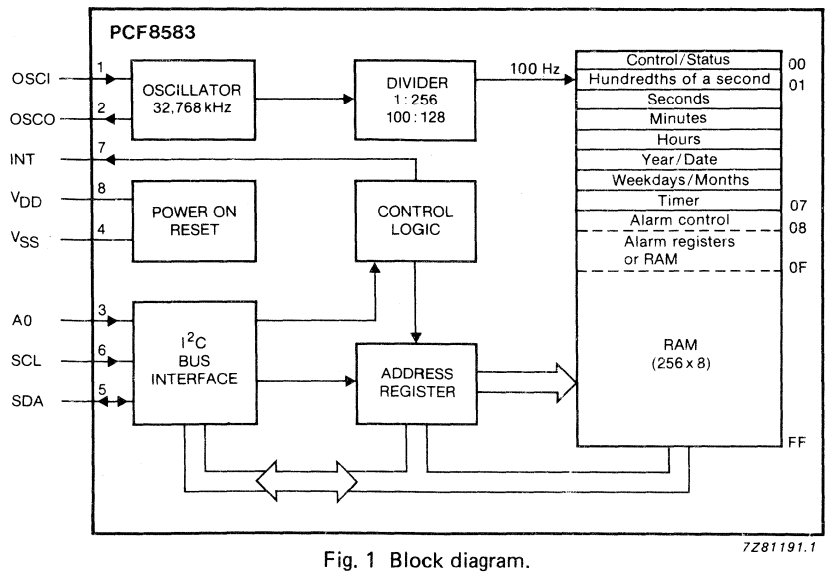


Fig. 1 Block diagram.

PACKAGE OUTLINES

PCF8583P: 8-lead DIL; plastic (SOT-97).
PCF8583T: 8-lead mini-pack; plastic (SO-8L; SOT-176).

PINNING

1	OSCI	oscillator input, 50 Hz or event-pulse input	
2	OSCO	oscillator output	
3	A0	address input	
4	V_{SS}	negative supply	
5	SDA	serial data line	I^2C bus
6	SCL	serial clock line	I^2C bus
7	INT	open drain interrupt output (active low)	
8	V_{DD}	positive supply	

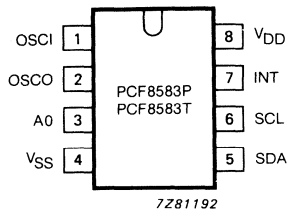


Fig. 2 Pinning diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range (pin 8); note 1	V_{DD}	−0,8 to 8,0	V
Voltage range on any input	V_I	−0,8 to V_{DD} + 0,8	V
DC input current (any input)	I_I	max. 10	mA
DC output current (any output)	I_O	max. 10	mA
Supply current (pin 4 or pin 8)	I_{DD}; I_{SS}	max. 50	mA
Power dissipation per package	P_{tot}	max. 300	mW
Power dissipation per output	P	max. 50	mW
Storage temperature range	T_{stg}	−65 to + 150	°C
Operating ambient temperature range	T_{amb}	−40 to + 85	°C

Note

1. Inputs and outputs are protected against electrostatic discharges in normal handling. However, to be totally safe, it is advised to take handling precautions appropriate to handling MOS devices (see 'Handling MOS devices').

FUNCTIONAL DESCRIPTION

The PCF8583 contains a 256 by 8-bit RAM with an 8-bit auto-increment address register, an on-chip 32,768 kHz oscillator circuit, a frequency divider, a serial two-line bidirectional I^2C bus interface and a power-on reset circuit.

The first 8 bytes of the RAM (memory addresses 00 to 07) are designed as addressable 8-bit parallel registers. The first register (memory address 00) is used as a control/status register. The memory addresses 01 to 07 are used as counters for the clock function. The memory addresses 08 to 0F are free RAM locations or may be programmed as alarm registers.

Counter function modes

When the control/status register is set a 32,768 kHz clock mode, a 50 Hz clock mode or an event-counter mode can be selected.

In the clock modes the hundredths of a second, seconds, minutes, hours, date, month (four year calendar) and weekdays are stored in a BCD format. The timer register stores up to 99 days. The event-counter mode is used to count pulses applied to the oscillator input (OSCO left open). The event counter stores up to 6 digits of data.

When one of the counters is read (memory locations 01 to 07), the contents of all counters are strobed into capture latches at the beginning of a read cycle. Therefore faulty reading of the count during a carry condition is prevented.

Alarm function modes

By setting the alarm enable bit of the control/status register the alarm control register (address 08) is activated.

By setting the alarm control register a dated alarm, a daily alarm, a weekday alarm or a timer alarm may be programmed. In the clock modes, the timer register (address 07) may be programmed to count hundredths of a second, seconds, minutes, hours or days. Days are counted when an alarm is not programmed.

Whenever an alarm event occurs the alarm flag of the control/status register is set. A timer alarm event will set the alarm flag and an overflow condition of the timer will set the timer flag. The open drain interrupt output is switched on (active LOW) when the alarm or timer flag is set (enabled).

When a timer function without any alarm function is programmed the remaining alarm registers (addresses 09 to 0F) may be used as free RAM space.

Control/status register

The control/status register is defined as the memory location 00 with free access for reading and writing via the I^2C bus. All functions and options are controlled by the contents of the control/status register (see Fig. 3).

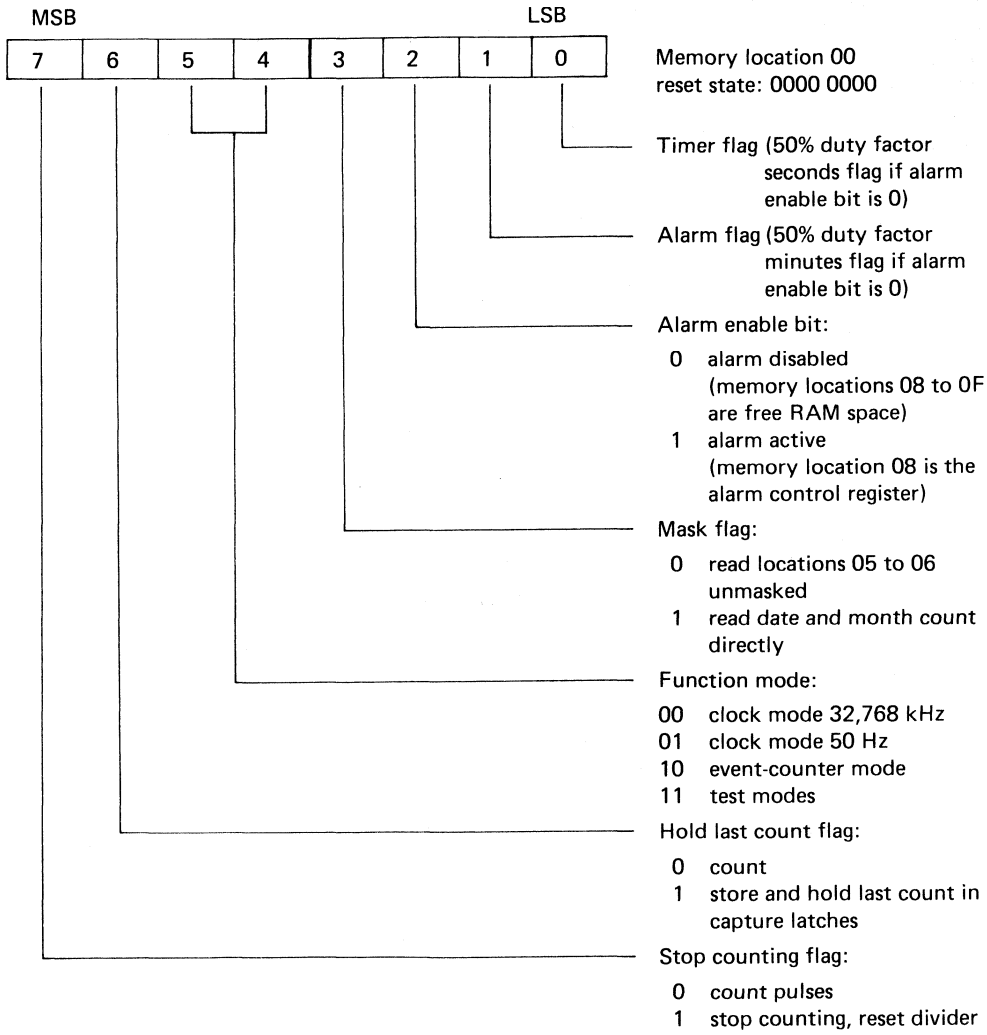


Fig. 3 Control/status register.

Counter registers

In the different modes the counter registers are programmed and arranged as shown in Fig. 4. Counter cycles are listed in Table 1.

In the clock modes 24 h or 12 h format can be selected by setting the most significant bit of the hours counter register. The format of the hours counter is shown in Fig. 5.

The year and date are packed into memory location 05 (see Fig. 6). The weekdays and months are packed into memory location 06 (see Fig. 7). When reading these memory locations the year and weekdays are masked out when the mask flag of the control/status register is set. This allows the user to read the date and month count directly.

In the event-counter mode events are stored in BCD format. D5 is the most significant and D0 the least significant digit. The divider is by-passed.

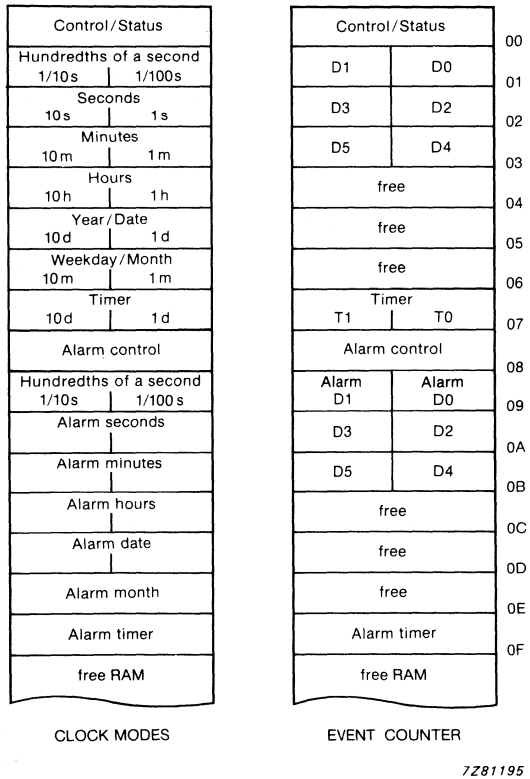
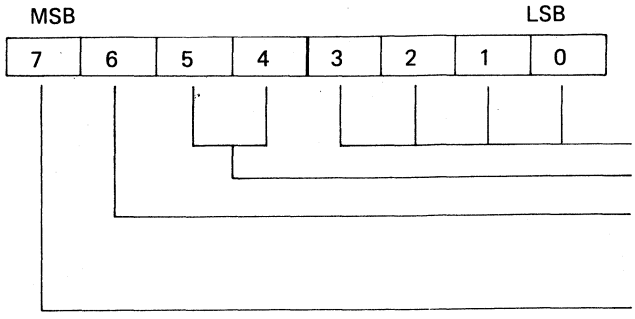


Fig. 4 Register arrangement.

Counter registers (continued)



Memory location 04 (hours counter)
reset state: 0000 0000

Unit hours BCD

Ten hours (0 to 2 binary)

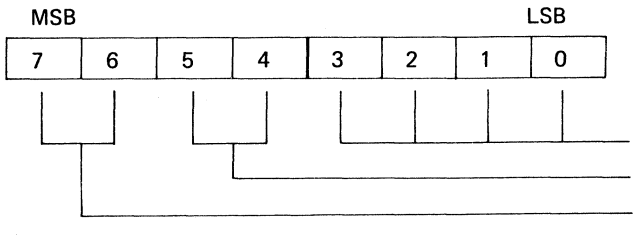
AM/PM flag:

0 AM
1 PM

Format:

0 24 h format, AM/PM flag remains unchanged
1 12 h format, AM/PM flag will be updated

Fig. 5 Format of the hours counter.



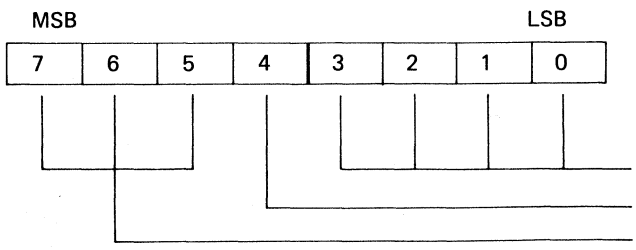
Memory location 05 (year/date)
reset state: 0000 0001

Unit days BCD

Ten days (0 to 3 binary)

Year (0 to 3 binary, read as 0 if the mask flag is set)

Fig. 6 Format of the year/date counter.



Memory location 06 (weekdays/months)
reset state: 0000 0001

Unit months BCD

Ten months

Weekdays (0 to 6 binary, read as 0 if the mask flag is set)

Fig. 7 Format of the weekdays/months counter.

Table 1 Cycle length of the time counters, clock modes

unit	counting cycle	carry to the next unit	contents of the month counter
hundredths of a second	00 to 99	99 to 00	
seconds	00 to 59	59 to 00	
minutes	00 to 59	59 to 00	
hours (24 h)	00 to 23	23 to 00	
hours (12 h)	12 AM, 01 AM to 11 AM, 12 PM, 01 PM to 11 PM	11 PM to 12 AM	
date	01 to 31 01 to 30 01 to 29 01 to 28	31 to 01 30 to 01 29 to 01 28 to 01	1, 3, 5, 7, 8, 10, 12 4, 6, 9, 11 2, year = 0 2, year = 1, 2, 3
months	01 to 12	12 to 01	
year	0 to 3		
weekdays	0 to 6	6 to 0	
timer/days	00 to 99	no carry	

DEVELOPMENT DATA

Alarm control register

When the alarm enable bit of the control/status register is set the alarm control register (address 08) is activated. All alarm, timer and interrupt output functions are controlled by the contents of the alarm control register (see Figs 8a and 8b).

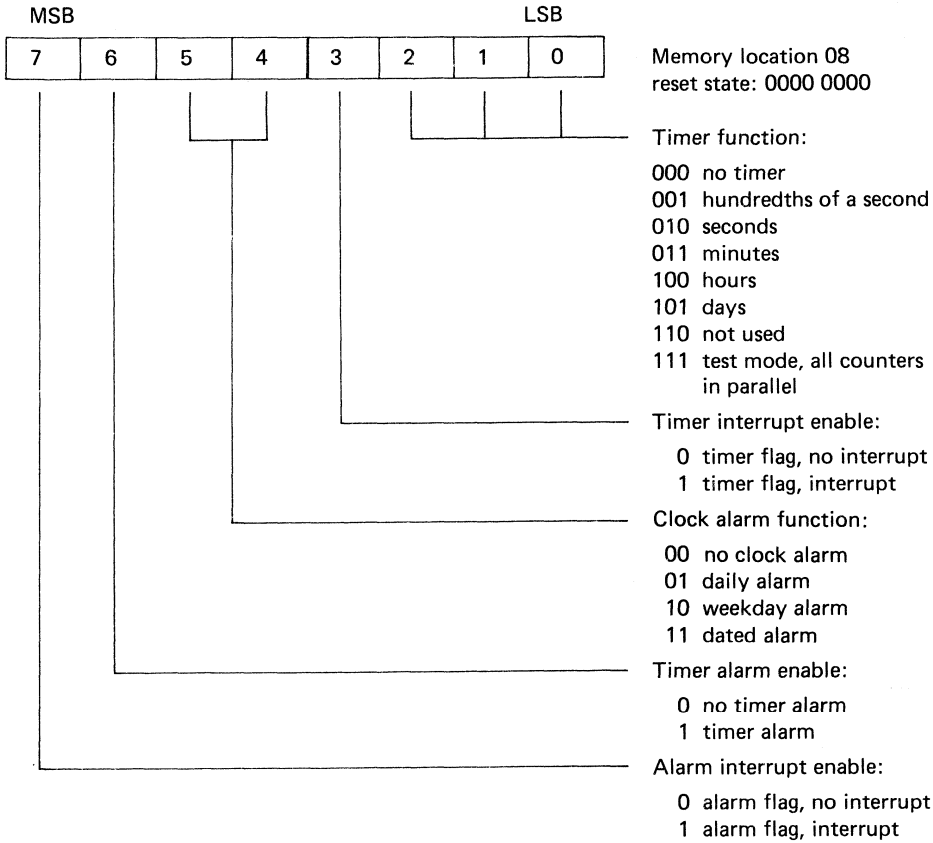


Fig. 8a Alarm control register, clock modes.

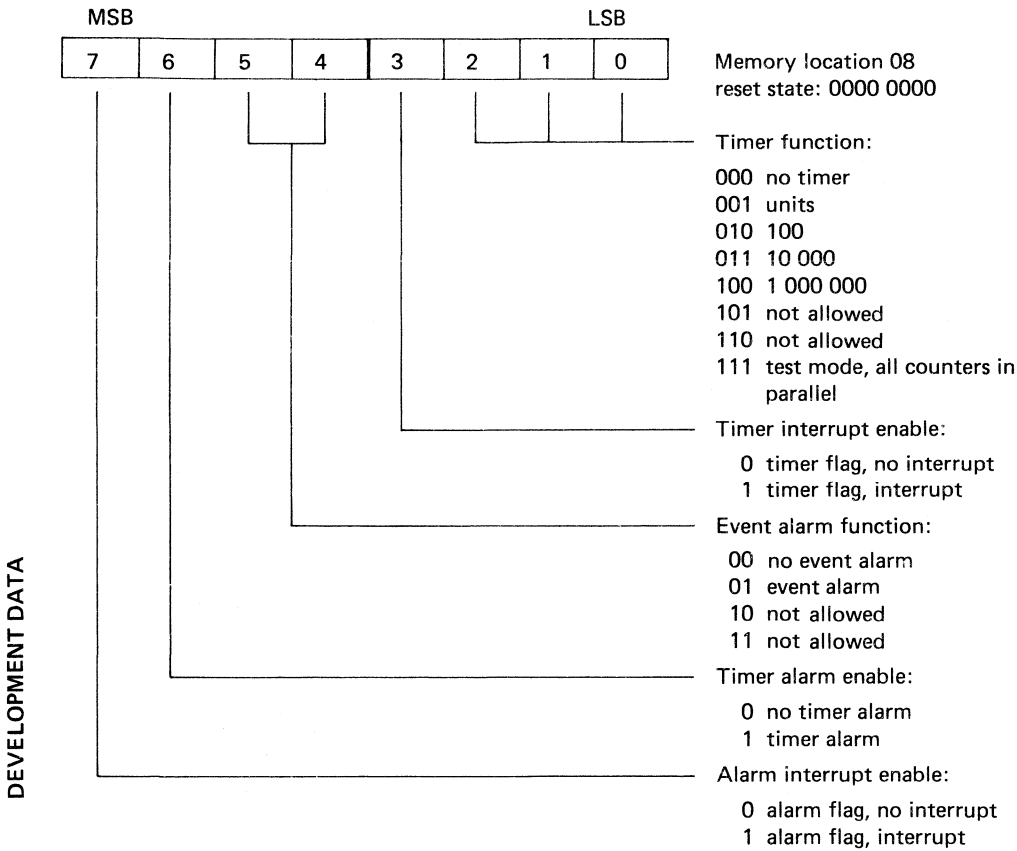


Fig. 8b Alarm control register, event-counter mode.

Alarm registers

All alarm registers are allocated with a constant address offset of hex 08 to the corresponding counter registers.

An alarm goes off when the contents of the alarm registers matches bit-by-bit the contents of the involved counter registers. The year and weekday bits are ignored in a dated alarm. A daily alarm ignores the month and date bits. When a weekday alarm is selected, the contents of the alarm weekday/month register will select the weekdays on which an alarm is activated (see Fig. 9).

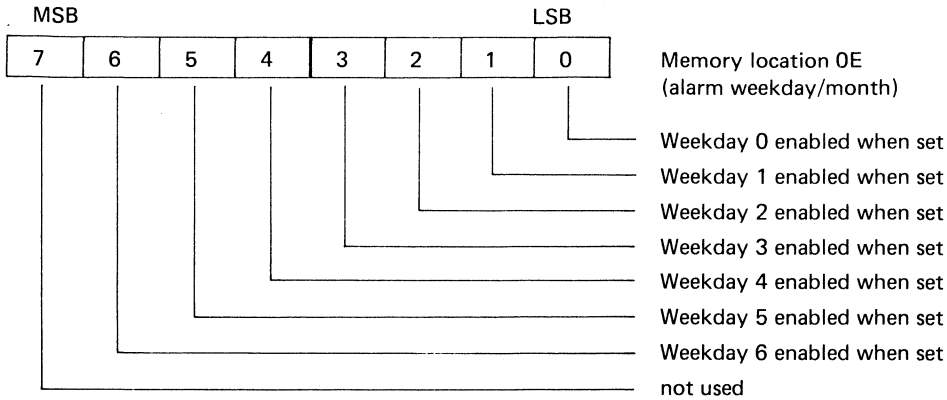


Fig. 9 Selection of alarm weekdays.

Interrupt output

The open-drain n-channel interrupt output is programmed by setting the alarm control register. It is switched on (active LOW) when the alarm flag or the timer flag is set. In the clock mode without alarm the output sequence is controlled by the timer flag. The OFF voltage of the interrupt output may exceed the supply voltage.

Oscillator and divider

A 32,768 kHz quartz crystal has to be connected to OSCI (pin 1) and OSCO (pin 2). A trimmer capacitor between OSCI and V_{DD} is used for tuning the oscillator. The oscillator frequency is scaled down to 128 Hz by the divider. A 100 Hz clock signal is derived from this signal.

In the 50 Hz clock mode or event-counter mode the oscillator is disabled and the oscillator input is switched to a high impedance state. This allows the user to feed the 50 Hz reference frequency or an external high speed event signal into the input OSCI.

Initialization

When power-up occurs the I^2C bus interface, the control/status register and all clock counters are reset. The device starts time keeping in the 32,768 kHz clock mode with the 24 h format on the first of January at 0.00.00: 00.

A second level-sensitive reset signal to the I^2C bus interface is generated as soon as the supply voltage drops below the interface reset level. This reset signal does not affect the control/status or clock counter registers.

It is recommended to set the stop counting flag of the control/status register before loading the actual time into the counters. Loading of illegal states will lead to a clock malfunction but will not latch-up the device.

CHARACTERICS OF THE I²C BUS

The I²C bus is for bidirectional, two-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor. Data transfer may be initiated only when the bus is not busy.

Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as a control signal.

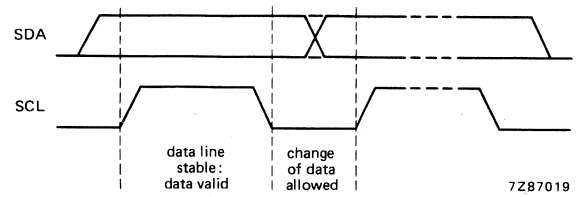


Fig. 10 Bit transfer.

Start and stop conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH, is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH, is defined as the stop condition (P).

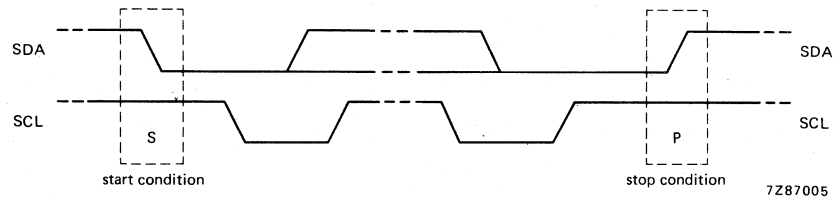


Fig. 11 Definition of start and stop condition.

System configuration

A device generating a message is a "transmitter", a device receiving a message is the "receiver". The device that controls the message is the "master" and the devices which are controlled by the master are the "slaves".

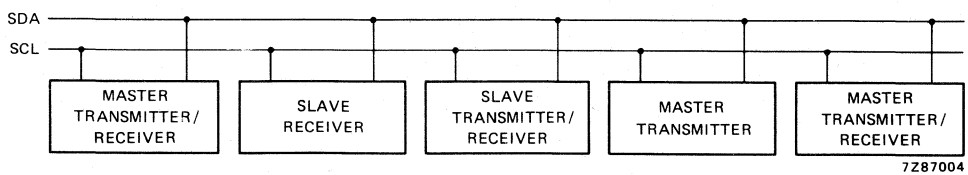


Fig. 12 System configuration.

Acknowledge

The number of data bytes transferred between the start and stop conditions from transmitter to receiver is not limited. Each data byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter whereas the master also generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledge has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse. A master receiver must signal an end of data to the transmitter by *not* generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

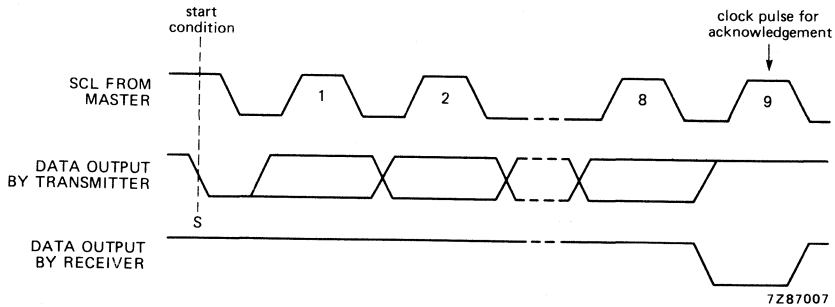


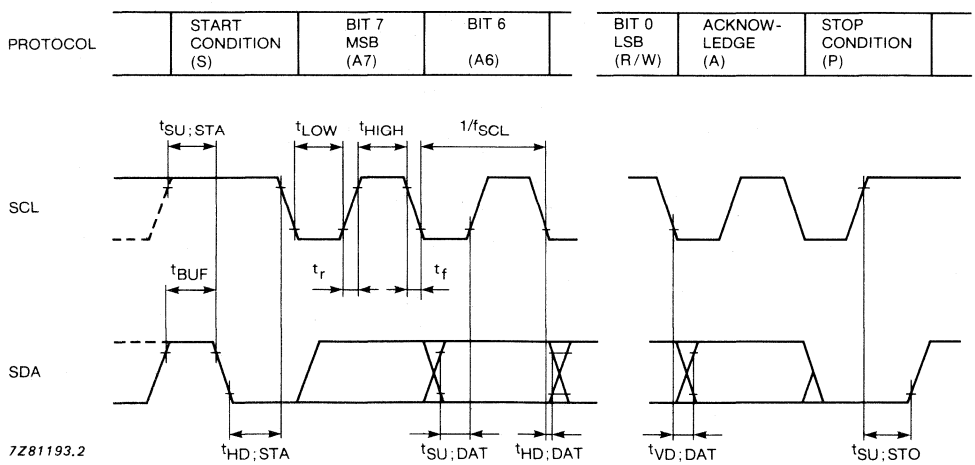
Fig. 13 Acknowledgement on the I^2C bus.

DEVELOPMENT DATA

Timing specifications

All the timing values are valid within the operating supply voltage and ambient temperature range and refer to V_{IL} and V_{IH} with an input voltage swing of V_{SS} to V_{DD}.

parameter	symbol	min.	typ.	max.	unit
SCL clock frequency	f_{SCL}	–	–	100	kHz
Tolerable spike width on bus	t_{SW}	–	–	100	ns
Bus free time	t_{BUF}	4,0	–	–	μs
Start condition set-up time	$t_{SU;STA}$	4,0	–	–	μs
Start condition hold time	$t_{HD;STA}$	4,7	–	–	μs
SCL LOW time	t_{LOW}	4,7	–	–	μs
SCL HIGH time	t_{HIGH}	4,0	–	–	μs
SCL and SDA rise time	t_r	–	–	1,0	μs
SCL and SDA fall time	t_f	–	–	0,3	μs
Data set-up time	$t_{SU;DAT}$	250	–	–	ns
Data hold time	$t_{HD;DAT}$	0	–	–	ns
SCL LOW to data out valid	$t_{VD;DAT}$	–	–	3,4	μs
Stop condition set-up time	$t_{SU;STO}$	4,0	–	–	μs



I²C bus protocol

Before any data is transmitted on the I²C bus, the device which should respond is addressed first. The addressing is always done with the first byte transmitted after the start procedure. The I²C bus configuration for the different PCF8583 READ and WRITE cycles is shown in Fig. 15.

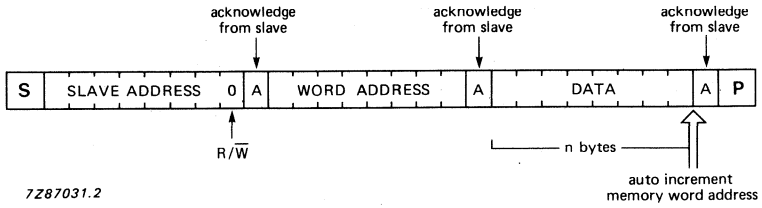


Fig. 15a Master transmits to slave receiver (WRITE mode).

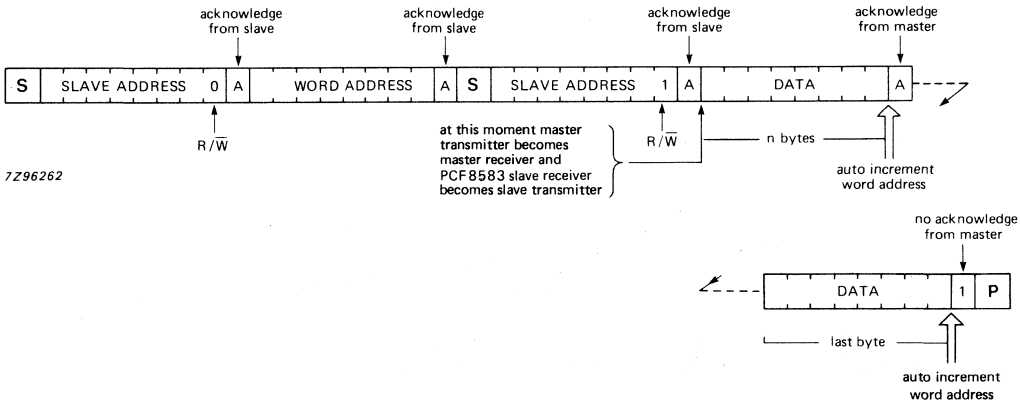


Fig. 15b Master reads after setting word address (WRITE word address; READ data).

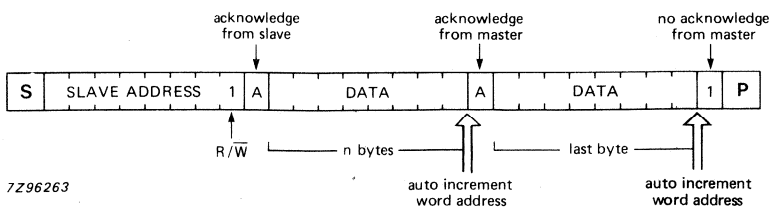


Fig. 15c Master reads slave immediately after first byte (READ mode).

DEVELOPMENT DATA

CHARACTERISTICS

V_{DD} = 2,0 to 6,0 V; V_{SS} = 0 V; T_{amb} = –40 to + 85 °C unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply					
Supply voltage (operating)	V_{DD}	2,5	–	6	V
Supply voltage (clock)	V_{DD}	1,0	–	6	V
Supply current					
T_{amb} = 0 to 70 °C operating at f_{SCL} = 100 kHz	I_{DD}	–	–	200	μA
Clock at V_{DD} = 5 V	I_{DDO}	–	10	50	μA
Clock at V_{DD} = 1 V	I_{DDO}	–	2	10	μA
Power-on reset voltage level (note 1)	V_{POR}	1,5	1,9	2,3	V
Inputs; input/output SDA					
Input voltage LOW (note 2)	V_{IL}	–0,8	–	0,3 x V_{DD}	V
Input voltage HIGH (note 2)	V_{IH}	0,7 x V_{DD}	–	V_{DD} + 0,8	V
Output current LOW at V_{OL} = 0,4 V	I_{OL}	3	–	–	mA
Output leakage current HIGH at V_{OH} = V_{DD}	I_{OH}	–	–	250	nA
Input leakage current at V_I = V_{DD} or V_{SS}	± I_I	–	–	250	nA
Input capacitance (SCL, SDA) at V_I = V_{SS}	C_I	–	–	7	pF
LOW V_{DD} data retention					
Supply voltage for data retention	V_{DDR}	1	–	6	V
Supply current at V_{DDR} = 1 V (note 3)	I_{DDR}	–	–	5	μA
Supply current at V_{DDR} = 1 V; T_{amb} = –25 to + 70 °C (note 3)	I_{DDR}	–	–	2	μA
Oscillator					
Integrated oscillator capacitance	C_{OSC}	–	40	–	pF
Oscillator stability for: ΔV_{DD} = 100 mV at V_{DD} = 1,5 V; T_{amb} = 25 °C	f/f_{OSC}	–	2×10^{-6}	–	–

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Quartz crystal parameters					
Frequency = 32,768 kHz					
Series resistance	R_S	–	–	40	KΩ
Parallel capacitance	C_L	–	9	–	pF
Trimmer capacitance	C_T	5	–	25	pF

Notes to characteristics

1. The power-on reset circuit resets the I^2C bus logic when $V_{DD} < V_{POR}$.
2. When the voltages are a diode voltage above or below the supply voltage V_{DD} or V_{SS} an input current will flow; this current must not exceed ± 0,5 mA.
3. Event or 50 Hz mode only (no Quartz).

APPLICATION INFORMATION

The PCF8583 slave address has a fixed combination 1010 as group 1.

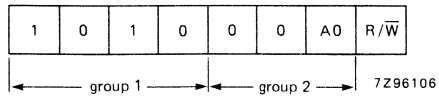


Fig. 16 PCF8583 address.

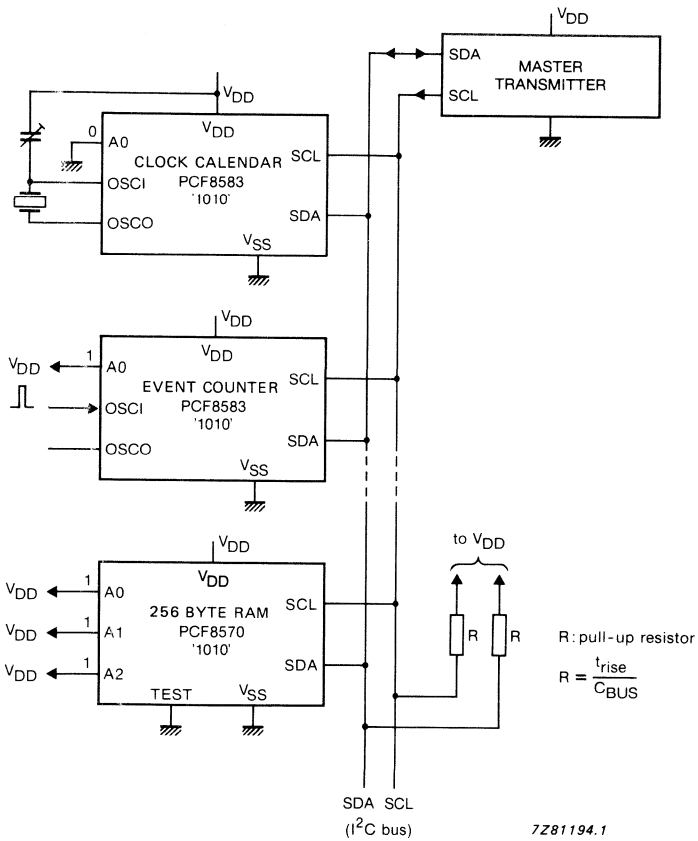


Fig. 17 PCF8583 application diagram.

DEVELOPMENT DATA

8-BIT A/D AND D/A CONVERTER

GENERAL DESCRIPTION

The PCF8591 is a single chip, single supply low power 8-bit CMOS data acquisition device with four analogue inputs, one analogue output and a serial I^2C bus interface. Three address pins A0, A1 and A2 are used for programming the hardware address, allowing the use of up to eight devices connected to the I^2C bus without additional hardware. Address, control and data to and from the device are transferred serially via the two-line bidirectional bus (I^2C).

The functions of the device include analogue input multiplexing, on-chip track and hold function, 8-bit analogue-to-digital conversion and an 8-bit digital-to-analogue conversion. The maximum conversion rate is given by the maximum speed of the I^2C bus.

FEATURES

- Single power supply
- Operating supply voltage 2,5 V to 6 V
- Low standby current
- Serial input/output via I^2C bus
- Address by 3 hardware address pins
- Sampling rate given by I^2C bus speed
- 4 analogue inputs programmable as single-ended or differential inputs
- Auto-incremented channel selection
- Analogue voltage range from V_{SS} to V_{DD}
- On-chip track and hold circuit
- 8-bit successive approximation A/D conversion
- Multiplying DAC with one analogue output

APPLICATIONS

Closed loop control systems; low power converter for remote data acquisition; battery operated equipment; acquisition of analogue values in automotive, audio and TV applications.

PACKAGE OUTLINES

PCF8591P: 16-lead DIL; plastic (SOT-38).
PCF8591T: 16-lead mini-pack; plastic (SO-16L; SOT-162A).

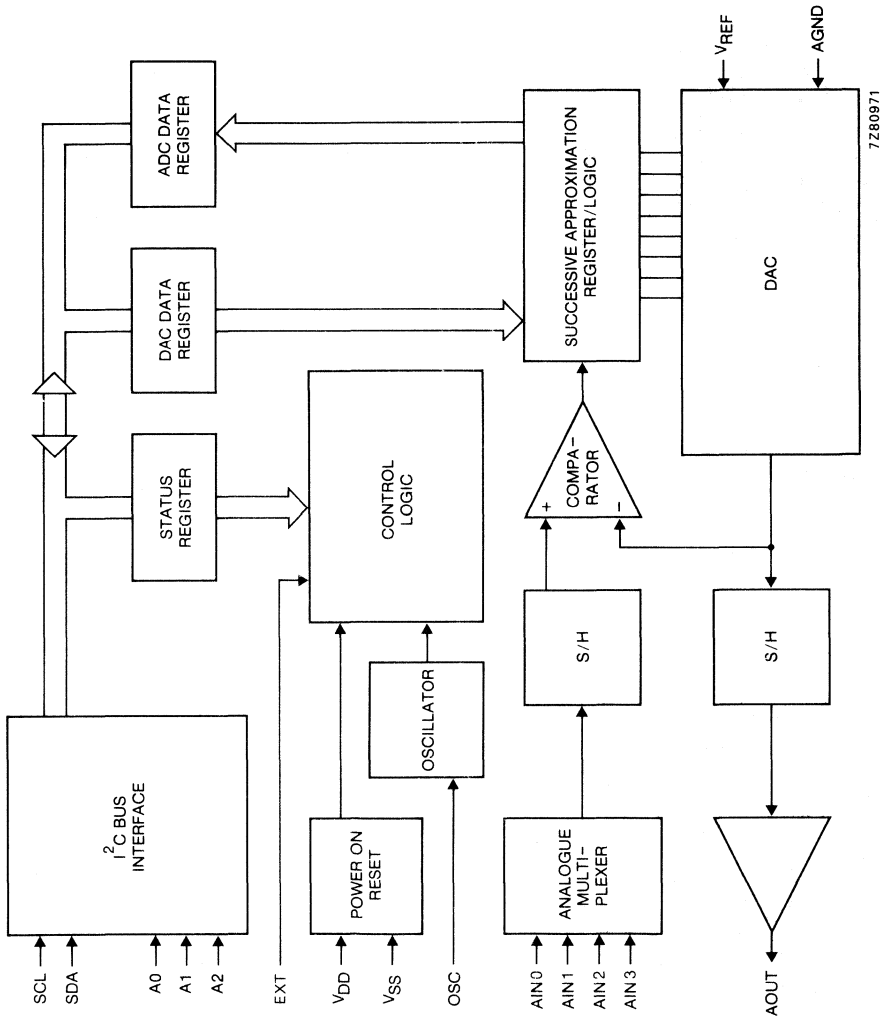


Fig. 1 Block diagram.

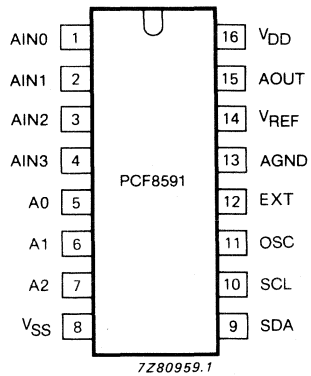


Fig. 2 Pinning diagram.

PINNING

1.	AIN0	analogue inputs (A/D converter)
2.	AIN1	
3.	AIN2	
4.	AIN3	
5.	A0	hardware address
6.	A1	
7.	A2	
8.	V_{SS}	negative supply voltage
9.	SDA	I^2C bus data input/output
10.	SCL	I^2C bus clock input/output
11.	OSC	oscillator input/output
12.	EXT	external/internal switch for oscillator input
13.	AGND	analogue ground
14.	V_{REF}	voltage reference input
15.	AOUT	analogue output (D/A converter)
16	V_{DD}	positive supply voltage

FUNCTIONAL DESCRIPTION

DEVELOPMENT DATA

Adressing

Each PCF8591 device in an I^2C bus system is activated by sending a valid address to the device. The address consists of a fixed part and a programmable part. The programmable part must be set according to the address pins A0, A1 and A2. The address always has to be sent as the first byte after the start condition in the I^2C bus protocol. The last bit of the address byte is the read/write-bit which sets the direction of the following data transfer (see Figs 3 and 10).

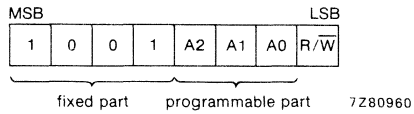


Fig. 3 Address byte.

Control byte

The second byte sent to a PCF8591 device will be stored in its control register and is required to control the device function.

The upper nibble of the control register is used for enabling the analogue output, and for programming the analogue inputs as single-ended or differential inputs. The lower nibble selects one of the analogue input channels defined by the upper nibble (see Fig. 4). If the auto-increment flag is set the channel number is incremented automatically after each A/D conversion.

The selection of a non-existing input channel results in the highest available channel number being allocated. Therefore, if the auto-increment flag is set, the next selected channel will be always channel 0. The most significant bits of both nibbles are reserved for future functions and have to be set to 0. After a power-on reset condition all bits of the control register are reset to 0. The D/A converter and the oscillator are disabled for power saving. The analogue output is switched to a high impedance state.

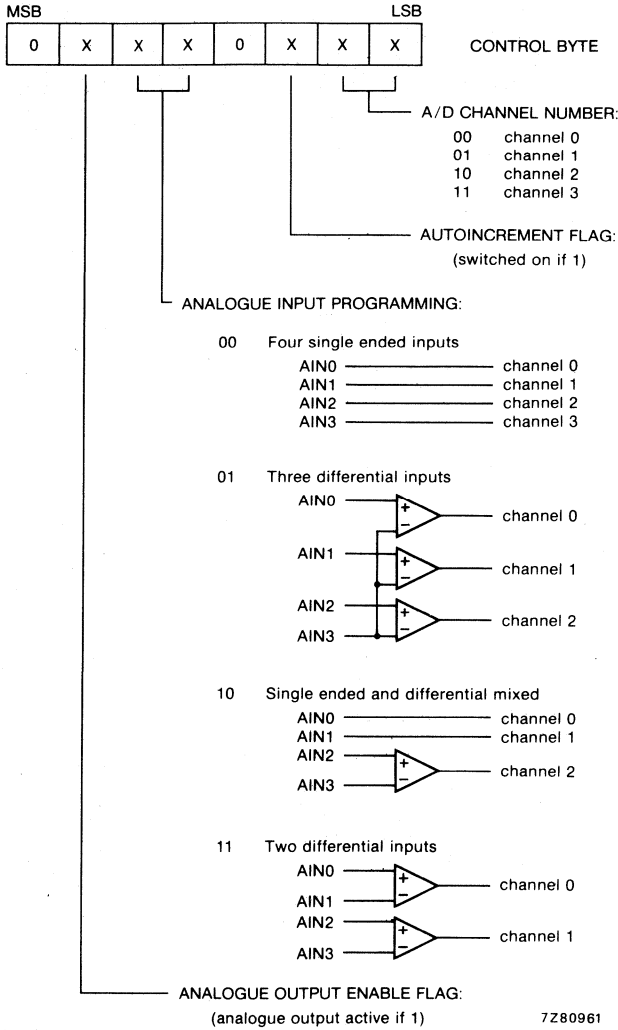


Fig. 4 Control byte.

D/A conversion

The third byte sent to a PCF8591 device is stored in the DAC data register and is converted to the corresponding analogue voltage using the on-chip D/A converter. This D/A converter consists of a resistor divider chain connected to the external reference voltage with 256 taps and selection switches. The tap-decoder switches one of these taps to the DAC output line (see Fig. 5).

The analogue output voltage is buffered by an auto-zeroed unity gain amplifier. This buffer amplifier may be switched on or off by setting the analogue output enable flag of the control register. In the active state the output voltage is held until a further data byte is sent.

The on-chip D/A converter is also used for successive approximation A/D conversion. In order to release the DAC for an A/D conversion cycle the unity gain amplifier is equipped with a track and hold circuit. This circuit holds the output voltage while executing the A/D conversion.

The output voltage supplied to the analogue output AOUT is given by the formula shown in Fig. 6. The waveforms of a D/A conversion sequence are shown in Fig. 7.

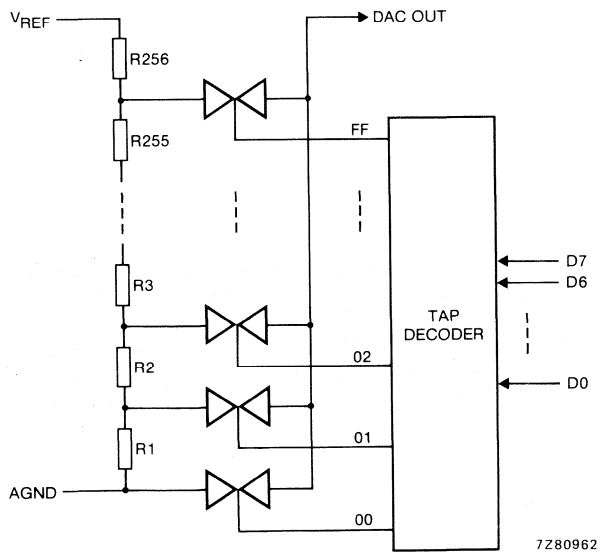


Fig. 5 DAC resistor divider chain.

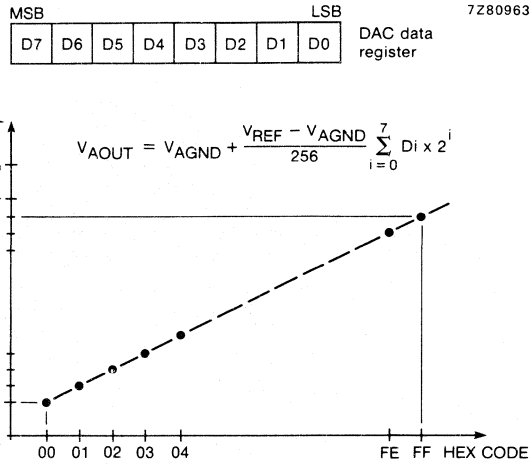


Fig. 6 DAC data and d.c. conversion characteristics.

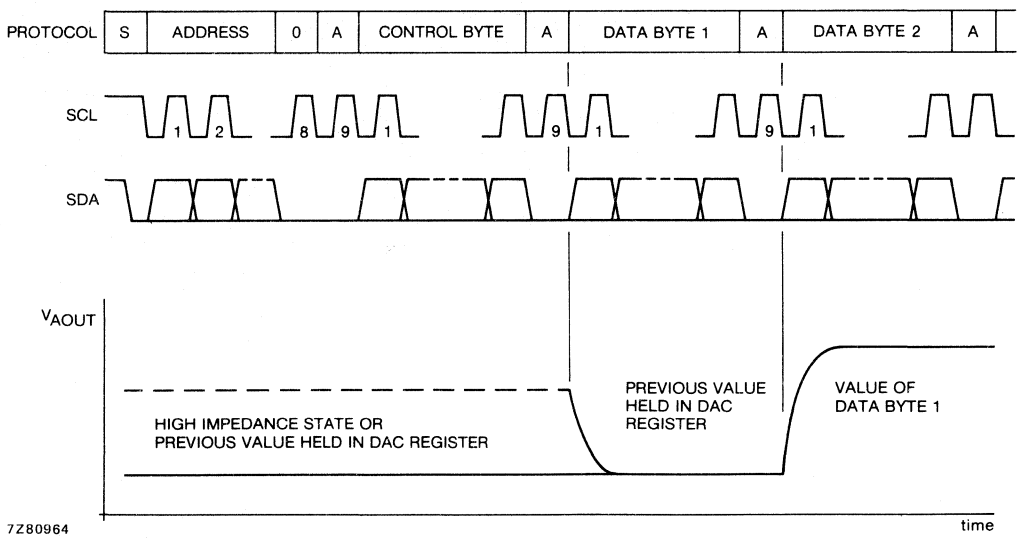


Fig. 7 D/A conversion sequence.

A/D conversion

The A/D converter makes use of the successive approximation conversion technique. The on-chip D/A converter and a high gain comparator are used temporarily during an A/D conversion cycle.

An A/D conversion cycle is always started after sending a valid read mode address to a PCF8591 device. The A/D conversion cycle is triggered at the trailing edge of the acknowledge clock pulse and is executed while transmitting the result of the previous conversion (see Fig. 8).

Once a conversion cycle is triggered an input voltage sample of the selected channel is stored on the chip and is converted to the corresponding 8-bit binary code. Samples picked up from differential inputs are converted to an 8-bit two's complement code (see Fig. 9). The conversion result is stored in the ADC data register and awaits transmission. If the auto-increment flag is set the next channel is selected.

The first byte transmitted in a read cycle contains the conversion result code of the previous read cycle. After a power-on reset condition the first byte read is a hexadecimal 80. The protocol of an I^2C bus read cycle is shown in Fig. 10.

The maximum A/D conversion rate is given by the actual speed of the I^2C bus.

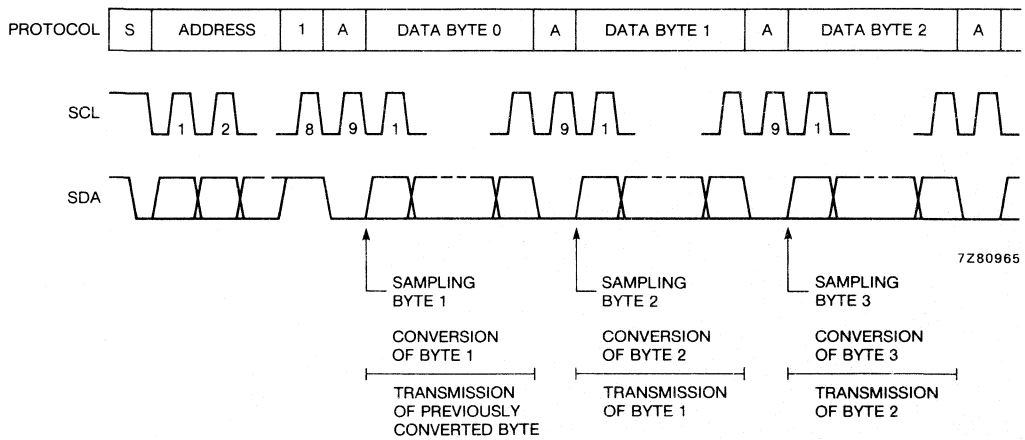


Fig. 8 A/D conversion sequence.

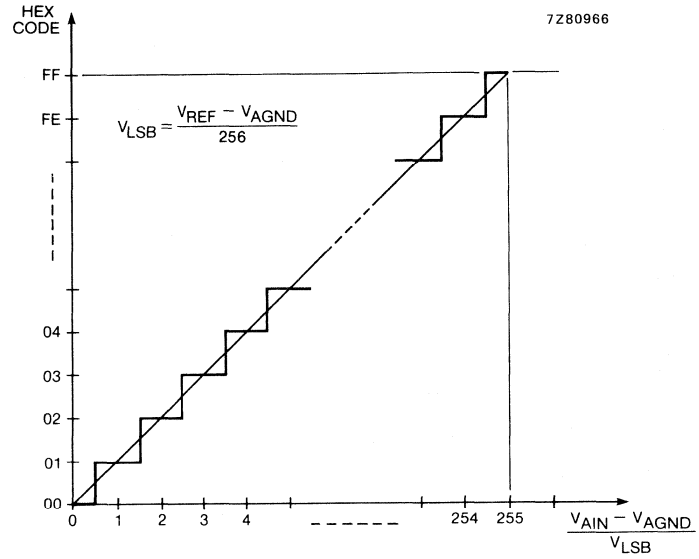


Fig. 9a A/D conversion characteristics of single-ended inputs.

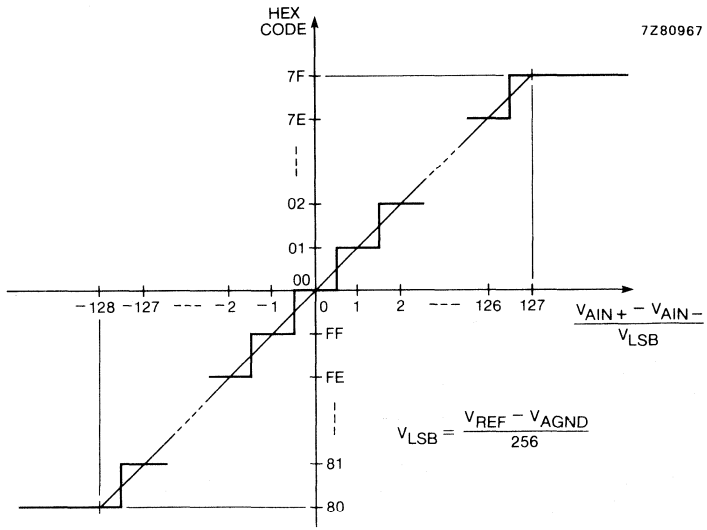


Fig. 9b A/D conversion characteristics of differential inputs.

Reference voltage

For the D/A and A/D conversion either a stable external voltage reference or the supply voltage has to be applied to the resistor divider chain (pins V_{REF} and AGND). The AGND pin has to be connected to the system analogue ground and may have a d.c. off-set with reference to V_{SS}.

A low frequency may be applied to the V_{REF} and AGND pins. This allows the use of the D/A converter as a one-quadrant multiplier; see Application Information and Fig. 6.

The A/D converter may also be used as a one or two quadrant analogue divider. The analogue input voltage is divided by the reference voltage. The result is converted to a binary code. In this application the user has to keep the reference voltage stable during the conversion cycle.

Oscillator

An on-chip oscillator generates the clock signal required for the A/D conversion cycle and for refreshing the auto-zeroed buffer amplifier. When using this oscillator the EXT pin has to be connected to V_{SS}. At the OSC pin the oscillator frequency is available.

If the EXT pin is connected to V_{DD} the oscillator output OSC is switched to a high impedance state allowing the user to feed an external clock signal to OSC.

Bus protocol

After a start condition a valid hardware address has to be sent to a PCF8591 device. The read/write bit defines the direction of the following single or multiple byte data transfer. For the format and the timing of the start condition (S), the stop condition (P) and the acknowledge bit (A) refer to the I^2C bus characteristics. In the write mode a data transfer is terminated by sending either a stop condition or the start condition of the next data transfer.

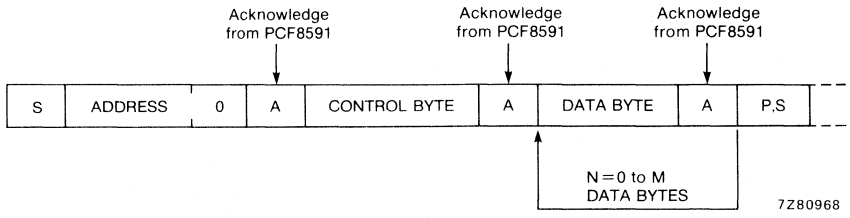


Fig. 10a Bus protocol for write mode, D/A conversion.

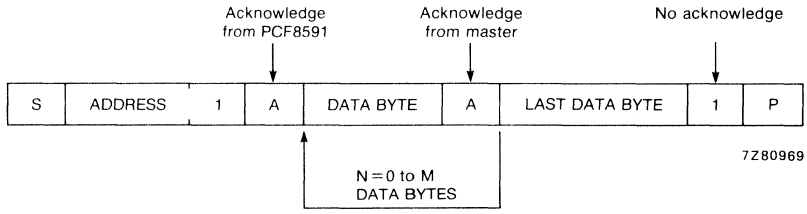


Fig. 10b Bus protocol for read mode, A/D conversion.

CHARACTERICS OF THE I²C BUS

The I²C bus is for bidirectional, two-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor. Data transfer may be initiated only when the bus is not busy.

Bit transfer

One data bit is transfered during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as a control signal.

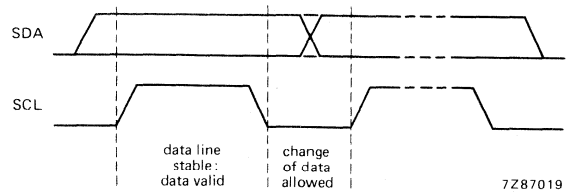


Fig. 11 Bit transfer.

Start and stop conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH, is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH, is defined as the stop condition (P).

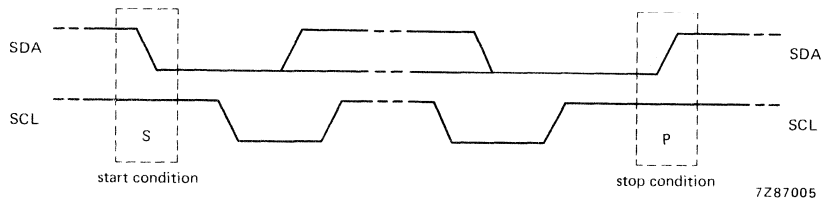


Fig. 12 Definition of start and stop condition.

System configuration

A device generating a message is a "transmitter", a device receiving a message is the "receiver". The device that controls the message is the "master" and the devices which are controlled by the master are the "slaves".

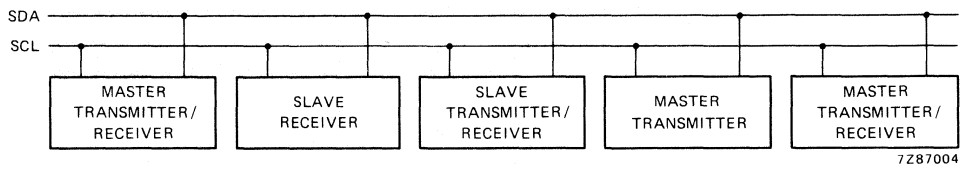


Fig. 13 System configuration.

Acknowledge.

The number of data bytes transfered between the start and stop conditions from transmitter to receiver is not limited. Each data byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter whereas the master also generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse. A master receiver must signal an end of data to the transmitter by *not* generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

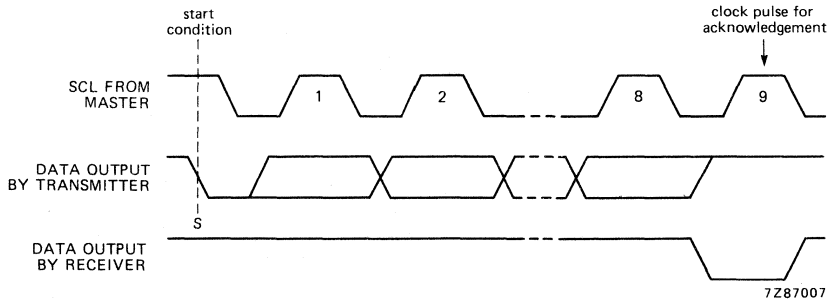


Fig. 14 Acknowledgement on the I^2C bus.

DEVELOPMENT DATA

Timing specifications

All the timing values are valid within the operating supply voltage and ambient temperature range and refer to V_{IL} and V_{IH} with an input voltage swing of V_{SS} to V_{DD}.

parameter	symbol	min.	typ.	max.	unit
SCL clock frequency	f_{SCL}	–	–	100	kHz
Tolerable spike width on bus	t_{SW}	–	–	100	ns
Bus free time	t_{BUF}	4,0	–	–	μs
Start condition set-up time	$t_{SU;STA}$	4,0	–	–	μs
Start condition hold time	$t_{HD;STA}$	4,7	–	–	μs
SCL LOW time	t_{LOW}	4,7	–	–	μs
SCL HIGH time	t_{HIGH}	4,0	–	–	μs
SCL and SDA rise time	t_R	–	–	1,0	μs
SCL and SDA fall time	t_F	–	–	0,3	μs
Data set-up time	$t_{SU;DAT}$	250	–	–	ns
Data hold time	$t_{HD;DAT}$	0	–	–	ns
SCL LOW to data out valid	$t_{VD;DAT}$	–	–	3,4	μs
Stop condition set-up time	$t_{SU;STO}$	4,0	–	–	μs

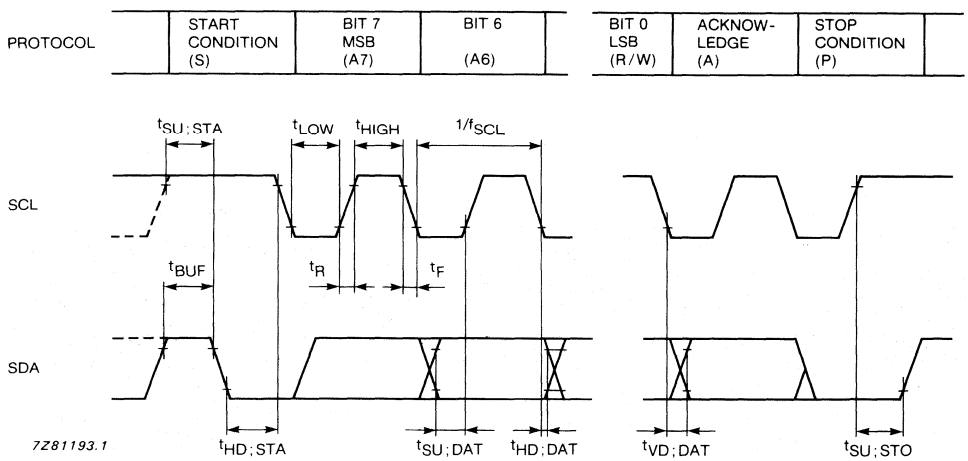


Fig. 15 I²C bus timing diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range	V_{DD}		−0,5 to +8,0 V
Voltage on any pin	V_I		−0,5 to V_{DD} +0,5 V
Input current d.c.	I_I	max.	10 mA
Output current d.c.	I_O	max.	20 mA
V_{DD} or V_{SS} current	I_{DD}, I_{SS}	max.	50 mA
Power dissipation per package	P_{tot}	max.	300 mW
Power dissipation per output	P	max.	100 mW
Storage temperature range	T_{stg}		−65 to +150 °C
Operating ambient temperature range	T_{amb}		−40 to +85 °C

Note:

Inputs and outputs are protected against electrostatic discharges in normal handling. However, to be totally safe, it is advised to take handling precautions appropriate to handling MOS devices (see 'Handling MOS devices').

CHARACTERISTICS

V_{DD} = 2,5 V to 6 V; V_{SS} = 0 V; T_{amb} = −40 °C to +85 °C unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage	operating	V_{DD}	2,5	–	6,0	V
Supply current	standby V_I = V_{SS} or V_{DD}; no load	I_{DD0}	–	1	15	μA
Supply current	operating; AOUT off; f_{SCL} = 100 kHz	I_{DD1}	–	125	250	μA
Supply current	AOUT active; f_{SCL} = 100 kHz	I_{DD2}	–	0,45	1,0	mA
Power-on reset level	note 1	V_{POR}	0,8	–	2,0	V
Digital inputs/output	SCL, SDA, A0, A1, A2					
Input voltage	LOW	V_{IL}	0	–	0,3 x V_{DD}	V
Input voltage	HIGH	V_{IH}	0,7 x V_{DD}	–	V_{DD}	V
Input current	leakage; V_I = V_{SS} to V_{DD}	I_I	–	–	250	nA
Input capacitance		C_I	–	–	5	pF
SDA output current	leakage; HIGH at V_{OH} = V_{DD}	I_{OH}	–	–	250	nA
SDA output current	LOW at V_{OL} = 0,4 V	I_{OL}	3,0	–	–	mA

parameter	conditions	symbol	min.	typ.	max.	unit
Reference voltage inputs	V_{REF}, AGND					
Voltage range	reference	V_{REF}	V_{AGND}	–	V_{DD}	V
Voltage range	analogue ground	V_{AGND}	V_{SS}	–	V_{REF}	V
Input current	leakage	I_I	–	–	250	nA
Input resistance	V_{REF} to AGND	R_{REF}	–	100	–	kΩ
Oscillator	OSC, EXT					
Input current	leakage	I_I	–	–	250	nA
Oscillator frequency		f_{OSC}	0,75	–	1,25	MHz

D/A CHARACTERISTICS

V_{DD} = 5,0 V; V_{SS} = 0 V; V_{REF} = 5,0 V; V_{AGND} = 0 V; R_{load} = 10 kΩ; C_{load} = 100 pF; T_{amb} = −40 °C to +85 °C unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Analogue output						
Output voltage range	no resistive load	V_{OA}	V_{SS}	–	V_{DD}	V
Output voltage range	R_{load} = 10 kΩ	V_{OA}	V_{SS}	–	0,9xV_{DD}	V
Output current	leakage; AOUT disabled	I_{LO}	–	–	250	nA
Accuracy						
Offset error	T_{amb} = 25 °C	OS_e	–	–	50	mV
Linearity error		L_e	–	–	±1,5	LSB
Gain error	no resistive load	G_e	–	–	1	%
Settling time	to ½ LSB full scale step	t_{DAC}	–	–	90	μs
Conversion rate		f_{DAC}	–	–	11,1	kHz
Supply noise rejection	at f = 100 Hz; V_{DD} = 0,1 V_{PP}	SNRR	–	40	–	dB

DEVELOPMENT DATA

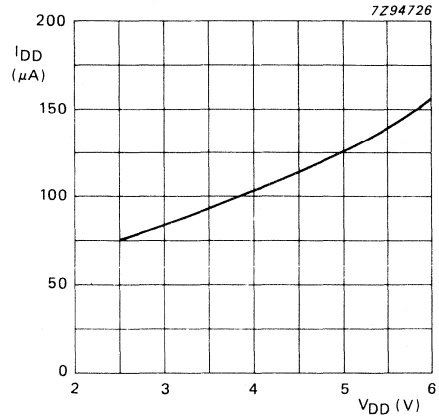
A/D CHARACTERISTICS

V_{DD} = 5,0 V; V_{SS} = 0 V; V_{REF} = 5,0 V; V_{AGND} = 0 V; R_{source} = 10 kΩ; T_{amb} = −40 °C to +85 °C unless otherwise specified

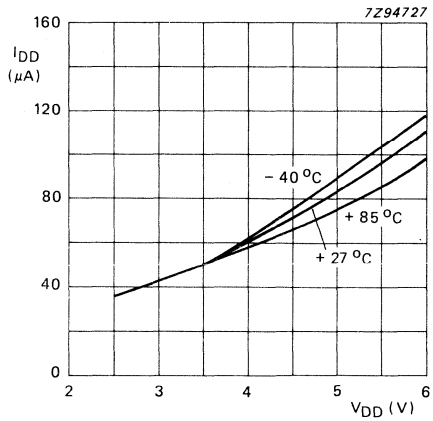
parameter	conditions	symbol	min.	typ.	max.	unit
Analogue inputs						
Input voltage range		V_{IA}	V_{SS}	–	V_{DD}	V
Input current	leakage	I_{IA}	–	–	100	nA
Input capacitance		C_{IA}	–	10	–	pF
Input capacitance	differential	C_{ID}	–	10	–	pF
Single-ended voltage	measuring range	V_{IS}	V_{AGND}	–	V_{REF}	V
Differential voltage	measuring range; $V_{FS} = V_{REF} - V_{AGND}$	V_{ID}	$\frac{-V_{FS}}{2}$	–	$\frac{+V_{FS}}{2}$	V
Accuracy						
Offset error	T_{amb} = 25 °C	OS_e	–	–	20	mV
Linearity error		L_e	–	–	±1,5	LSB
Gain error		G_e	–	–	1	%
Gain error	small-signal; ΔV_{IN} = 16 LSB	GS_e	–	–	5	%
Rejection ratio	common-mode	CMRR	–	60	–	dB
Supply noise rejection	at f = 100 Hz; V_{DDN} = 0,1xV_{PP}	SNRR	–	40	–	dB
Conversion time		t_{ADC}	–	–	90	μs
Sampling/conversion rate		f_{ADC}	–	–	11,1	kHz

Note

1. The power on reset circuit resets the I^2C bus logic when V_{DD} is less than V_{POR}.



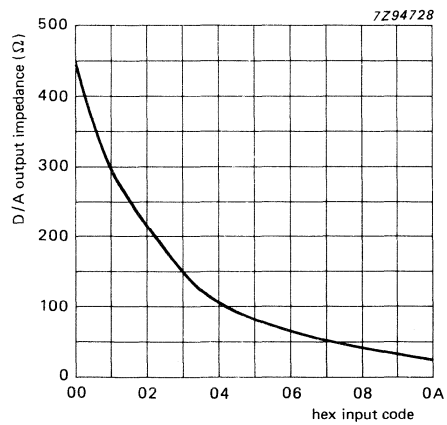
(a) internal oscillator; T_{amb} = + 27 °C.



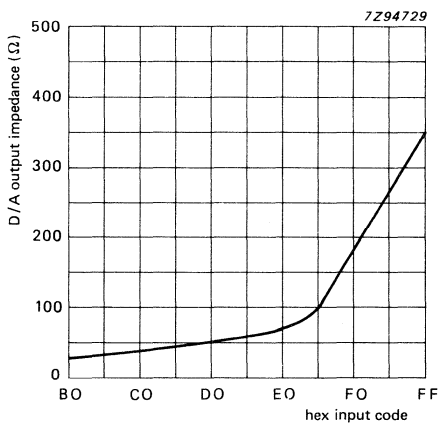
(b) external oscillator.

Fig. 16 Operating supply current against supply voltage (analogue output disabled).

DEVELOPMENT DATA



(a) output impedance near negative power rail; T_{amb} = + 27 °C.



(b) output impedance near positive power rail; T_{amb} = + 27 °C.

Fig. 17 Output impedance of analogue output buffer (near power rails).

The x-axis represents the hex input-code equivalent of the output voltage.

APPLICATION INFORMATION

Inputs must be connected to V_{SS} or V_{DD} when not in use. Analogue inputs may also be connected to AGND or V_{REF}.

In order to prevent excessive ground and supply noise and to minimize cross-talk of the digital to analogue signal paths the user has to design the printed-circuit board layout very carefully. Supply lines common to a PCF8591 device and noisy digital circuits and ground loops should be avoided. Decoupling capacitors ($> 10\ \mu F$) are recommended for power supply and reference voltage inputs.

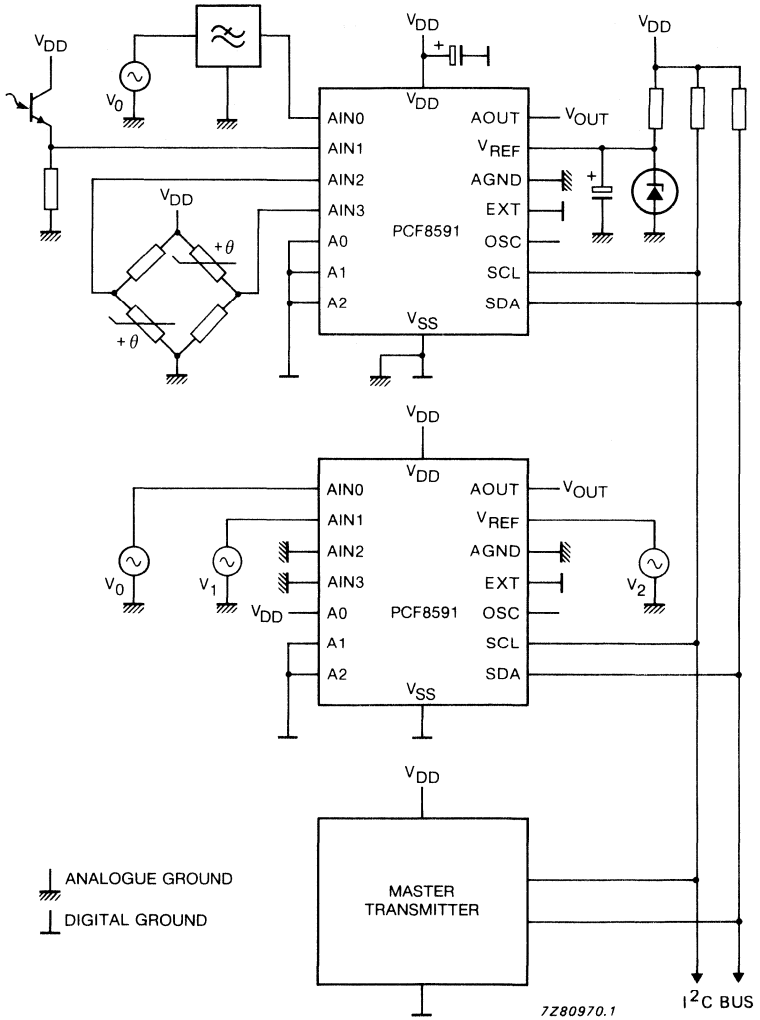


Fig. 18 Application diagram.

4-DIGIT LED-DRIVER WITH I²C BUS INTERFACE

GENERAL DESCRIPTION

The LED-driver is a bipolar integrated circuit made in an I²L compatible 18 volts process. The circuit is especially designed to drive four 7-segment LED displays with decimal point by means of multiplexing between two pairs of digits. It features an I²C bus slave transceiver interface with the possibility to program four different SLAVE ADDRESSES, a POWER RESET flag, 16 current sink OUTPUTS, controllable by software up to 21 mA, two multiplex drive outputs for common anode segments, an on-chip multiplex oscillator, control bits to select static, dynamic and blank mode, and one bit for segment test.

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage		V_{CC}	4,5	5	15	V
Supply current all outputs OFF	V_{CC} = 5 V	I_{CC}	–	9,5	–	mA
Total power dissipation 24-lead DIL (SOT-101B)		P_{tot}	–	–	1000	mW
Operating ambient temperature range		T_{amb}	−20	–	+ 70	°C

PACKAGE OUTLINE

SAA1064P: 24-lead DIL; plastic (with internal heat spreader) (SOT-101B).

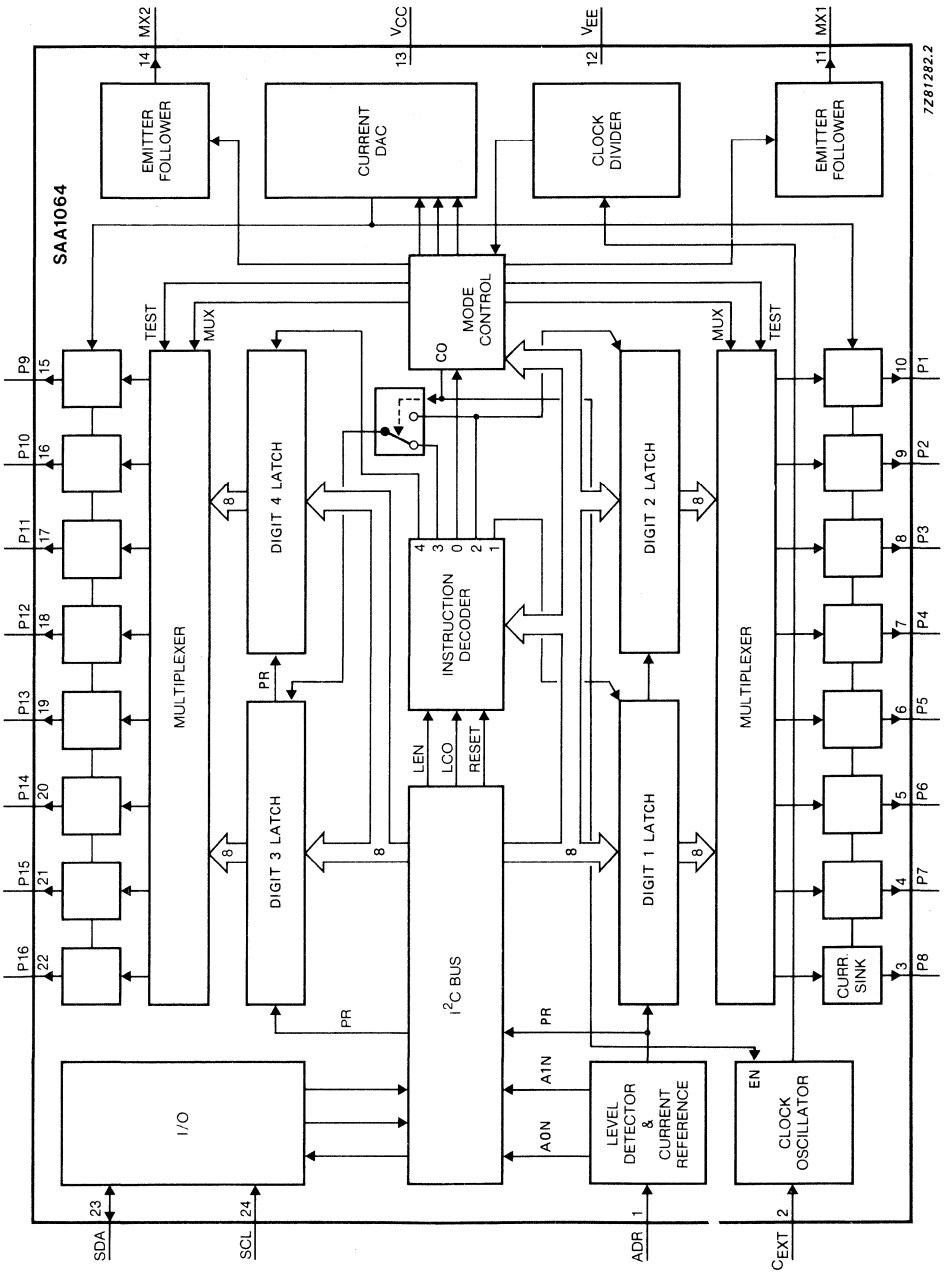


Fig. 1 Block diagram.

PINNING

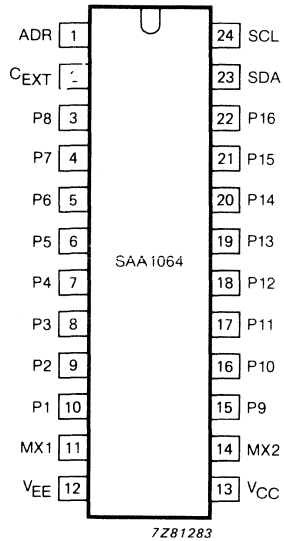


Fig. 2 Pinning diagram.

FUNCTIONAL DESCRIPTION

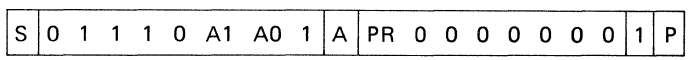


Fig. 3a I²C bus format; READ mode.

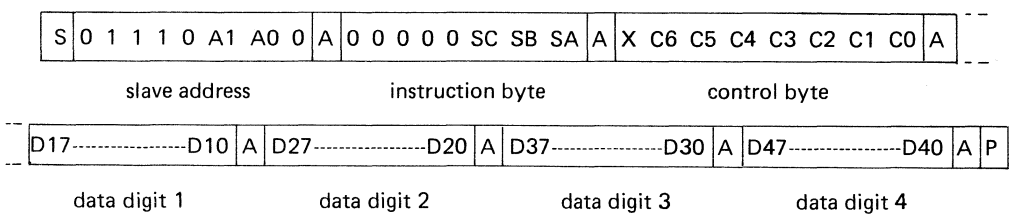


Fig. 3b I²C bus format; WRITE mode.

S = start condition
P = stop condition
A = acknowledge
X = don't care

A1, A0 = programmable address bits
SC SB SA = subaddress bits
C6 to C0 = control bits
PR = POWER RESET flag

Address pin ADR

Four different slave addresses can be chosen by connecting ADR either to V_{EE}, 3/8 V_{CC}, 5/8 V_{CC} or V_{CC}. This results in the corresponding valid addresses HEX 70, 72, 74 and 76 for writing and 71, 73, 75 and 77 for reading. All other addresses cannot be acknowledged by the circuit.

Status byte

Only one bit is present in the status byte, the POWER RESET flag. A logic 1 indicates the occurence of a power failure since the last time it was read out. After completion of the READ action this flag will be set to logic 0.

Subaddressing

The bits SC, SB and SA form a pointer and determine to which register the data byte following the instruction byte will be written. All other bytes will then be stored in the registers with consecutive subaddresses. This feature is called Auto-Increment (AI) of the subaddress and enables a quick initialization by the master.
The subaddress pointer will wrap around from 7 to 0.
The subaddresses are given as follows:

SC	SB	SA	sub-address	function
0	0	0	00	control register
0	0	1	01	digit 1
0	1	0	02	digit 2
0	1	1	03	digit 3
1	0	0	04	digit 4
1	0	1	05	reserved, not used
1	1	0	06	
1	1	1	07	

Control bits (see Fig. 4)

The control bits C0 to C6 have the following meaning:

C0 = 0	static mode, i.e. continuous display of digits 1 and 2
C0 = 1	dynamic mode, i.e. alternating display of digit 1 + 3 and 2 + 4
C1 = 0/1	digits 1 + 3 are blanked/not blanked
C2 = 0/1	digits 2 + 4 are blanked/not blanked
C3 = 1	all segment outputs are switched-on for segment test*
C4 = 1	adds 3 mA to segment output current
C5 = 1	adds 6 mA to segment output current
C6 = 1	adds 12 mA to segment output current

Data

A segment is switched ON if the corresponding data bit is logic 1. Data bits D17 to D10 correspond with digit 1, D27 to D20 with digit 2, D37 to D30 with digit 3 and D47 to D40 with digit 4.
The MSBs correspond with outputs P8 and P16, the LSBs with P1 and P9. Digit numbers 1 to 4 are equal to their subaddresses (hex) 1 to 4.

* At a current determined by C4, C5 and C6.

SDA, SCL

The SDA and SCL I/O meet the I²C bus specification. For protection against positive voltage pulses on these inputs voltage regulator diodes are connected to V_{EE}. This means that normal line voltage should not exceed 5,5 volt. Data will be latched on the positive-going edge of the acknowledge related clock pulse.

Power-on reset

The power-on reset signal is generated internally and sets all bits to zero, resulting in a completely blanked display. Only the POWER RESET flag is set.

External Control (C_{EXT})

With a capacitor connected to pin 2 the multiplex frequency can be set (see Fig. 5). When static this pin can be connected to V_{EE} or V_{CC} or left floating since the oscillator will be switched off.

Segment outputs

The segment outputs P1 to P16 are controllable current-sink sources. They are switched on by the corresponding data bits and their current is adjusted by control bits C4, C5 and C6.

Multiplex outputs

The multiplex outputs MX1 and MX2 are switched alternately in dynamic mode with a frequency derived from the clock-oscillator. In static mode MX1 is switched on. The outputs consist of an emitter-follower, which can be used to drive the common anodes of two displays directly provided that the total power dissipation of the circuit is not exceeded. If this occurs external transistors should be connected to pins 11 and 14 as shown in Fig. 5.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage (pin 13)		V_{CC}	−0,5	18	V
Supply current (pin 13)		I_{CC}	−50	200	mA
Total power dissipation SOT-101 24-lead DIL		P_{tot}		1000	mW
SDA, SCL voltages		$V_{23,\ 24\text{-}12}$	−0,5	5,9	V
Voltages A0-MX1 and MX2-P16		$V_{1\text{-}11,}$ $V_{14\text{-}22}$	−0,5	V_{CC} + 0,5	V
Input/output current all pins	outputs OFF	± I	−	10	mA
Operating ambient temperature range		T_{amb}	−20	+ 70	°C
Storage temperature range		T_{stg}	−65	+ 125	°C

THERMAL RESISTANCE

From crystal to ambient .
24-lead DIL $R_{th\ cr\text{-}a}$ 35 K/W

CHARACTERISTICS

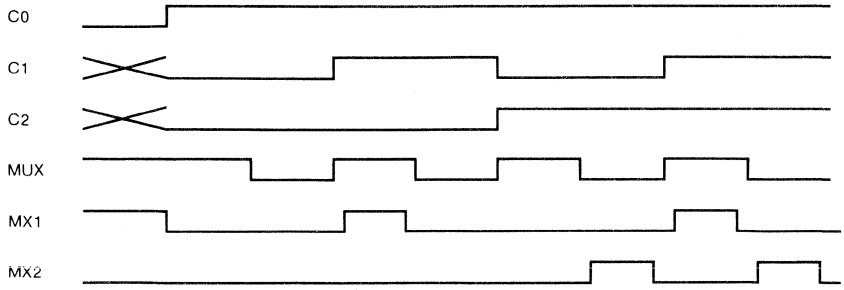
V_{CC} = 5 V; T_{amb} = 25 °C; voltages are referenced to ground (V_{EE} = 0 V); unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage (pin 13)		V_{CC}	4,5	5,0	15	V
Supply current	all outputs OFF V_{CC} = 5 V	I_{CC}	7,0	9,5	14,0	mA
Power dissipation	all outputs OFF	P_d	–	50	–	mW
SDA; SCL bus (pins 23 and 24)						
Input voltages		$V_{23,24}$	0	–	5,5	V
Logic input voltage LOW		$V_{IL(L)}$	–	–	1,5	V
Logic input voltage HIGH		$V_{IH(L)}$	3,0	–	–	V
Input current LOW	$V_{23,24} = V_{EE}$	I_{IL}	–	–	−10	μA
Input current HIGH	$V_{23,24} = V_{CC}$	I_{IH}	–	–	10	μA
SDA						
Logic output voltage LOW	I_O = 3 mA	$V_{OL(L)}$	–	–	0,4	V
Output sink current		I_O	3	–	–	mA
Address input (pin 1)						
Input voltage programmable address bits:						
A0 = 0; A1 = 0		V_1	V_{EE}	–	3/16V_{CC}	V
A0 = 1; A1 = 0		V_1	5/16V_{CC}	3/8V_{CC}	7/16V_{CC}	V
A0 = 0; A1 = 1		V_1	9/16V_{CC}	5/8V_{CC}	11/16V_{CC}	V
A0 = 1; A1 = 1		V_1	13/16V_{CC}	–	V_{CC}	V
Input current LOW	$V_1 = V_{EE}$	I_1	–	–	−10	μA
Input current HIGH	$V_1 = V_{CC}$	I_1	–	–	10	
External control (C_{EXT}) pin 2						
Switching level input						
Input voltage LOW		V_{IL}	–	–	V_{CC}−2,5	V
Input voltage HIGH		V_{IH}	V_{CC}−1,5	–	–	V
Input current	V_2 = 2 V	I_2	−140	−160	−180	μA
	V_2 = 4 V	I_2	140	160	180	μA

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Segment outputs (P8 to P1; pins 3 to 10) (P9 to P16; pins 15 to 22)						
Output voltages	I_O = 15 mA	V_O	–	–	0,5	V
Output current HIGH	$V_O = V_{CC}$ = 15 V	I_O	–	–	± 10	μA
Output current LOW control bits HIGH C4, C5 and C6	V_O = 5 V	I_O	17,85	21	25	mA
Contribution of:						
control bit C4		I_O	2,55	3,0	4,0	mA
control bit C5		I_O	5,1	6,0	7,0	mA
control bit C6		I_O	10,2	12,0	14,0	mA
Relative segment 1 output accuracy with respect to highest value when:						
I_3 to I_{10} and I_{15} to I_{22} = 3 mA		ΔI_O	–	–	5	%
I_3 to I_{10} and I_{15} to I_{22} = 21 mA		ΔI_O	–	–	7	%
Multiplex 1 and 2 (pins 11 and 14)						
Output voltage (when ON)	I_O = 50 mA	V_O	V_{CC} 1,5	–	–	V
Output current HIGH (when ON)	V_O = 2 V	$I_{11}; I_{14}$	50	–	*	mA
Output current LOW (when OFF)	V_O = 2 V	$-I_{11}; -I_{14}$	50	70	100	mA
Output period	$C_{2\text{-}12}$ = 2,7 nF	T_{MPX}	5	–	10	ms
	$C_{2\text{-}12}$ = 820 pF	T_{MPX}	–	1,25	–	ms
	$C_{2\text{-}12}$ = 390 pF	T_{MPX}	–	666	–	μs
Output duty factor			48,4	–	–	%

* Value to be fixed.



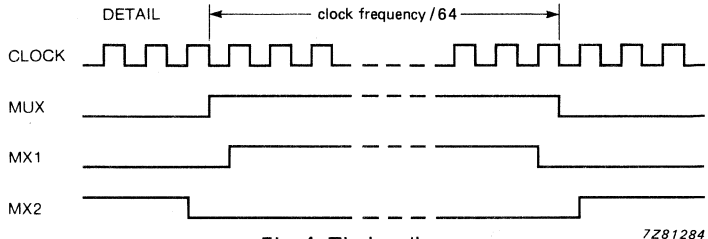


Fig. 4 Timing diagram.

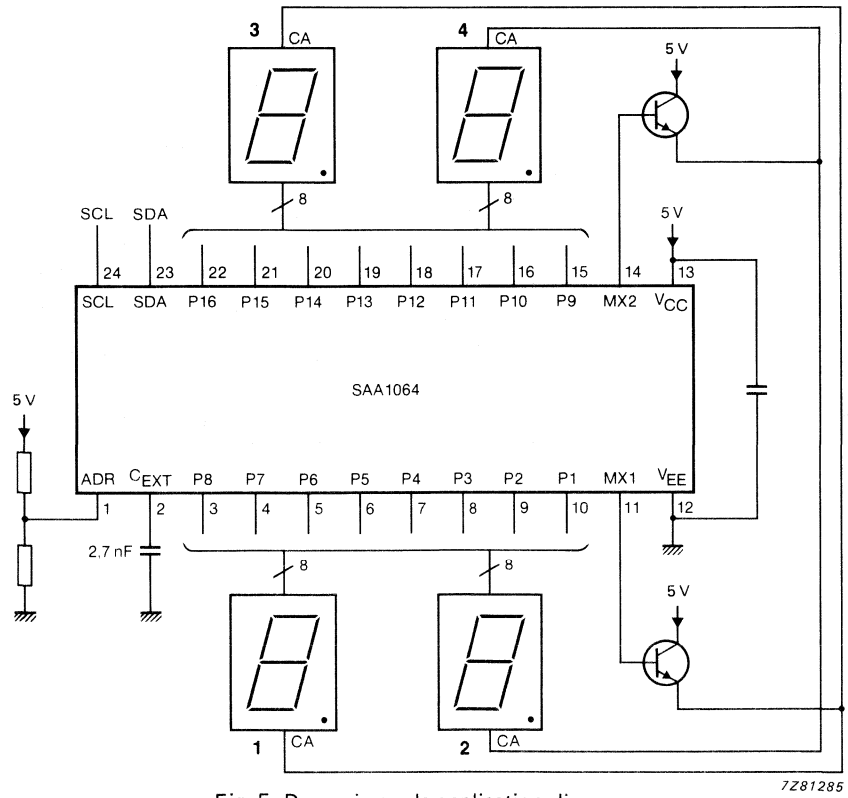


Fig. 5 Dynamic mode application diagram.

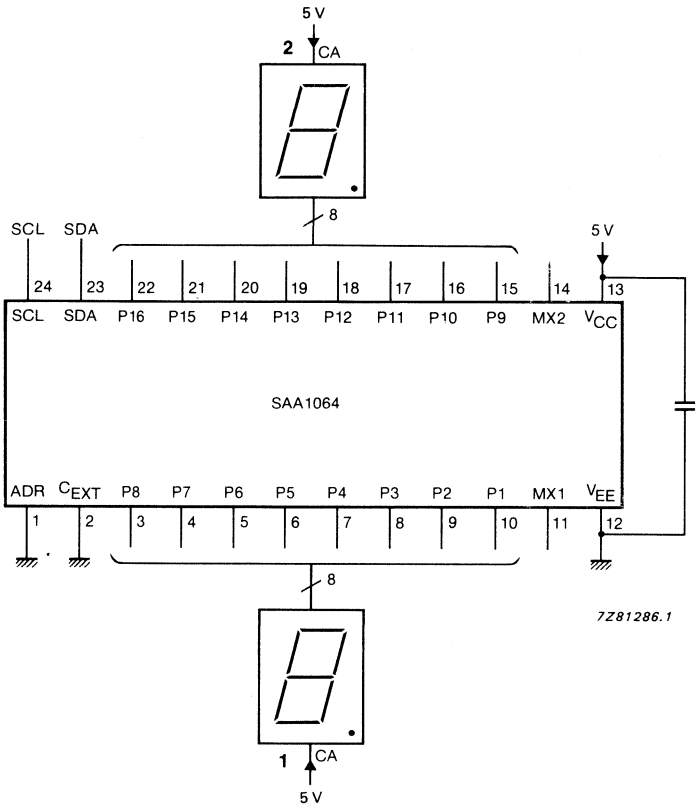


Fig. 6 Static mode application diagram.

PCM-AUDIO IDENT-WORD INTERFACE (IDI)

GENERAL DESCRIPTION

The SAA1136 is an extension to the PCM-audio system for 8 mm cassette video recorders that allows the PCM bus to be accessed via the two-line bidirectional I²C bus. Other ICs in the system are error-corrector-1 ECO-1 (SAA1131), error-corrector-2 ECO-2 (SAA1132), analog/digital interface ADI (SAA1133) and RAM storage.

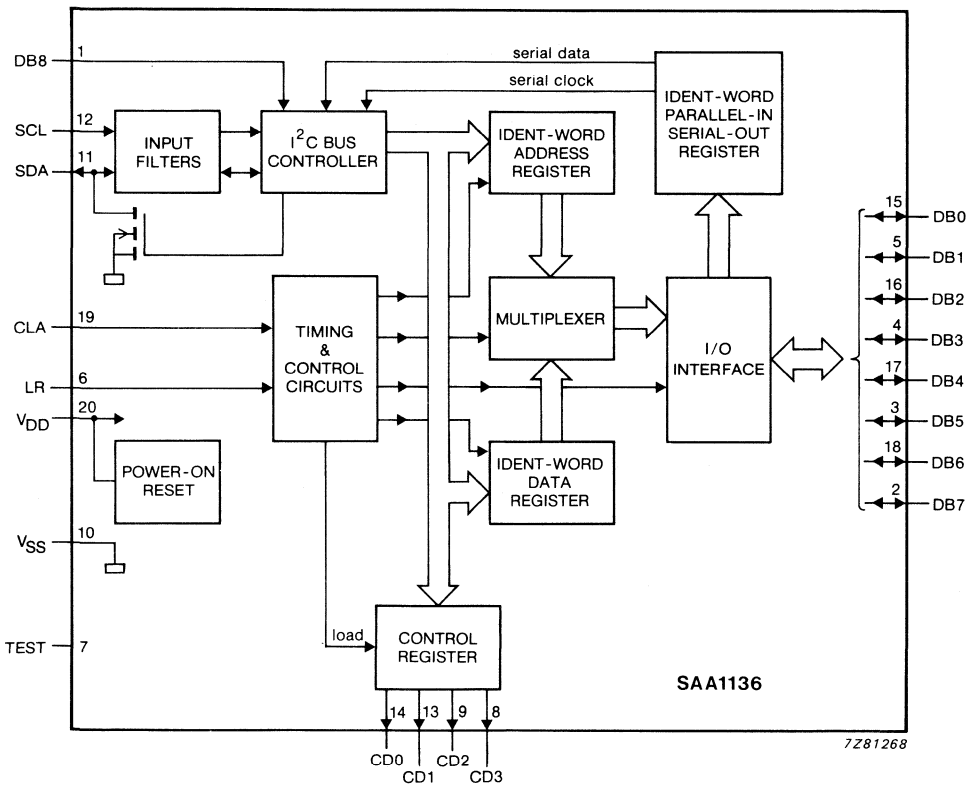


Fig. 1 Block diagram.

PACKAGE OUTLINES

SAA1136P: 20-lead DIL; plastic (SOT-146).
SAA1136T: 20-lead mini-pack; plastic (SO-20; SOT-163A).

PINNING

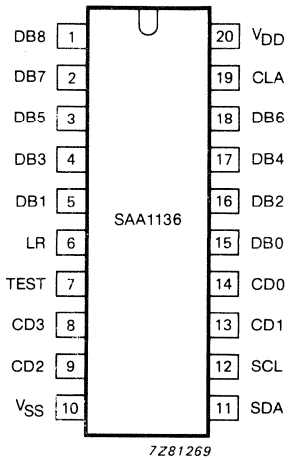


Fig. 2 Pinning diagram.

Power supplies

V_{DD}	positive supply voltage (+ 5 V)
V_{SS}	ground (0 V)

Inputs (TTL)

DB8	fault flag input from data bus
SCL	I^2C bus serial data clock

Inputs (CMOS)

LR	system data bus control, typ. 31,25 kHz (CCIR) or 31,45 kHz (NTSC)
TEST	test pin. Must be held LOW for normal operation
CLA	system clock, typ. 1437,5 kHz (CCIR) or 1449 kHz (NTSC) (92 x line frequency)

Input/outputs (TTL-input/3-state push-pull output)

DB0 (lsb) to DB7 (msb)	data bus connections. I/O state is determined by the process being performed

Input/output (TTL-input/open drain output)

SDA	I^2C bus data input/output

Outputs (CMOS push-pull)

CD0 to CD3	control outputs

FUNCTIONAL DESCRIPTION

The IDI is instructed via the I²C bus to perform one of three functions:

WRITE — Following a WRITE instruction, the address and data for an ident-word are received from the I²C bus. These are transcoded and transferred to the PCM bus during the 6th CLA clock following a transition of LR.

READ — Following a READ instruction, an ident-word address is received from the I²C bus. The ident-word corresponding to this address is read from the PCM bus on the 6th CLA clock following a transition of LR. The ident-word is then transcoded and transferred to the I²C bus.

CONTROL — Following a WRITE instruction and a specific (pointer) address from the I²C bus, the next I²C data controls the CD0-CD3 outputs.

CHARACTERISTICS OF THE I²C BUS

The I²C bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

DEVELOPMENT DATA

Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals.

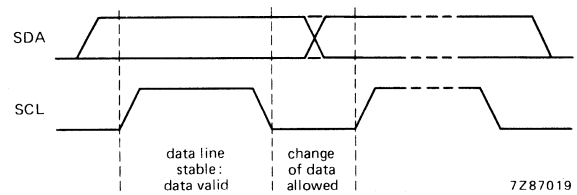


Fig. 3 Bit transfer.

CHARACTERISTICS OF THE I²C BUS (continued)

Start and stop conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the stop condition (P).

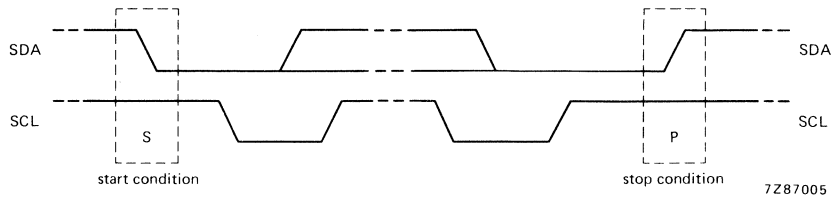


Fig. 4 Definition of start and stop conditions.

System configuration

A device generating a message is a "transmitter", a device receiving a message is the "receiver". The device that controls the message is the "master" and the devices which are controlled by the master are the "slaves".

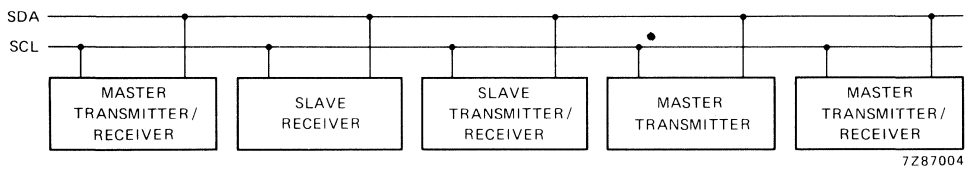


Fig. 5 System configuration.

Acknowledge

The number of data bytes transferred between the start and stop conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter whereas the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse, set-up and hold times must be taken into account. A master receiver must signal an end of data to the transmitter by *not* generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

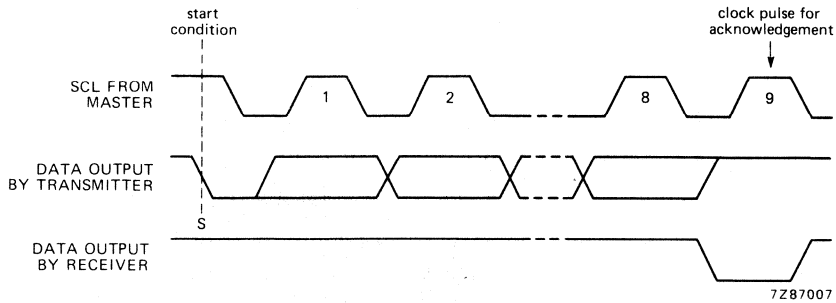


Fig. 6 Acknowledgement on the I^2C bus.

Timing specifications

Within the I^2C bus specifications a high-speed mode and a low-speed mode are defined. The device operates in both modes and the timing requirements are as follows:

High-speed mode

Masters generate a bus clock with a maximum frequency of 100 kHz. Detailed timing is shown in Fig. 7.

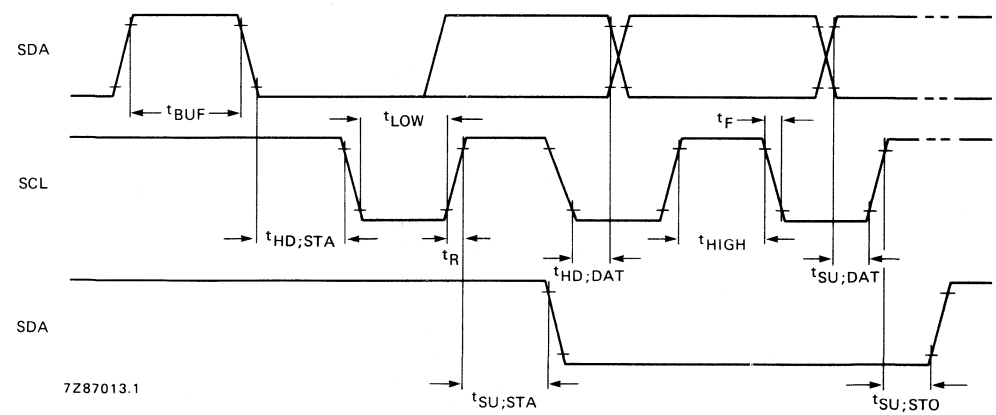


Fig. 7 Timing of the high-speed mode.

Where:

t_{BUF}	$t \geqslant t_{LOWmin}$	The minimum time the bus must be free before a new transmission can start
$t_{HD;STA}$	$t \geqslant t_{HIGHmin}$	Start condition hold time
t_{LOWmin}	4,7 μs	Clock LOW period

Timing specifications (continued)

High-speed mode (continued)

$t_{HIGHmin}$	4 μs	Clock HIGH period
$t_{SU;STA}$	$t \geqslant t_{LOWmin}$	Start condition set-up time, only valid for repeated start code
$t_{HD;DAT}$	$t \geqslant 0$ μs	Data hold time
$t_{SU;DAT}$	$t \geqslant 250$ ns	Data set-up time
t_R	$t \leqslant 1$ μs	Rise time of both the SDA and SCL line
t_F	$t \leqslant 300$ ns	Fall time of both the SDA and SCL line
$t_{SU;STO}$	$t \geqslant t_{LOWmin}$	Stop condition set-up time

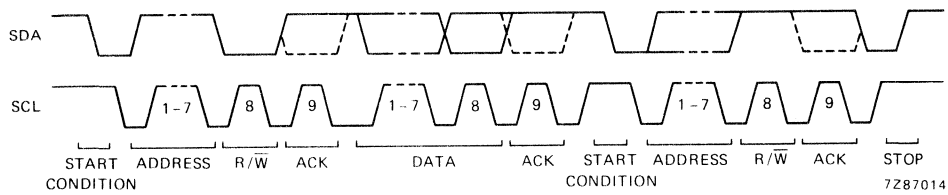


Fig. 8 Complete data transfer in the high-speed mode.

Where:

Clock t_{LOWmin}	4,7 μs
$t_{HIGHmin}$	4 μs
The dashed line is the acknowledgement of the receiver	
Mark-to-space ratio	1 : 1 (LOW-to-HIGH)
Max. number of bytes	unrestricted
Premature termination of transfer	allowed by generation of STOP condition
Acknowledge clock bit	must be provided by the master

Note

All the timing values refer to V_{IH} and V_{IL} levels with a voltage swing of V_{SS} to V_{DD}.

Low-speed mode

Masters generate a bus clock with a maximum frequency of 2 kHz; a minimum LOW period of 105 μs and a minimum HIGH period of 365 μs. The mark-to-space ratio is 1 : 3 LOW-to-HIGH. Detailed timing is shown in Fig. 9.

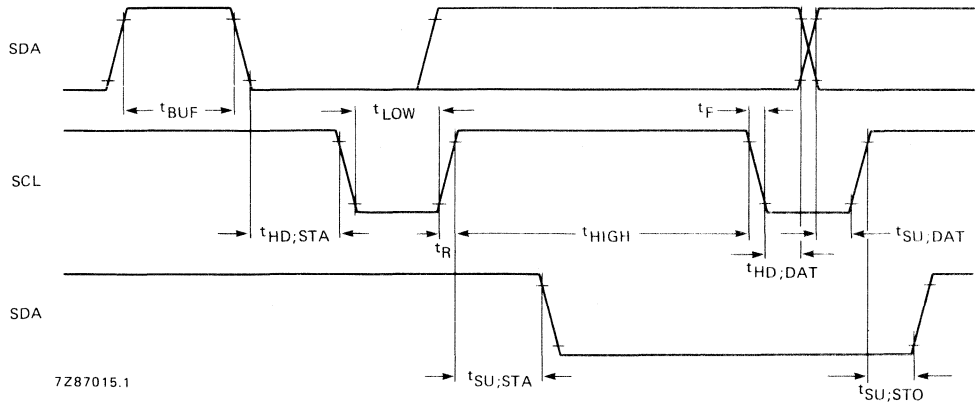


Fig. 9 Timing of the low-speed mode.

Where:

t_{BUF}	$t \geqslant 105\ \mu s$ (t_{LOWmin})
$t_{HD;STA}$	$t \geqslant 365\ \mu s$ ($t_{HIGHmin}$)
t_{LOW}	130 μs ± 25 μs
t_{HIGH}	390 μs ± 25 μs
$t_{SU;STA}$	130 μs ± 25 μs *
$t_{HD;DAT}$	$t \geqslant 0\ \mu s$
$t_{SU;DAT}$	$t \geqslant 250$ ns
t_R	$t \leqslant 1\ \mu s$
t_F	$t \leqslant 300$ ns
$t_{SU;STO}$	130 μs ± 25 μs

* Only valid for repeated start code.

Note

All the timing values refer to V_{IH} and V_{IL} levels with a voltage swing of V_{SS} to V_{DD}. For definitions see high-speed mode.

Timing specifications (continued)

Low-speed mode (continued)

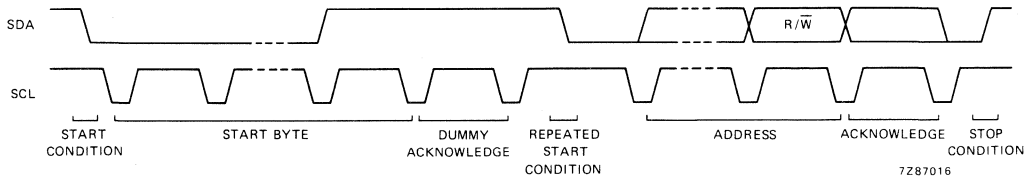
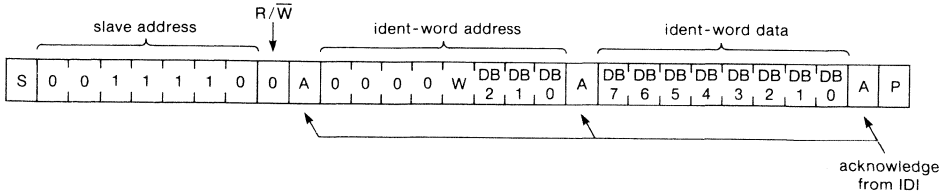


Fig. 10 Complete data transfer in the low-speed mode.

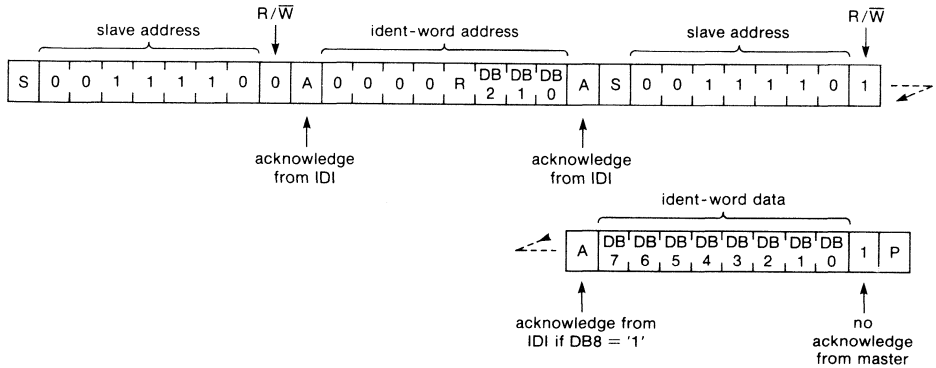
Where:	
Clock t_{LOWmin}	130 μs ± 25 μs
$t_{HIGHmin}$	390 μs ± 25 μs
Mark-to-space ratio	1 : 3 (LOW-to-HIGH)
Start byte	0000 0001
Max. number of bytes	6
Premature termination of transfer	not allowed
Acknowledge clock bit	must be provided by master

I²C bus protocol

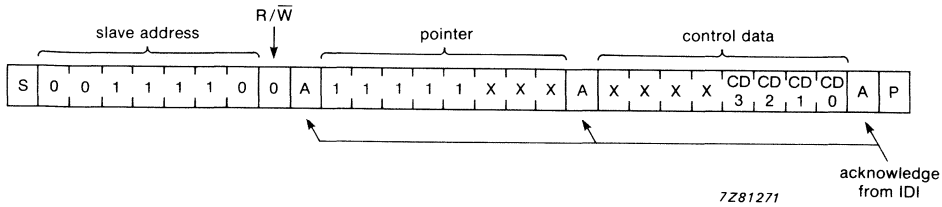
Before any data is transmitted on the I²C bus, the device which should respond is addressed first. The addressing is always done with the first byte after the start procedure. The IDI slave address is 0 0 1 1 1 1 0. The bus protocol for the WRITE, READ and CONTROL functions is shown in Fig. 11.



(a) WRITE



(b) READ



(c) CONTROL

Fig. 11 I²C bus protocol.

DEVELOPMENT DATA

RATINGS

Limiting values in accordance with the Absolute Maximum Rating System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage range	pin 20	$V_{DD} = V_{20-10}$	−0,5	7,0	V
Supply current	pin 20	I_{DD}	–	50	mA
Supply current	pin 10	I_{SS}	–	50	mA
Input voltage range		V_I	−0,5	V_{DD} + 0,5*	V
Input current		I_I	–	±10	mA
Output current		I_O	–	±10	mA
Total power dissipation		P_{tot}	–	200	mW
Storage temperature range		T_{stg}	−55	+150	°C

* V_{DD} + 0,5 V not to exceed 7,0 V.

HANDLING

Inputs and outputs are protected against electrostatic charge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see 'Handling MOS Devices').

D.C. CHARACTERISTICS

T_{amb} = −20 to +70 °C; V_{DD} = 4,75 to 5,25 V; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage	pin 20	V_{DD}	4,75	5,0	5,25	V
Supply current	pin 20; $V_I = V_{DD}$ or V_{SS} for all inputs; I_O = 0 mA for all outputs	I_{DD}	–	–	100	μA
Inputs LR, CLA						
Input voltage HIGH		V_{IH}	0,7xV_{DD}	–	–	V
Input voltage LOW		V_{IL}	–	–	0,3xV_{DD}	V
Input leakage current		I_I	–	–	1	μA

parameter	conditions	symbol	min.	typ.	max.	unit
Inputs DB8, SCL, TEST						
Input voltage HIGH		V_{IH}	2,0	–	–	V
Input voltage LOW		V_{IL}	–	–	0,8	V
Input leakage current		I_I	–	–	1	μA
Input/outputs DB0 to DB7						
Input voltage HIGH		V_{IH}	2,0	–	–	V
Input voltage LOW		V_{IL}	–	–	0,8	V
Output voltage HIGH	$-I_{OH}$ = 1,0 mA	V_{OH}	V_{DD}–0,4	–	–	V
Output voltage LOW	I_{OL} = 1,6 mA	V_{OL}	–	–	0,4	V
3-state OFF-state leakage current		I_{OZ}	–	–	20	μA
Input/output SDL						
Input voltage HIGH		V_{IH}	2,0	–	–	V
Input voltage LOW		V_{IL}	–	–	0,8	V
Output voltage LOW	$+I_{OL}$ = 5 mA	V_{OL}	–	–	0,4	V
3-state OFF-state leakage current		I_{OZ}	–	–	20	μA

DEVELOPMENT DATA

A.C. CHARACTERISTICS

T_{amb} = −20 to +70 °C; V_{DD} = 4,75 to 5,25 V; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
INPUTS					
Serial data clock SCL frequency	f_{SCL}	–	–	100	kHz
System clock CLA frequency	f_{CLA}	–	–	2,1	MHz
LR to CLA set-up time	t_{su}	20	–	–	ns
DB0-DB7, DB8 to CLA set-up time	t_{su}	20	–	–	ns
LR to CLA hold time	t_h	10	–	–	ns
DB0-DB7, DB8 to CLA hold time	t_h	10	–	–	ns
OUTPUTS					
CLA to DB0-DB7 output delay time C_L = 50 pF	t_{OD}	20	–	100	ns

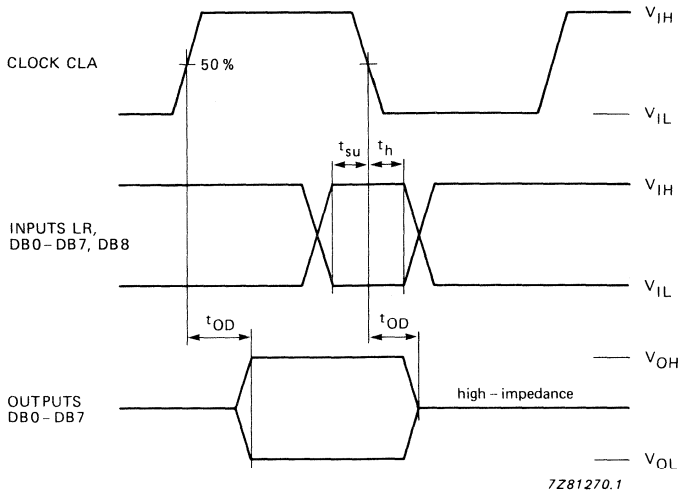


Fig. 12 Waveforms showing the input set-up and hold times of LR, DB0-DB7 and DB8 to CLA, and the clock-to-output delay time from CLA to DB0-DB7 (DB0-DB7 input levels are TTL, all other levels are CMOS).

TUNER SWITCHING CIRCUIT

The SAA1300 is for switching on and off the supply lines of various circuit parts via an I^2C bus signal. Furthermore, it can be used to supply current for switching diodes in radio and television tuners. It contains 5 output stages, which are capable of supplying up to 85 mA in the ON state or sinking up to $-100\ \mu A$ in the OFF state.

Current limiting and short-circuit protection are included. The output stages are driven by a shift register/latch combination which is loaded via data from the I^2C bus. A power-on reset of the latches ensures the OFF state of the output stages (OUT 2 to OUT 5) without data reception from the I^2C bus. A subaddressing system allows the connection of up to three circuits on the same I^2C bus lines; one of the outputs (OUT 1, pin 7) can also be used as an input to select the device via a simple internal A/D converter.

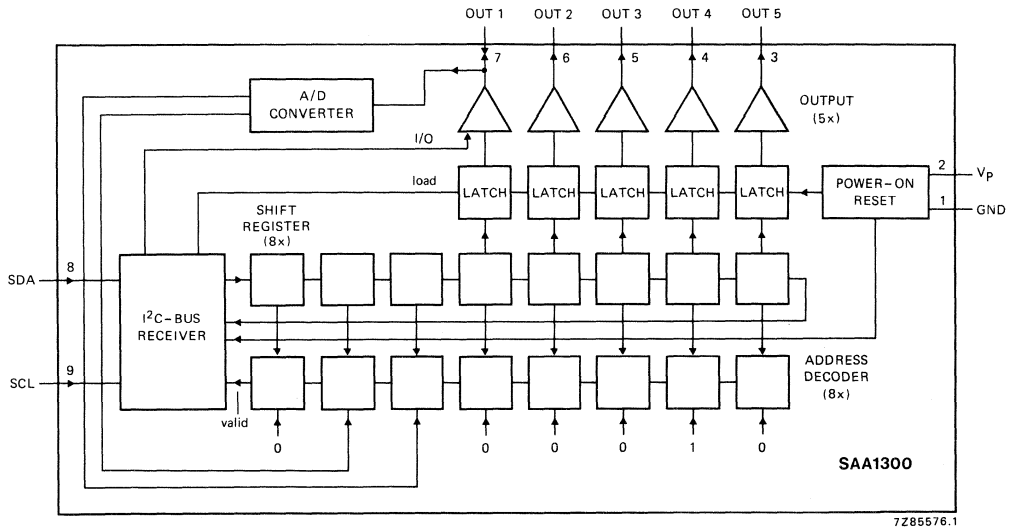


Fig. 1 Block diagram.

PACKAGE OUTLINE

9-lead SIL; plastic (SOT-142).

PINNING

pin no.	symbol	function
1	GND	ground
2	V_P	positive supply
3	OUT 5	outputs
4	OUT 4	
5	OUT 3	
6	OUT 2	
7	OUT 1	output and subaddressing input
8	SDA	serial data line (I^2C bus)
9	SCL	serial clock line (I^2C bus)

I^2C BUS INFORMATION

Address, first byte

0 1 0 0 0 A B 0 where,

A	B	function	condition
0	0	general address	OUT 1 = output
0	1	OUT 1 = input	address accepted if $V_{OUT\,1} = V_{OUT\,L}$ (LOW)
1	0	OUT 1 = input	address accepted if $V_{OUT\,1} = V_{OUT\,H}$ (HIGH)
1	1	OUT 1 = input	address accepted if $V_{OUT\,1} = V_{OUT\,M}$ (MEDIUM)

Data, second byte

OUT 5, OUT 4, OUT 3, OUT 2, OUT 1, X, X, X

The I/O output stage (OUT 1) is switched as an input stage after a power-on reset. It depends on the contents of the first data transmission whether the output stage is switched as an output or remains as an input.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	13,2	V
Input voltage range at SDA, SCL	V_I		−0,5 to + 6,0	V
Input voltage range at OUT 1	V_I		−0,5 to + 12,5	V
Output voltage range at OUT 1 to OUT 5	V_O		−0,5 to + 12,5	V
Input current at SDA, SCL	I_I	max.	20	mA
Input current at OUT 1	I_I	max.	20	mA
Total power dissipation	P_{tot}	max.	825	mW
Storage temperature range	T_{stg}		−40 to + 125	°C
Operating ambient temperature range	T_{amb}		−20 to + 80	°C

CHARACTERISTICS

V_P = 8 V; T_{amb} = 25 °C; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply (pin 2)					
Supply voltage range	V_P	4	8	12	V
Supply current					
5 outputs LOW	I_{PL}	5	10	15	mA
5 outputs HIGH	I_{PH}	30	50	70	mA
Power-on reset level output stage in "OFF' condition	V_{PR}	–	3,5	3,8	V
Maximum power dissipation*	P_{max}	–	650	–	mW
Inputs SDA, SCL (pins 8 and 9)					
Input voltage HIGH	V_{IH}	3,0	–	5,5	V
Input voltage LOW	V_{IL}	0	–	1,5	V
Input current HIGH	$-I_{IH}$	–	–	10	μA
Input current LOW	I_{IH}	–	–	0,4	μA
Acknowledge sink current	I_{ACK}	2,5	–	–	mA
Maximum input frequency	$f_{i\,max}$	100	–	–	kHz
Outputs OUT 1 to OUT 5 (pins 3 to 7)					
Maximum output current; source: "ON"	I_{Oso}	+ 85	–	+ 150	mA
Maximum output current; source: "ON" T_{amb} = 80 °C	I_{Oso}	60	–	–	mA
Output voltage HIGH at I_{Oso} = 85 mA	V_{OH}	V_P–2	–	–	V
Output current; sink "OFF"	I_{Osi}	–100	–300	–	μA
Output voltage LOW at I_{Osi} = –100 μA	V_{OL}	–	–	100	mV
Output voltage MEDIUM at I_O = 10 mA	V_{OM}	V_P–0,5	–	–	V
OUT 1 used as subaddressing input					
Input voltage HIGH (code 1 0)	$V_{OUT\,1H}$	0,72 V_P	–	V_P	V
Input voltage MEDIUM (code 1 1)	$V_{OUT\,1M}$	0,39 V_P	–	0,61 V_P	V
Input voltage LOW (code 0 1)	$V_{OUT\,1L}$	0	–	0,28 V_P	V

* Outputs must not be driven simultaneously at maximum source current.

INFRARED REMOTE CONTROL TRANSCODER (RC-5)

GENERAL DESCRIPTION

The SAA3028 is intended for use in general purpose (RC-5) remote control systems. The main function of this integrated circuit is to convert RC-5 biphase coded signals into equivalent binary values. Two input circuits are available: one for RC-5 coded signals only; the other is selectable to accept (1) RC-5 coded signals only, or (2) RC-5 (extended) coded signals only. The input used is that at which an active code is first detected. Coded signals not in RC-5/RC-5(ext) format are rejected. Data input and output is by serial transfer, the output interface being compatible for I^2C bus operation.

Features

- Converts RC-5 or RC-5(ext) biphase coded signals into binary equivalents
- Two data inputs, one fixed (RC-5), one selectable (RC-5/RC-5(ext))
- Rejects all codes not in RC-5/RC-5(ext) format
- I^2C output interface capability
- Power-off facility
- Master/slave addressable for multi-transmitter/receiver applications in RC-5(ext) mode
- Power-on-reset for defined start-up

QUICK REFERENCE DATA

Supply voltage range	V_{DD}	4,5 to	5,5 V
Supply current (quiescent) at V_{DD} = 5,5 V; T_{amb} = 25 °C	I_{DD}	max.	200 μA
Operating ambient temperature range	T_{amb}	−25 to	+85 °C

PACKAGE OUTLINE

16-lead DIL; plastic (SOT-38Z).

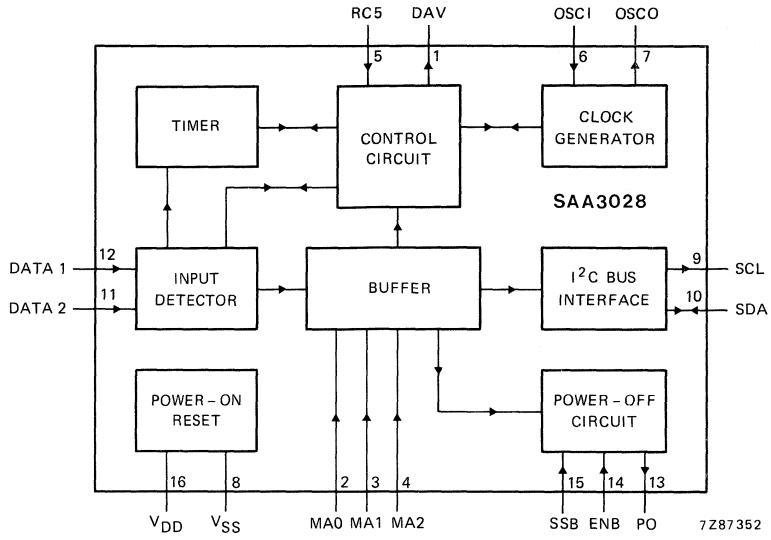


Fig. 1 Block diagram.

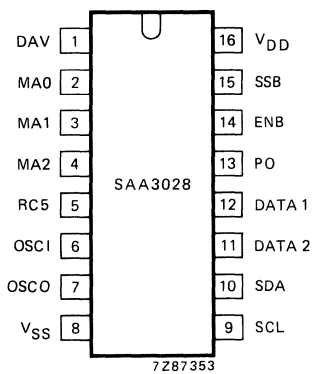


Fig. 2 Pinning diagram.

PINNING

1	DAV	data valid output with open drain N-channel transistor
2	MA0	master address inputs
3	MA1	
4	MA2	
5	RC5	data 2 input select
6	OSCI	oscillator input
7	OSCO	oscillator output
8	V_{SS}	negative supply (ground)
9	SCL	serial clock line (I^2C bus)
10	SDA	serial data line (I^2C bus)
11	DATA 2	data 2 input
12	DATA 1	data 1 input
13	PO	power-off signal output with open drain N-channel transistor
14	ENB	enable input
15	SSB	set standby input
16	V_{DD}	positive supply (+5 V)

FUNCTIONAL DESCRIPTION

Input function

The two data inputs are accepted into the buffer as follows:

- DATA 1. Only biphase coded signals which conform to the RC-5 format are accepted at this input.
- DATA 2. This input performs according to the logic state of the select input RC5. When RC5 = HIGH, DATA 2 input will accept only RC-5 coded signals. When RC5 = LOW, DATA 2 input will accept only RC-5(ext) coded signals.

The input detector selects the input, DATA 1 or DATA 2, in which a HIGH to LOW transition is first detected. The selected input is then accepted by the buffer for code conversion. All signals received that are not in the RC-5 or RC-5(ext) format are rejected.

Formats of RC-5 and RC-5(ext) biphase coded signals are shown in Figs 3 and 4 respectively; the codes commence from the left of the formats shown. The bit-times of the biphase codes are defined in Fig. 5.

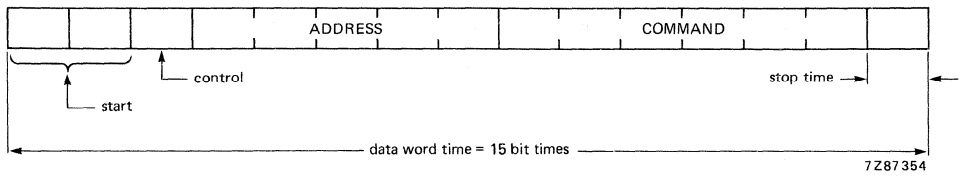


Fig. 3 RC-5 code format: the first start bit is used only for detection and input gain-setting; stop time = 1,5 bit-times (nominal).

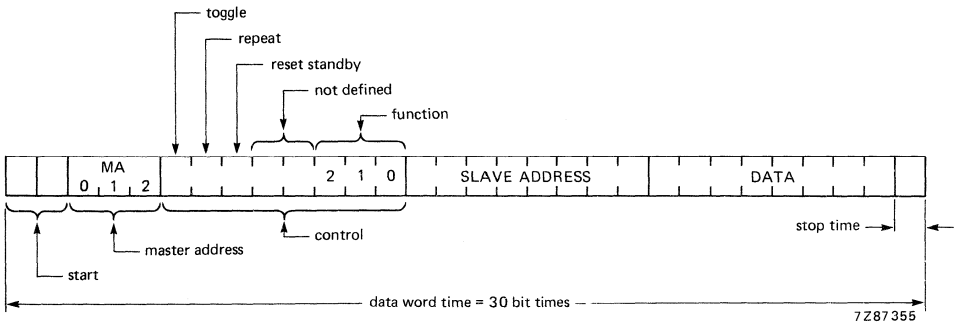


Fig. 4 RC-5(extended) code format: the first start bit is used only for detection and input gain-setting; stop time = 1,5 bit-times (nominal).

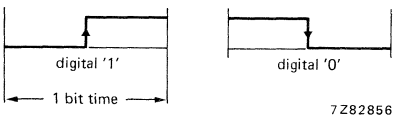


Fig. 5 Biphase code definition: RC-5 bit-time = $2^7 \times T_{OSC}$ = 1,778 ms (typical); RC-5(ext) bit-time = $2^6 \times T_{OSC}$ = 0,89 ms (typical), where T_{OSC} = the oscillator period time.

FUNCTIONAL DESCRIPTION (continued)

More information is added to the input data held in the buffer in order to make it suitable for transmission via the I^2C interface. The information now held in the buffer is as follows:

RC-5 buffer contents		RC-5(ext) buffer contents	
• data valid indicator	1 bit	• data valid indicator	1 bit
• format indicator	1 bit	• format indicator	1 bit
• input indicator	1 bit	• input indicator	1 bit
• control	1 bit	• master address	3 bits
• address data	5 bits	• control	8 bits
• command data	6 bits	• slave address	8 bits
		• data	8 bits

The information assembled in the buffer is subjected to the following controls before being made available at the I^2C interface:

ENB = HIGH — Enables the set standby input SSB.

SSB = LOW — Causes power-off output PO to go HIGH.

PO = HIGH — This occurs when the set standby input SSB = LOW and allows the existing values in the buffer to be overwritten by the new binary equivalent values. After ENB = LOW, SSB is don't care.

PO = LOW — This occurs according to the type of code being processed, as follows:

RC-5. When the binary equivalent value is transferred to the buffer.

RC-5(ext). When the reset standby bit is active and the master address bits are equal in value to the MA0, MA1, MA2 inputs.

At power-on, PO is reset to LOW.

DAV = HIGH — This occurs when the buffer contents are valid. If the buffer is not empty, or an output transfer is taking place, then the new binary values are discarded.

Output function

The data is assembled in the buffer in the format shown in Fig. 6 for RC-5 binary equivalent values, or in the format shown in Fig. 7 for RC-5(ext) binary equivalent values. The data is output serially, starting from the left of the formats shown in Figs 6 and 7.

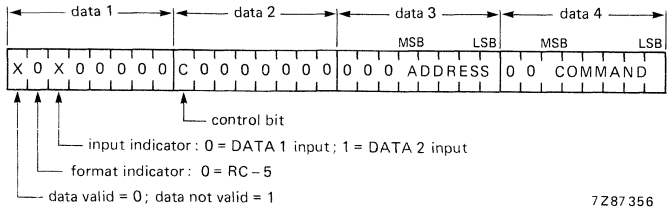


Fig. 6 RC-5 binary equivalent value format.

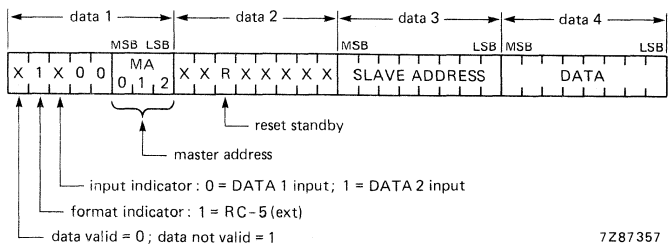


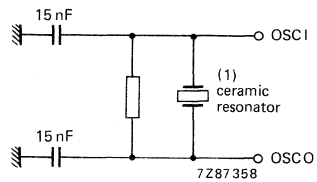
Fig. 7 RC-5(ext) binary equivalent value format.

The output signal DAV, derived in the buffer from the data valid bit, is provided to facilitate use of the transcoder on an interrupt basis. This output is reset to LOW during power-on.

The I^2C interface allows transmission on a bidirectional, two-wire I^2C bus. The interface is a slave transmitter with a built-in slave address, having a fixed 7-bit binary value of 0100110. Serial output of the slave address onto the I^2C bus starts from the left-hand bit.

Oscillator

The oscillator can comprise a ceramic resonator circuit as shown in Fig. 8. The typical frequency of oscillation is 455 kHz.



(1) Catalogue number of ceramic resonator: 2422 540 98008.

Fig. 8 Oscillator circuit.

DEVELOPMENT DATA

FUNCTIONAL DESCRIPTION (continued)

I²C bus transmission

Formats for I²C transmission in low and high speed modes are shown respectively in Figs 9 and 10.

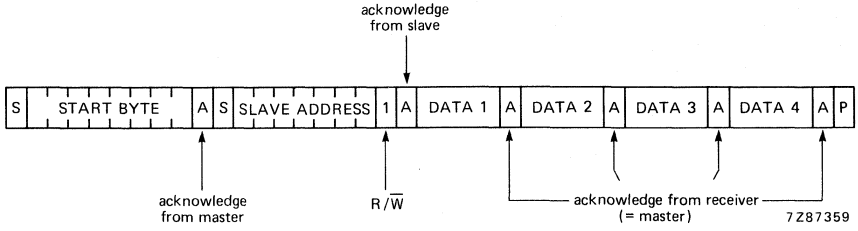


Fig. 9 Format for transmission in I²C low speed mode.

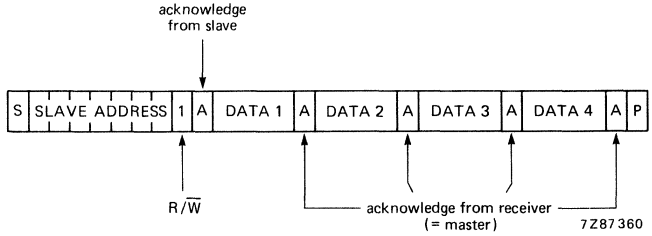


Fig. 10 Format for transmission in I²C high speed mode.

Note to Figures 9 and 10

When R/$\overline{W}$ bit = 0; the slave generates a NACK (negative acknowledge), leaves the data line HIGH and waits for a stop (P) condition.

When the receiver generates a NACK; the slave leaves the data line HIGH and waits for P (the slave acting as if all data has been transmitted).

When all data has been transmitted, the data line remains HIGH and the slave waits for P.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range with respect to V_{SS}	V_{DD}	−0,5 to	+15	V
Input voltage range	V_I	−0,5 to	(V_{DD}+0,5)	V*
Input current	$\pm I_I$	max.	10	mA
Output voltage range	V_O	−0,5 to	(V_{DD}+0,5)	V*
Output current	$\pm I_O$	max.	10	mA
Power dissipation output OSCO	P_O	max.	50	mW
Power dissipation per output (all other outputs)	P_O	max.	100	mW
Total power dissipation per package	P_{tot}	max.	200	mW
Operating ambient temperature range	T_{amb}	−25 to	+85	°C
Storage temperature range	T_{stg}	−55 to	+150	°C

HANDLING

Inputs and outputs are protected against electrostatic charge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see "Handling MOS Devices").

DEVELOPMENT DATA

* V_{DD} + 0,5 V not to exceed 15 V.

CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = −25 to 85 °C unless otherwise specified

parameter	V_{DD} (V)	symbol	min.	typ.	max.	unit
Supply voltage	–	V_{DD}	4,5	–	5,5	V
Supply current; quiescent at T_{amb} = 25 °C	5,5	I_{DD}	–	–	200	μA
Inputs						
MA0, MA1, MA2, DATA 1, DATA 2, RC5, SCL, ENB, SSB, OSCI						
Input voltage HIGH	4,5 to 5,5	V_{IH}	0,7 x V_{DD}	–	V_{DD}	V
Input voltage LOW	4,5 to 5,5	V_{IL}	0	–	0,3 x V_{DD}	V
Input leakage current at V_I = 5,5 V; T_{amb} = 25 °C	5,5	I_I	–	–	1	μA
Input leakage current at V_I = 0 V; T_{amb} = 25 °C;	5,5	$-I_I$	–	–	1	μA
Outputs						
DAV, PO						
Output voltage LOW at I_{OL} = 1,6 mA	4,5 to 5,5	V_{OL}	–	–	0,4	V
Output leakage current at V_O = 5,5 V; T_{amb} = 25 °C	5,5	I_{OR}	–	–	1	μA
OSCO						
Output voltage HIGH at $-I_{OH}$ = 0,2 mA	4,5 to 5,5	V_{OH}	V_{DD} − 0,5	–	–	V
Output voltage LOW at I_{OL} = 0,3 mA	4,5 to 5,5	V_{OL}	–	–	0,4	V
Output leakage current at T_{amb} = 25 °C; V_O = 5,5 V	5,5	I_{OR}	–	–	1	μA
V_O = 0 V	5,5	I_{OR}	–	–	1	μA
SDO						
Output voltage LOW at I_{OL} = 2 mA	4,5 to 5,5	V_{OL}	–	–	0,4	V
Output leakage current at V_O = 5,5 V; T_{amb} = 25 °C	5,5	I_{OR}	–	–	1	μA
Oscillator						
Max. oscillator frequency (Fig. 8)	4,75	f_{OSCI}	500	–	–	kHz

ENHANCED COMPUTER CONTROLLED TELETEXT CIRCUIT (ECCT)

GENERAL DESCRIPTION

The SAA5243 is a MOS N-channel integrated circuit which performs all the digital logic functions of a 625-line World System Teletext decoder. It operates in conjunction with the teletext video processor SAA5231, standard static RAMs and is controlled via the 2-wire I²C bus. The device can be used to provide videotex display conforming to a serial character attribute protocol.

Features

- Microcomputer controlled for flexibility
- High quality flicker-free display using a 12 x 10 character matrix
- Field flyback (lines 2 to 22), or full channel (all lines) data acquisition
- Up to four simultaneous page requests enabling acquisition during one magazine cycle
- Direct interface up to 8 K bytes static RAM
- Automatic language section of up to seven different languages
- 25th display row for software generated status messages
- Cursor control for videotex/telesoftware
- 7-bits parity or 8-bit data acquisition
- Extension packet reception option
- Standard I²C bus slave transceiver (slave address 0010001)
- Single 5 volt power supply
- Mask programmable character sets
- Slave sync mode operation
- $\overline{\text{Odd}}$/even field output for de-interlaced displays

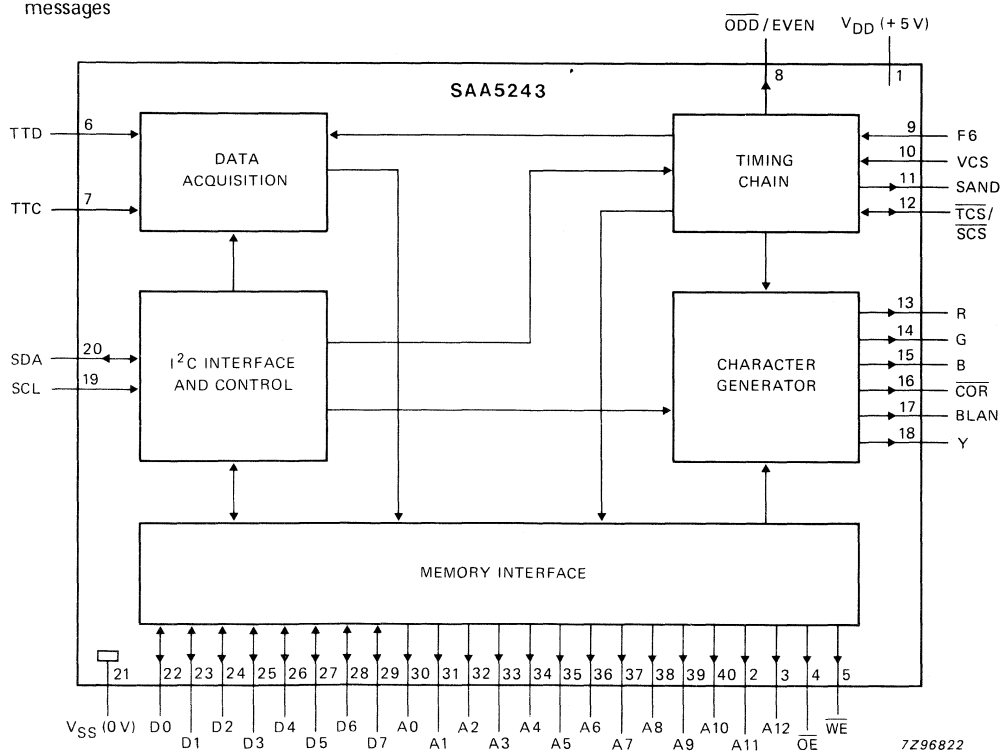


Fig. 1 Block diagram.

PACKAGE OUTLINES 40-lead DIL; plastic (SOT-129).

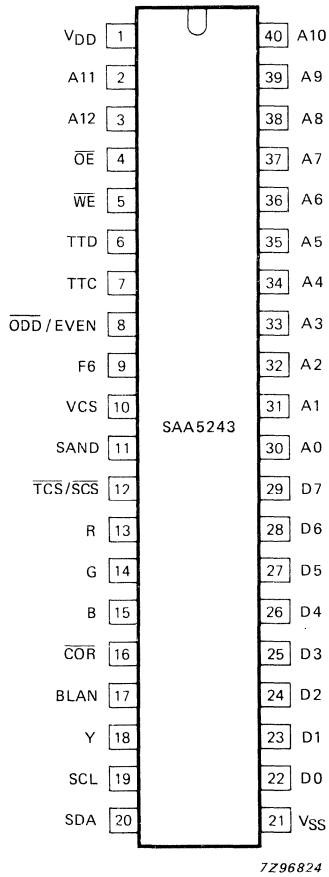


Fig. 2 Pinning diagram.

PINNING

1	V_{DD}	**Power supply**: + 5 V power supply pin.
2, 3, 40	A11, A12, A10	**Chapter Address**: three outputs that select which 1 K byte chapter of external RAM is being accessed for any read or write cycle.
4	$\overline{OE}$	**Output Enable**: active low output signal used to control the reading of the external RAM. It occurs continuously at a 1 MHz rate.
5	$\overline{WE}$	**Write Enable**: active low output signal used to control the writing of data to the external RAM. It occurs for a valid write cycle only and is interleaved with the read cycles.
6	TTD	**Teletext Data**: input from the SAA5231 Video Input Processor (VIP2). It is clamped to V_{SS} for 4 to 8 μs of each television line to maintain the correct d.c. level following the external a.c. coupling.

7	TTC	**Teletext Clock**: 6,9375 MHz clock input from the SAA5231. It is internally a.c. coupled to an active clamp input buffer.
8	$\overline{\text{ODD}}$/EVEN	**$\overline{\text{Odd}}$/Even**: for interlaced mode, the output changes once per field at 2 μs before the end of line 311 (624). The output is high for even fields and low for odd fields.
9	F6	**Character display clock**: 6 MHz clock input from the SAA5231. It is internally a.c. coupled to an active clamp input buffer.
10	VCS	**Video Composite Sync**: input from the SAA5231 derived from the incoming video signal. Sync pulses are active high.
11	SAND	**Sandcastle**: 3-level sandcastle output to the SAA5231 containing the phase locking and colour burst blanking information.
12	$\overline{\text{TCS}}$/$\overline{\text{SCS}}$	**Text Composite Sync/Scan Composite Sync**: as an output an active low composite sync waveform (TCS) with interlaced or non-interlaced format (see Fig. 6) which is fed to the SAA5231 to drive the display timebases. Alternatively this pin can act as an input for an active low composite sync waveform (SCS) to 'slave' the display timing circuits.
13, 14, 15	R, G, B	**Red, Green, Blue:** these 3 open drain outputs are the character video signals to the television display circuits. They are active high and contain character and background information.
16	$\overline{\text{COR}}$	**Contrast Reduction**: open drain, active low output which allows selective contrast reduction of the television picture to enhance a mixed mode display.
17	BLAN	**Blanking**: open drain, active high output which controls the blanking of the television picture for a normal text display and for a mixed display.
18	Y	**Character foreground**: open drain, active high video output signal containing all the foreground information displayed on the television screen (e.g. for driving a display printer).
19	SCL	**Serial Clock**: input signal which is the I^2C bus clock from the microcontroller.
20	SDA	**Serial Data**: is the I^2C bus data line. It is an input/output function with an open drain output.
21	V_{SS}	**Ground**: 0 volts.
22-29	DO-D7	**8 RAM data lines**: 3-state input/output pins which carry the data bytes to and from the external RAM.
30-39	A0-A9	**RAM address**: 10 output signals that determine which byte location within a 1 K byte chapter of external RAM is accessed for any read or write cycle.

DEVELOPMENT DATA

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range (pin 1)	V_{DD}	−0,3 to + 7,5	V
Input voltage range			
VCS, SDA, SCL, D0-D7	V_I	−0,3 to + 7,5	V
TTC, TTD, F6, $\overline{TCS}$/$\overline{SCS}$	V_I	−0,3 to + 10,0	V
Output voltage range			
SAND, A0-A12, $\overline{OE}$, $\overline{WE}$, D0-D7, SDA, $\overline{ODD}$/EVEN, R, G, B, BLAN, $\overline{COR}$, Y	V_O	−0,3 to + 7,5	V
$\overline{TCS}$/$\overline{SCS}$	V_O	−0,3 to + 10,0	V
Storage temperature range	T_{stg}	−20 to + 125	°C
Operating ambient temperature range	T_{amb}	−20 to + 70	°C

DEVELOPMENT DATA

CHARACTERISTICS

V_{DD} = 5 V ± 10%; V_{SS} = 0 V; T_{amb} = −20 to + 70 °C unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
SUPPLY					
Supply voltage (pin 1)	V_{DD}	4,5	5,0	5,5	V
Supply current (pin 1)	I_{DD}	–	160	270	mA
INPUTS (note 1)					
TTD (note 2)					
External coupling capacitor	C_{ext}	–	–	50	nF
Input voltage (peak-to-peak value)	$V_{I(p-p)}$	2,0	–	7,0	V
Input data rise and fall times (note 3)	t_r, t_f	10	–	80	ns
Input data set-up time (note 4)	t_{DS}	40	–	–	ns
Input data hold time (note 4)	t_{DH}	40	–	–	ns
Input leakage current at V_I = 0 to 10 V	I_{LI}	–	–	20	μA
Input capacitance	C_I	–	–	7	pF
TTC; F6 (note 5)					
D.C. input voltage range	V_I	−0,3	–	+ 10,0	V
A.C. input voltage (peak-to-peak value) F6	$V_{I(p-p)}$	1,0	–	7,0	V
A.C. input voltage (peak-to-peak value) TTC	$V_{I(p-p)}$	1,5	–	7,0	V
Input peaks relative to 50% duty cycle	± V_P	0,2	–	3,5	V
TTC clock frequency	f_{TTC}	–	6,9375	–	MHz
F6 clock frequency	f_{F6}	–	6,0	–	MHz
Clock rise and fall times (note 3)	t_r, t_f	10	–	80	ns
Input leakage current at V_I = 0 to 10 V	I_{LI}	–	–	20	μA
Input capacitance	C_I	–	–	7	pF
VCS					
Input voltage LOW	V_{IL}	0	–	0,8	V
Input voltage HIGH	V_{IH}	2,0	–	V_{DD}	V
Input rise and fall times (note 3)	t_r, t_f	–	–	500	ns
Input leakage current at V_I = 5,5 V	I_{LI}	–	–	10	μA
Input capacitance	C_I	–	–	7	pF

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
SCL					
Input voltage LOW	V_{IL}	0	–	1,5	V
Input voltage HIGH	V_{IH}	3,0	–	V_{DD}	V
SCL clock frequency	f_{SCL}	0	–	100	kHz
Input rise and fall times (note 3)	t_r, t_f	–	–	2	μs
Input leakage current at V_I = 5,5 V	I_{LI}	–	–	10	μA
Input capacitance	C_I	–	–	7	pF
INPUT/OUTPUTS (note 6)					
$\overline{TCS}$ (output)/$\overline{SCS}$ (input)					
Input voltage LOW	V_{IL}	0	–	1,5	V
Input voltage HIGH	V_{IH}	3,5	–	10,0	V
Input rise and fall times (note 3)	t_r, t_f	–	–	500	ns
Input leakage current at V_I = 0 to 10 V and output in high impedance state	$\pm I_{LI}$	–	–	10	μA
Input capacitance	C_I	–	–	7	pF
Output voltage LOW at I_{OL} = 0,4 mA	V_{OL}	0	–	0,4	V
Output voltage HIGH					
at $-I_{OH}$ = 0,2 mA	V_{OH}	2,4	–	V_{DD}	V
at I_{OH} = 0,1 mA	V_{OH}	2,4	–	6,0	V
Output rise and fall times between 0,6 V and 2,2 V levels	t_r, t_f	–	–	100	ns
Load capacitance	C_L	–	–	50	pF
SDA (note 7)					
Input voltage LOW	V_{IL}	0	–	1,5	V
Input voltage HIGH	V_{IH}	3,0	–	V_{DD}	V
Input rise and fall times (note 3)	t_r, t_f	–	–	2	μs
Input leakage current at V_I = 5,5 V with output off	I_{LI}	–	–	10	μA
Input capacitance	C_I	–	–	7	pF
Output voltage LOW at I_{OL} = 3 mA	V_{OL}	0	–	0,5	V
Output fall time between 3,0 V and 1,0 V levels	t_f	–	–	200	ns
Load capacitance	C_L	–	–	400	pF

DEVELOPMENT DATA

parameter	symbol	min.	typ.	max.	unit
INPUT/OUTPUTS (continued)					
D0-D7 (note 8)					
Input voltage LOW	V_{IL}	0	–	0,8	V
Input voltage HIGH	V_{IH}	2,0	–	V_{DD}	V
Input leakage current at V_I = 0 V to 5,5 V and output in high impedance state	$\pm I_{LI}$	–	–	10	μA
Input capacitance	C_I	–	–	7	pF
Output voltage LOW at I_{OL} = 1,6 mA	V_{OL}	0	–	0,4	V
Output voltage HIGH at $-I_{OH}$ = 0,2 mA	V_{OH}	2,4	–	V_{DD}	V
Output rise and fall times between 0,6 V and 2,2 V levels	t_r, t_f	–	–	50	ns
Load capacitance	C_L	–	–	120	pF
OUTPUTS (note 6)					
A0-A12; $\overline{OE}$; $\overline{WE}$ (note 8)					
Output voltage LOW at I_{OL} = 1,6 mA	V_{OL}	0	–	0,4	V
Output voltage HIGH at $-I_{OH}$ = 0,2 mA	V_{OH}	2,4	–	V_{DD}	V
Output rise and fall times between 0,6 V and 2,2 V levels	t_r, t_f	–	–	50	ns
Load capacitance	C_L	–	–	120	pF
$\overline{ODD}$/EVEN					
Output voltage LOW at I_{OL} = 0,4 mA	V_{OL}	0	–	0,4	V
Output voltage HIGH at $-I_{OH}$ = 0,2 mA	V_{OH}	2,4	–	V_{DD}	V
Output rise and fall times between 0,6 V and 2,2 V levels	t_r, t_f	–	–	100	ns
Load capacitance	C_L	–	–	50	pF
SAND (note 9)					
Output voltage LOW at I_{OL} = 0,2 mA	V_{OL}	0	–	0,25	V
Output voltage INTERMEDIATE at I_{OL} = ± 10 μA	V_{OI}	1,1	–	3,1	V

CHARACTERISTICS (continued)

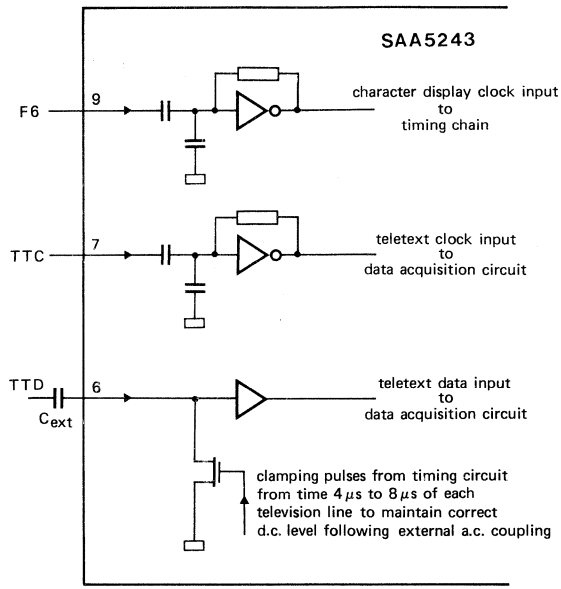
parameter	symbol	min.	typ.	max.	unit
SAND (continued)					
Output voltage HIGH at I_{OH} = 0 to −10 μA	V_{OH}	4,0	–	V_{DD}	V
Output rise time V_{OL} to V_{OI} between 0,4 V and 0,9 V levels	t_{r1}	–	–	400	ns
Output rise time V_{OI} to V_{OH} between 3,3 V and 3,8 V levels	t_{r2}	–	–	200	ns
Output fall time V_{OH} to V_{OL} between 3,8 V and 0,4 V levels	t_f	–	–	50	ns
Load capacitance	C_L	–	–	30	pF
R; G; B; $\overline{\text{COR}}$; BLAN; Y (note 10)					
Output voltage LOW at I_{OL} = 2 mA	V_{OL}	0	–	0,4	V
Output voltage LOW at I_{OL} = 5 mA	V_{OL}	0	–	1,0	V
Pull-up voltage as seen at pin	V_{PU}	–	–	6,0	V
Output fall time with a load resistor of 1,2 kΩ to 6 V and measured between 5,5 V and 1,5 V	t_f	–	–	20	ns
Skew delay between outputs with a load resistor of 1,2 kΩ to 6 V and measured on the falling edges at 3,5 V	t_{SK}	–	–	20	ns
Load capacitance	C_L	–	–	25	pF
Output leakage current at V_{PU} = 0 to 6 V with output off	I_{LO}	–	–	10	μA
TIMING					
I^2C bus (note 11)					
Clock low period	t_{LOW}	4	–	–	μs
Clock high period	t_{HIGH}	4	–	–	μs
Data set-up time	$t_{SU;DAT}$	250	–	–	ns
Data hold time	$t_{HD;DAT}$	170	–	–	ns
Stop set-up time from clock high	$t_{SU;STO}$	4	–	–	μs
Start set-up time following a stop	t_{BUF}	4	–	–	μs
Start hold time	$t_{HD;STA}$	4	–	–	μs
Start set-up time following clock low-to-high transition	$t_{SU;STA}$	4	–	–	μs

parameter	symbol	min.	typ.	max.	unit
TIMING (continued)					
Memory interface (note 12)					
Cycle time	t_{CY}	–	500	–	ns
Address change to $\overline{OE}$ LOW	t_{OE}	60	–	–	ns
Address active time	t_{ADDR}	450	500	–	ns
$\overline{OE}$ pulse duration	t_{OEW}	320	–	–	ns
Access time from $\overline{OE}$ to data valid	t_{ACC}	–	–	200	ns
Data hold time from $\overline{OE}$ HIGH or address change	t_{DH}	0	–	–	ns
Address change to $\overline{WE}$ LOW	t_{WE}	40	–	–	ns
$\overline{WE}$ pulse duration	t_{WEW}	200	–	–	ns
Data set-up time to $\overline{WE}$ HIGH	t_{DS}	100	–	–	ns
Data hold time from $\overline{WE}$ HIGH	t_{DHWE}	20	–	–	ns
Write recovery time	t_{WR}	25	–	–	ns

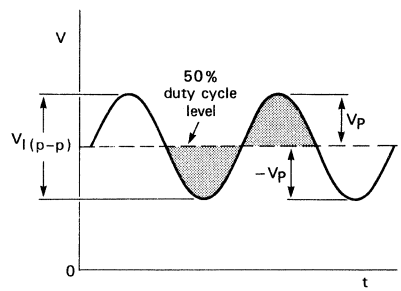
DEVELOPMENT DATA

Notes to the characteristics

1. All inputs are protected against static charge under normal handling.
2. The TTD input incorporates an internal clamping diode in addition to the active clamping transistor (see Fig. 3).
3. Rise and fall times between 10% and 90% levels.
4. Teletext input data set-up and hold times are with respect to a 50% duty cycle level of the rising edge of the teletext clock input (TTC). Data stable 1 $\geqslant$ 2,0 V; data stable 0 $\leqslant$ 0,8 V (see Fig. 4).
5. The TTC and F6 inputs have internal clamping diodes and are a.c. coupled (see Fig. 3).
6. All outputs and input/outputs are protected against static charge under normal handling and connection to V_{DD} and V_{SS}.
7. For details of I^2C bus timing see Fig. 8.
8. For details of RAM timing see Fig. 9.
9. For details of synchronization timing see Fig. 5.
10. For details of display output timing see Fig. 7.
11. The I^2C bus timings are referred to V_{IH} = 3 V and V_{IL} = 1,5 V. For waveforms see Fig. 8.
12. The memory interface timings are referred to V_{IL} = 1,5 V. For waveforms see Fig. 9.



(a)

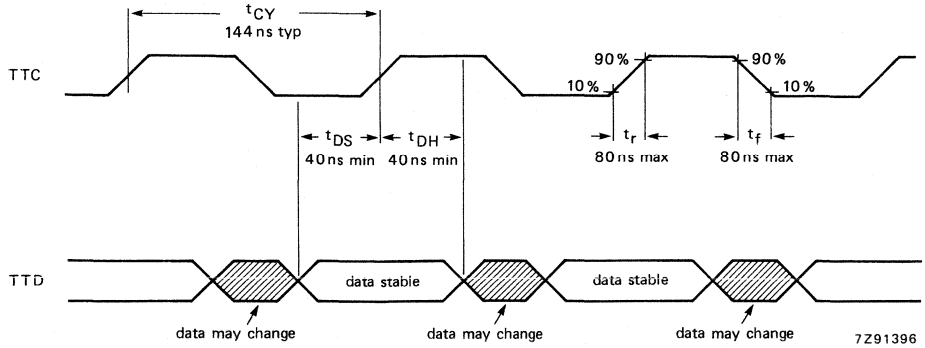


shaded regions equal in area

7Z91395.P

(b)

Fig. 3 (a) F6, TTC and TTD input circuitry (b) input waveform parameters.



Data stable: 1 is $\geqslant$ 2,0 V; 0 is $\leqslant$ 0,8 V.

Fig. 4 Teletext data input timing.

DEVELOPMENT DATA

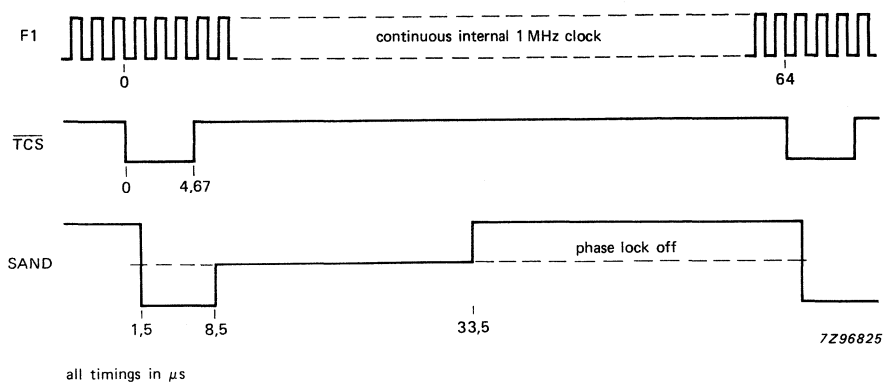
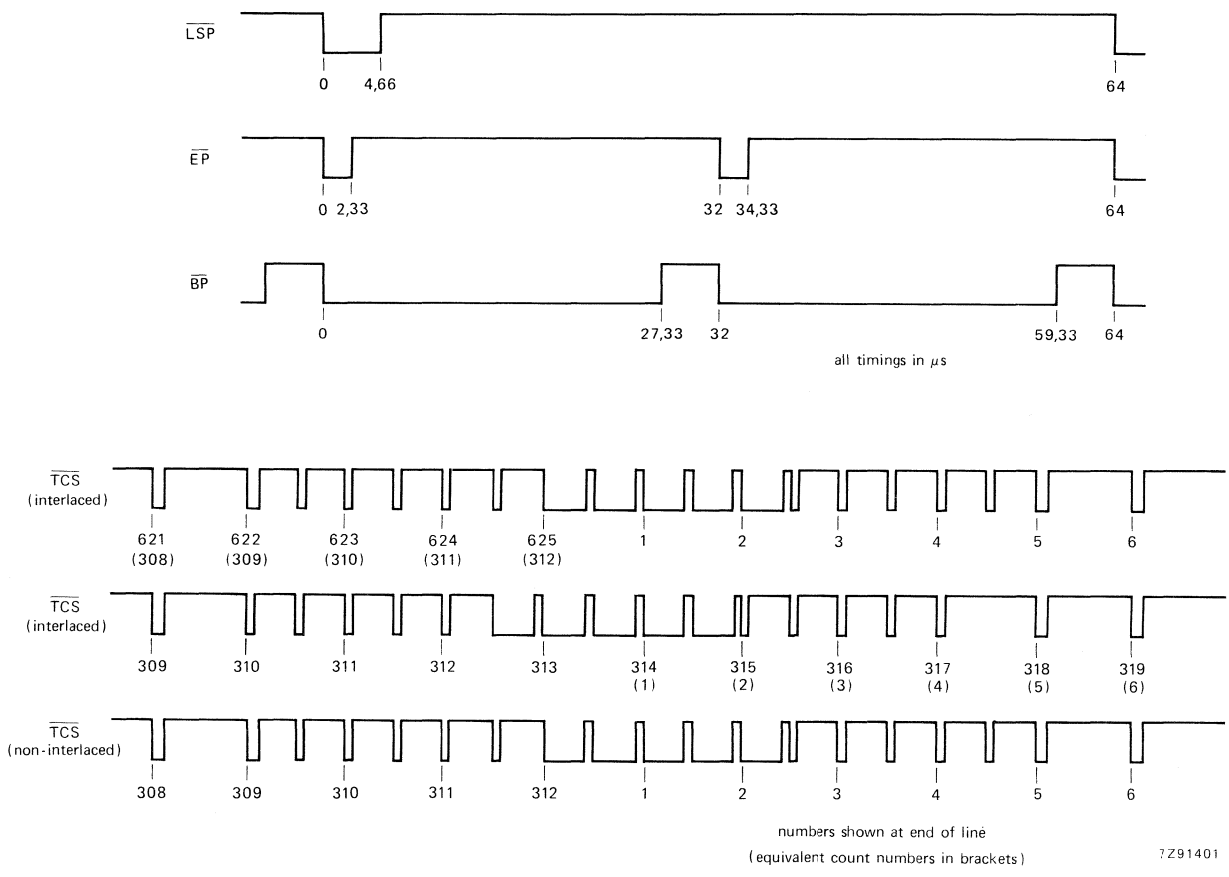


Fig. 5 Synchronization timing.



Line sync pulses ($\overline{LSP}$), equalizing pulses ($\overline{EP}$) and broad pulses ($\overline{BP}$) are combined to provide the text composite sync waveform ($\overline{TCS}$) as shown. All timings measured from falling edge of $\overline{LSP}$ with a tolerance of ± 100 ns.

Fig. 6 Composite sync waveforms.

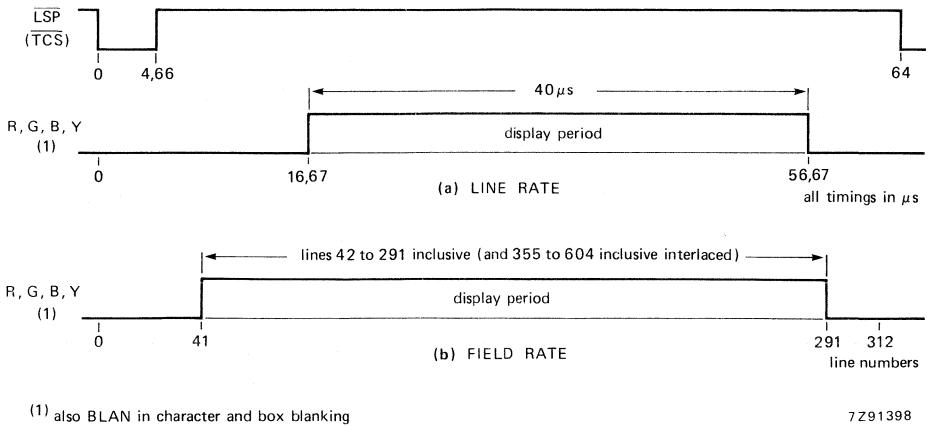


Fig. 7 Display output timing (a) line rate (b) field rate.

DEVELOPMENT DATA

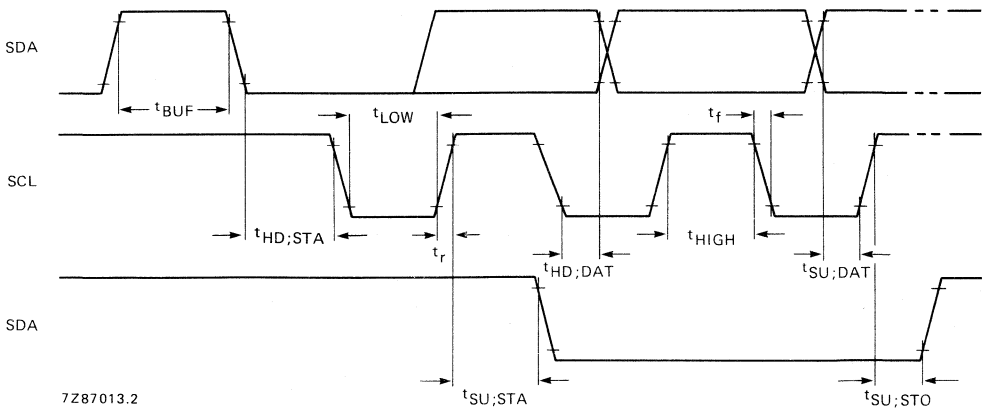


Fig. 8 I^2C bus timing.

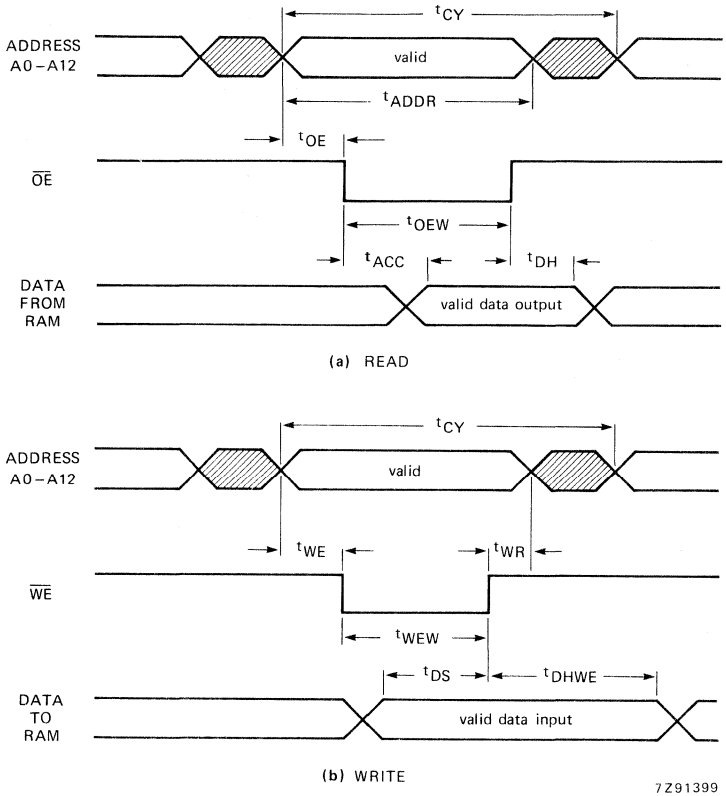
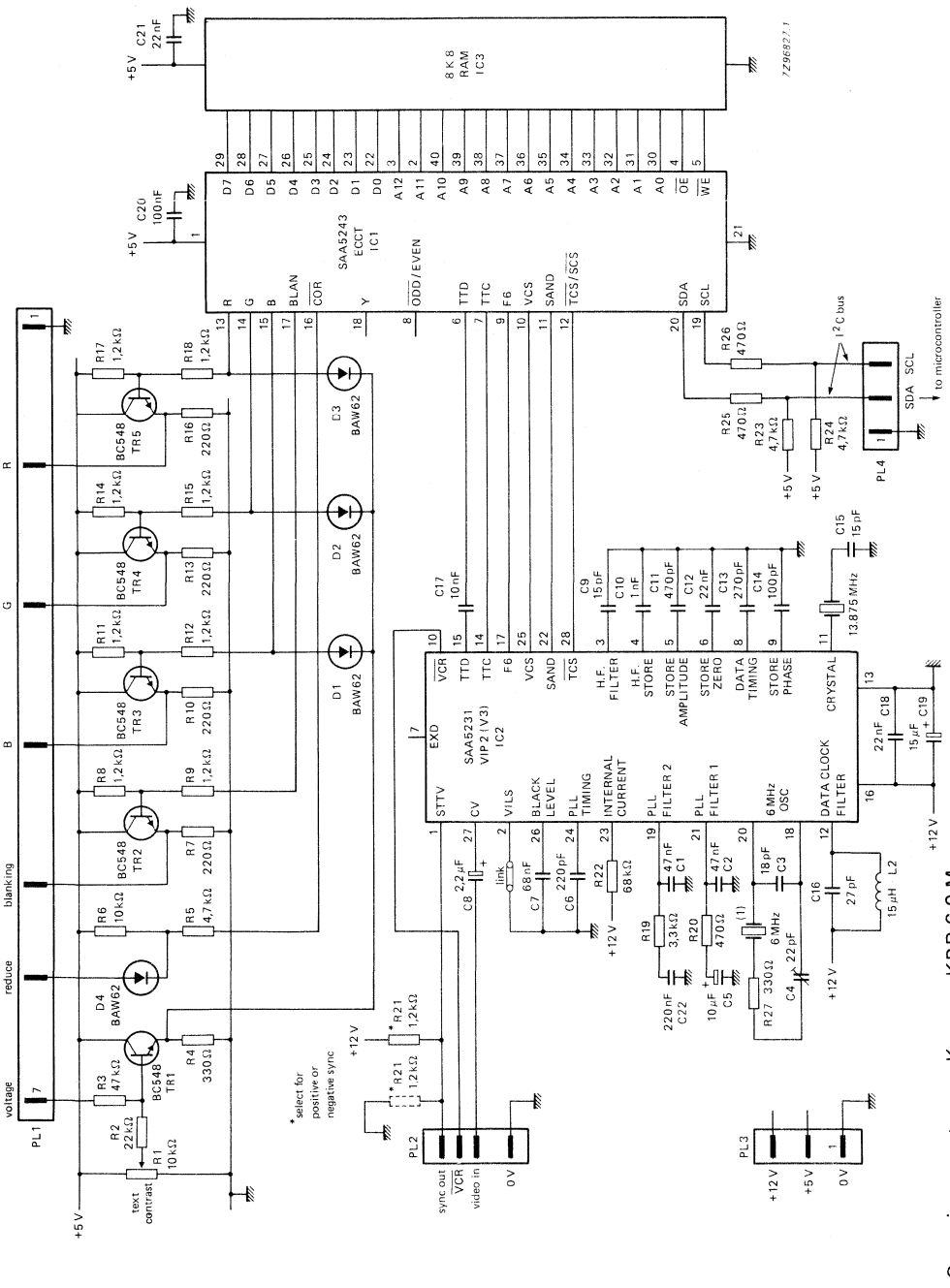


Fig. 9 Memory interface timing (a) read (b) write.

DEVELOPMENT DATA

APPLICATION INFORMATION



(1) Ceramic resonator e.g. Kyocera KBR 6,0 M.

Fig. 10 ECCT based multi-page decoder circuit diagram.

APPLICATION INFORMATION (continued)

ECCT page memory organization

The organization of a page memory is shown in Fig. 11. The ECCT provides an additional row compared with first generation decoders bringing the display format up to 40 characters by 25 rows. Rows 0 to 23 form the teletext page as broadcast and row 24 is the extra row available for user-generated status messages.

A MORE DETAILED DESCRIPTION OF ECCT OPERATION AND APPLICATION IS AVAILABLE ON REQUEST.

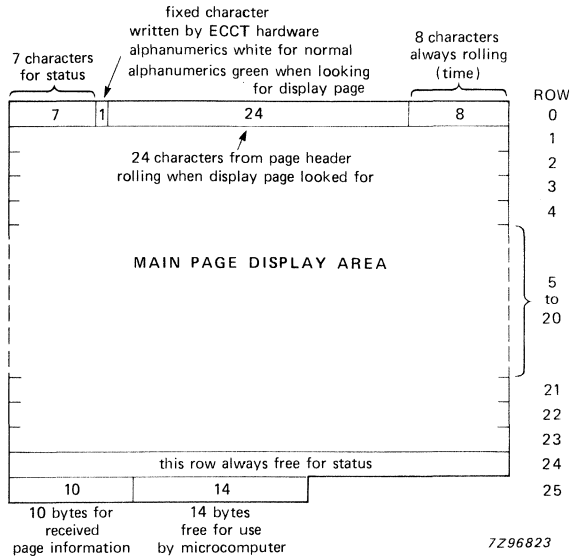


Fig. 11 Page memory organization.

Table 1 Row 25 received control data format

D0	PU0	PT0	MU0	MT0	HU0	HT0	C7	C11	MAG0	0
D1	PU1	PT1	MU1	MT1	HU1	HT1	C8	C12	MAG1	0
D2	PU2	PT2	MU2	MT2	HU2	C5	C9	C13	MAG2	0
D3	PU3	PT3	MU3	C4	HU3	C6	C10	C14	0	0
D4	HAM.ER	HAM.ER	HAM.ER	HAM.ER	HAM.ER	HAM.ER	HAM.ER	HAM.ER	$\overline{\text{FOUND}}$	0
D5	0	0	0	0	0	0	0	0	0	PBLF
D6	0	0	0	0	0	0	0	0	0	0
D7	0	0	0	0	0	0	0	0	0	0
Column	0	1	2	3	4	5	6	7	8	9

Where:

MAG	magazine	page number	MU	minutes units	page sub-code
PU	page units		MT	minutes tens	
PT	page tens		HU	hours units	
PBLF	page being looked for		HT	hours tens	
$\overline{\text{FOUND}}$	LOW for page has been found		C4-C14	transmitted control bits	
HAM.ER	Hamming error in corresponding byte				

Row 0

Row 0 is for the page header. The first seven columns (o to 6) are free for status messages. The eigth is an alphanumeric white or green control character, written automatically by ECCT to give a green rolling header when a page is being looked for. The last eight characters are for rolling time.

Row 25

The first 10 bytes of row 25 contain control data relating to the received page. Seven digits are used to identify a page as shown in Table 1. The remaining 14 bytes are free for use by the microcomputer.

Register maps

ECCT mode registers R1 to R11 are shown in Table 2. R1 to R10 are WRITE only; R11 is READ/WRITE.
Register map (R3), for page requests, is shown in detail in Table 3.

Table 2 ECCT register map

D7	D6	D5	D4	D3	D2	D1	D0		
TA	$\overline{7+P}$/ 8 BIT	ACQ. $\overline{ON}$/OFF	GHOST ROW ENABLE	$\overline{DEW}$/ FULL FIELD	TCS ON	T1	T0	R1	Mode
–	BANK SELECT A2	ACQ. CCT A1	ACQ. CCT A0	TB	START COLUMN SC2	START COLUMN SC1	START COLUMN SC0	R2	Page request address
–	–	–	PRD4	PRD3	PRD2	PRD1	PRD0	R3	Page request data
–	–	–	–	–	A2	A1	A0	R4	Display chapter
BKGND OUT	BKGND IN	COR OUT	COR IN	TEXT OUT	TEXT IN	PON OUT	PON IN	R5	Display control (normal)
BKGND OUT	BKGND IN	COR OUT	COR IN	TEXT OUT	TEXT IN	PON OUT	PON IN	R6	Display control (newsflash/subtitle)
STATUS ROW $\overline{BTM}$/TOP	CURSOR ON	$\overline{CONCEAL}$/ REVEAL	$\overline{TOP}$/ BOTTOM	$\overline{SINGLE}$/ DOUBLE HEIGHT	BOX ON 24	BOX ON 1-23	BOX ON 0	R7	Display mode
–	–	–	–	CLEAR MEM.	A2	A1	A0	R8	Active chapter
–	–	–	R4	R3	R2	R1	R0	R9	Active row
–	–	C5	C4	C3	C2	C1	C0	R10	Active column
D7 (R/W)	D6 (R/W)	D5 (R/W)	D4 (R/W)	D3 (R/W)	D2 (R/W)	D1 (R/W)	D0 (R/W)	R11	Active data

– bit does not exist

DEVELOPMENT DATA

Notes to Table 2

The arrows shown on the right of the register map indicate that the register auto-increments to the next one on the following I^2C transmission byte. TA and TB must be logic 0 for normal operation.
All bits in registers R1 to R10 are cleared to logic 0 on power-up except bits D0 and D1 of registers R5 and R6 which are set to logic 1.
All memory is cleared to 'space' (00100000) on power-up, except row 0 column 7 chapter 0, which is 'alpha white' (00000111) as the acquisition circuit is enabled but all pages are on hold.

APPLICATION INFORMATION (continued)

Table 2 (continued)

Where:

R1 Mode

T0, T1	interlace/non-interlace 312/313 line control
TCS ON	text composite sync or direct sync select
$\overline{\text{DEW}}$/FULL FIELD	field-flyback or full channel mode
7 + P/8 BIT	7 bits with parity checking or 8-bit mode
TA, TB	test bits; 0 for normal operation

R2 Page request address

START COLUMN	start column for page request data
ACQ CCT	selects one of four acquisition circuits
BANK SELECT	selects bank of four pages being addressed for acquisition
R3 Page request data	see Table 3
R4 Display chapter	determines which of the 8 pages is displayed
R5, R6 Display control	for normal and newsflash/subtitle
PON	picture on
TEXT	text on
COR	contrast reduction on
BKGND	background colour on

These functions have IN and OUT referring to inside and outside the boxing function respectively.

R7 Display mode

BOX ON 0 (1-23, 24)	boxing function allowed on row 0 (row 1-23, 24)
STATUS ROW $\overline{\text{BTM}}$/TOP	row 25 displayed above or below the main text
R8 to R11	active chapter, row, column and data information written to or read from page memory via the I^2C bus.

Table 3 Register map for page requests (R3)

Start Column	PRD4	PRD3	PRD2	PRD1	PRD0
0	Do care Magazine	$\overline{\text{HOLD}}$	MAG2	MAG1	MAG0
1	Do care Page tens	PT3	PT2	PT1	PT0
2	Do care Page units	PU3	PU2	PU1	PU0
3	Do care Hours tens	X	X	HT1	HT0
4	Do care Hours units	HU3	HU2	HU1	HU0
5	Do care Minutes tens	X	MT2	MT1	MT0
6	Do care Minutes units	MU3	MU2	MU1	MU0

Notes to Table 3

Abbreviations are as for Table 1 except for D0 CARE bits.
When the D0 CARE bit is set to logic 1 this means the corresponding digit is to be taken into account for page requests. If the D0 CARE bit is set to logic 0 the digit is ignored. This allows, for example, 'normal' or 'timed page' selection.
If $\overline{\text{HOLD}}$ is set LOW, the page is held and not updated.
There are four groups of data shown in Table 3, one for each acquisition circuit (four simultaneous page requests).
Columns auto-increment on successive I^2C transmission bytes.

DEVELOPMENT DATA

APPLICATION INFORMATION (continued)

CHARACTER SETS

The UK teletext specification allows the selection of national character sets via the page header transmission bits, C12 to C14 as shown in Table 4. The basic 96 character sets differs only in the 13 national option characters as indicated in Table 7 with reference to their table position in the basic character matrix shown in Table 6. ECCT automatically decodes transmission bits C12 to C14. Other combinations of C12 to C14 are defaulted to English in SAA5243P/E. With 8-bit decoding the character matrices are shown in Table 5.

Table 4 Selection of national character sets (SAA5243P/E)

PHCB	ENGLISH	GERMAN	SWEDISH	ITALIAN	FRENCH	SPANISH
C12	0	0	0	0	1	1
C13	0	0	1	1	0	0
C14	0	1	0	1	0	1

Where:

PHCB page header control bits.

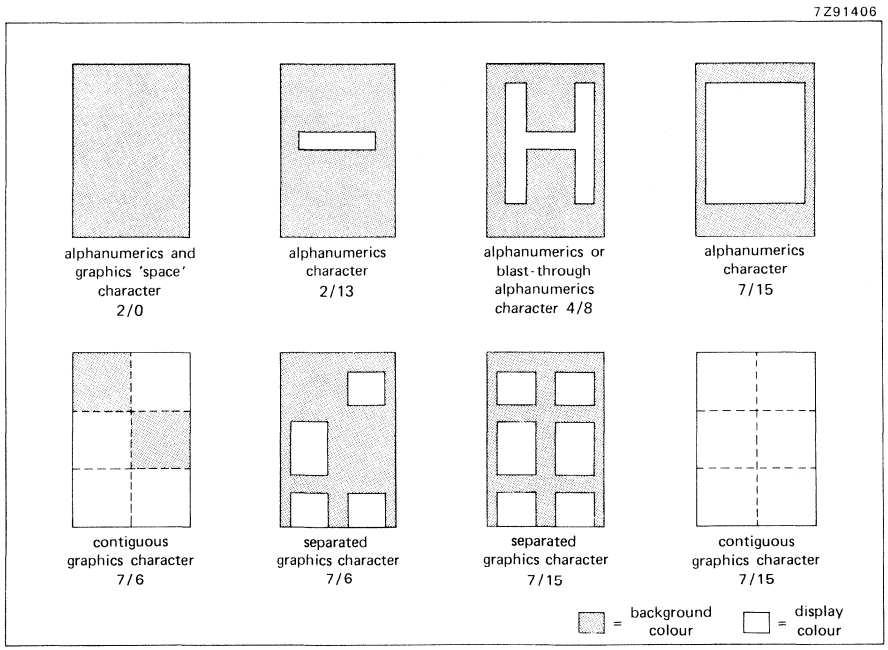


Fig. 12 Character format.

Table 5 Character data input decoding (SAA5243E)

BITS b8	0	0	0 or 1		0 or 1		0	0	0		0		1	1	1	1	1	1
b7	0	0	1		1		0	1	1		1		0	0	1	1	1	1
b6	0	0	0		0		1	0	1		1		0	0	1	1	1	1
b5	0	1	0		1		0	0	0		1		0	1	0	1	0	1
b4 b3 b2 b1 ↓ ↓ ↓ ↓ row / column →	0	1	2	2a	3	3a	4	5	6	6a	7	7a	8	9	12	13	14	15
0 0 0 0	0	alpha–numerics black	graphics black															
0 0 0 1	1	alpha–numerics red	graphics red															
0 0 1 0	2	alpha–numerics green	graphics green															
0 0 1 1	3	alpha–numerics yellow	graphics yellow															
0 1 0 0	4	alpha–numerics blue	graphics blue															
0 1 0 1	5	alpha–numerics magenta	graphics magenta															
0 1 1 0	6	alpha–numerics cyan	graphics cyan															
0 1 1 1	7	** alpha–numerics white	graphics white															
1 0 0 0	8	flash	conceal display															
1 0 0 1	9	** steady	** contiguous graphics															
1 0 1 0	10	** end box	separated graphics															
1 0 1 1	11	start box	* ESC															
1 1 0 0	12	** normal height	** black back–ground															
1 1 0 1	13	double height	new back–ground															
1 1 1 0	14	* SO	hold graphics															
1 1 1 1	15	* SI	** release graphics															

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DEVELOPMENT DATA

* These control characters are reserved for compatibility with other data codes.

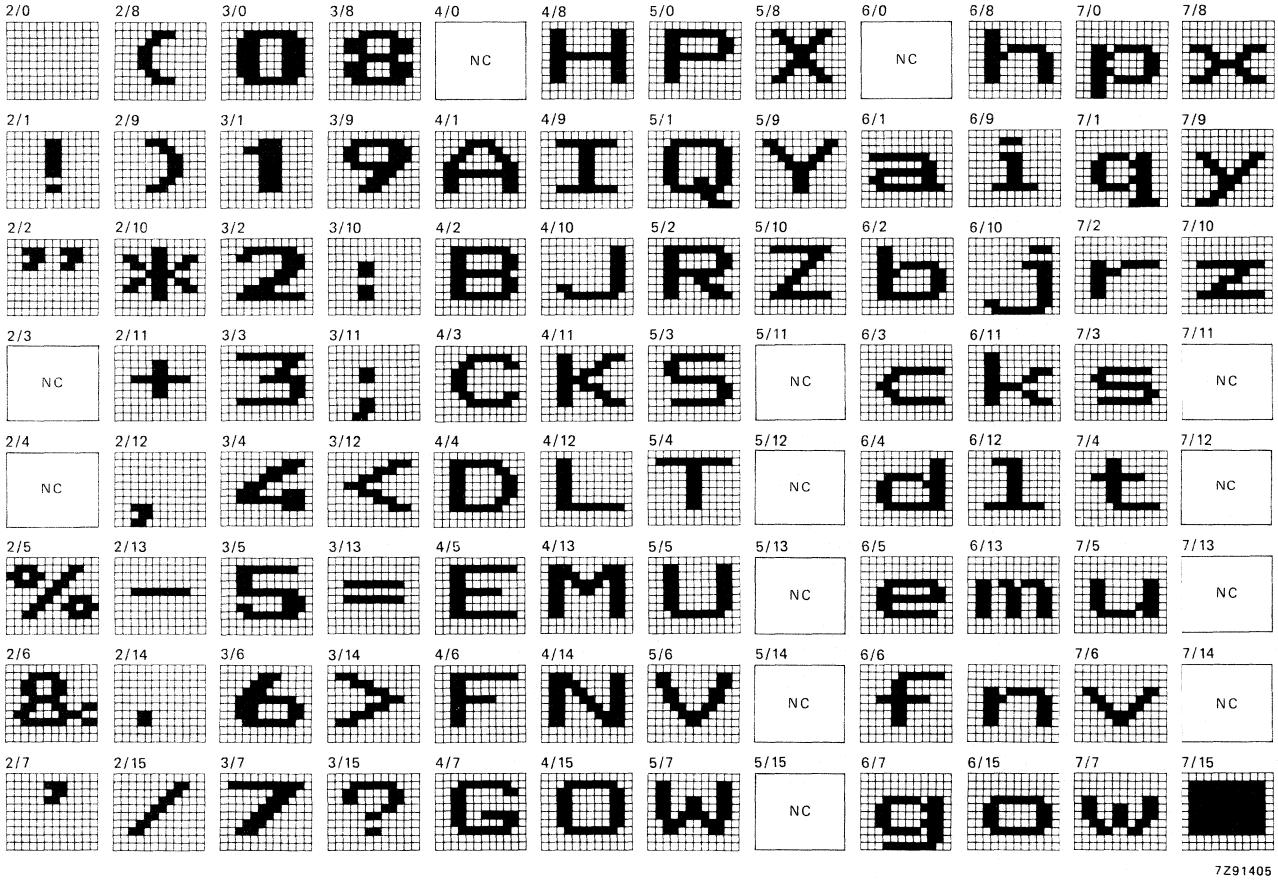
** These control characters are presumed before each row begins.

APPLICATION INFORMATION (continued)

Notes to Table 5

1. Control characters shown in columns 0 and 1 are normally displayed as spaces.
2. Codes may be referred to by column and row. For example 2/5 refers to %.
3. Black represents displayed colour. White represents background.
4. Character rectangle shown as follows: □
5. The SAA5243E national option characters are shown in Table 7.
6. Characters 8/6, 8/7, 9/5, 9/6 and 9/7 are special characters to combine with character 8/5.
7. With bit 8 = 0 national option characters will be decoded according to the setting of control bits C12 to C14 (see Table 4).

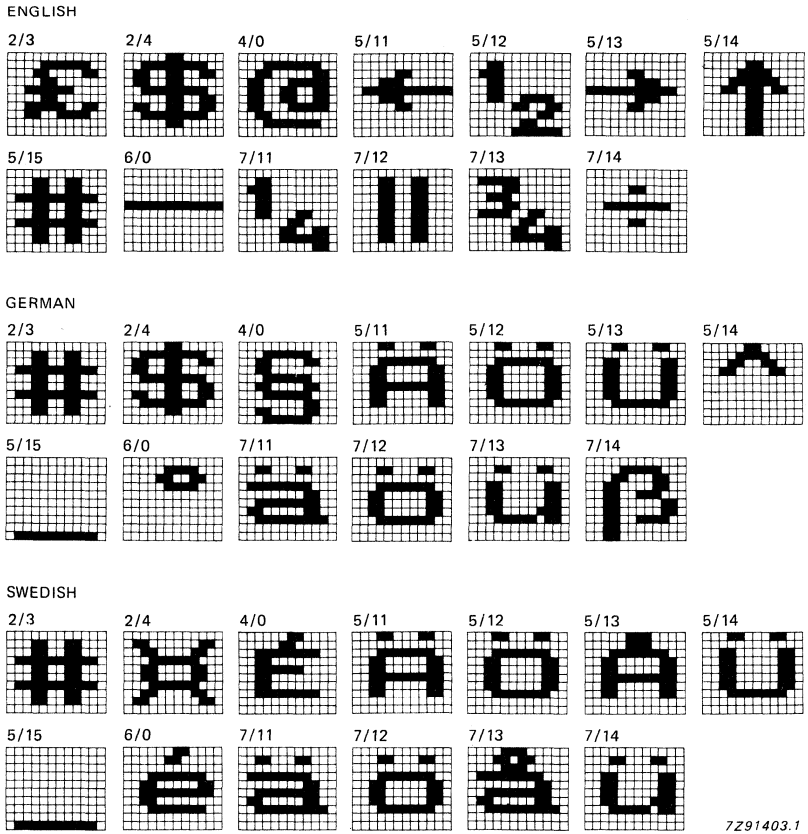
Table 6 SAA5243 basic character matrix



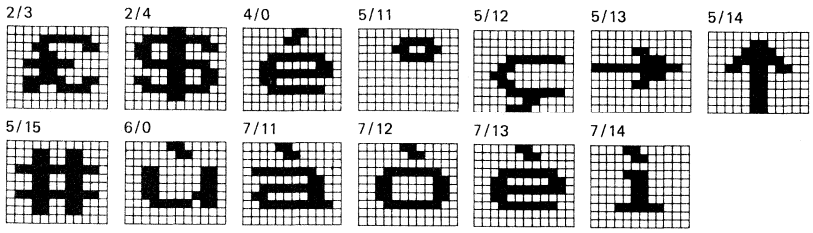
Where: NC national option character position.

APPLICATION INFORMATION (continued)

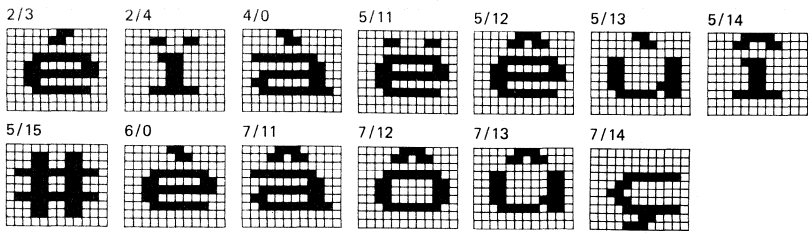
Table 7 SAA5243E character set (national option characters)



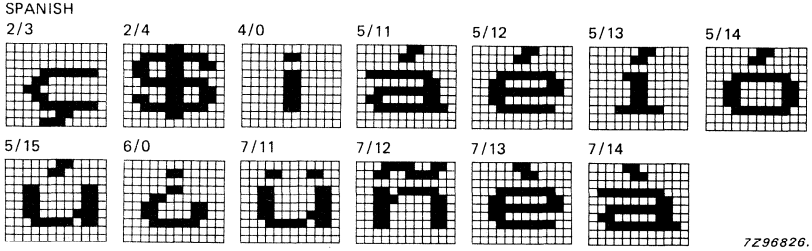
ITALIAN



FRENCH



SPANISH



7Z96826.1

FIELD MEMORY CONTROLLER

The SAA9020 field memory controller (FMC), a 24-pin CMOS integrated circuit, is for application in memory-based feature tv receivers. It is part of the field memory system for providing picture quality enhancement. The SAA9020 provides the system I^2C bus interface and is used to control the picture enhancement processor (SAA9010) and the system field memory.

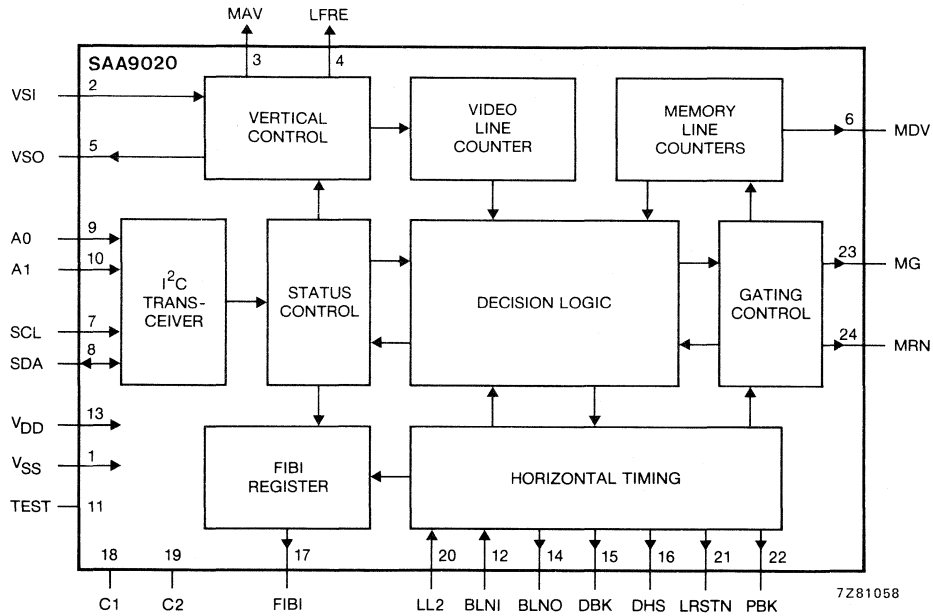


Fig. 1 Block diagram.

PACKAGE OUTLINE

24-lead DIL; plastic (SOT-101A).

PINNING

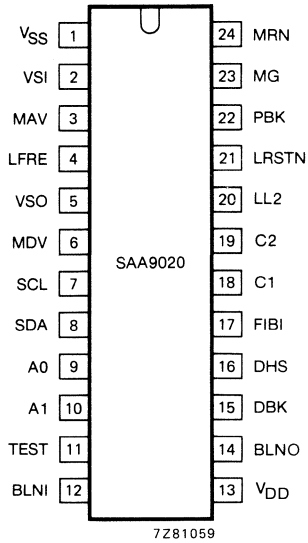


Fig. 2 Pinning diagram.

1	V_{SS}	negative supply voltage (0 V)
2	VSI	vertical synchronization input pulse
3	MAV	memory above video output signal that indicates the memory contents being processed were spatially above the incoming video
4	LFRE	line flicker reduction enable. This output signal indicates that a standard field length has been received
5	VSO	vertical synchronizing output. This is a delayed vertical synchronizing pulse that is HIGH for 14 to 15 line-periods and is derived from VSI or internal memory counters, depending on the mode of operation
6	MDV	memory data valid output. This is HIGH during the period when the outputs from the memories are known to be valid, i.e. during store/recall and still picture
7	SCL	serial clock input for the I^2C bus transceiver
8	SDA	serial data input/output and acknowledge output for I^2C bus transceiver
9, 10	A0, A1	address inputs for the I^2C bus transceiver. Normally hard-wired to a fixed address
11	TEST	connected to V_{SS} for normal operation
12	BLNI	blanking input. A rising edge of this input resets the horizontal timing of the FMC
13	V_{DD}	positive supply voltage (+ 5 V). Requires external decoupling to V_{SS}
14	BLNO	blanking output. This signal is LOW during vertical and horizontal flyback periods and when undefined data is expected from the picture enhancement processor (SAA9010

15	DBK	delayed burst key output. To correct signal processing delays the position of DBK can be adjusted by the programmable output delay with respect to BLNO
16	DHS	delayed horizontal synchronization pulse output. To correct signal processing delays the position of DHS can be adjusted by the programmable output delay with respect to BLNO
17	FIBI	format identification, blanking and instruction output. Indicates the format (order) of the video samples and carries instructions to control the picture enhancement processor (SAA9010)
18, 19	C1, C2	pins for connecting an external decoupling capacitor (low inductance type), C1 = V_{DD} and C2 = V_{SS}
20	LL2	20,25 MHz line-locked clock input
21	LRSTN	line reset output pulse
22	PBK	phase-reference burst key output. The duty factor of this output is typically 50% and the timing of the rising edge can be adjusted by the programmable input delay
23	MG	memory gating output to the field memories to control data input, output and line shifting. This output is set to float when the background memory function is requested and by power-on-reset
24	MRN	memory refresh control output to the field memories. This output is set to float when a background memory function is requested and by power-on-reset

FUNCTIONAL DESCRIPTION

Operation

The main task of the FMC is to control the synchronism between incoming video, memory data and the display. During store/recall picture and still picture, where a field of video has been stored in the memories, the memories are not synchronized to the incoming video; when the memory contents are displayed the display synchronism is controlled by the memory counters and not by the incoming video.

The FMC communicates with the PEP via the FIBI signal and controls the memories via the MG and MRN signals. Communication with the FMC is made via the I^2C transceiver which is also used to set up certain FIBI data.

Other functions of the field memory controller are:

- to execute commands for changes of system operating modes by controlling the internal status of the PEP and the drive signals of the field memories;
- to divide the clock frequency (LL2) to the applicable line frequency;
- to pass the vertical sync pulse to the deflection circuits or, if necessary, to generate its own vertical sync pulse (e.g. for stored picture display);
- to delay the horizontal drive and the clamp pulse for the RGB processing and compensate for delays to the video signal in the PEP;
- to provide the means of making the system independent of tv standards (an important aspect of this function is its control of the virtual memory length).

There are six modes of operation, one of which releases control of the memories for other uses such as background text storage. The remaining five modes are direct video, store/recall picture, still picture, cross-colour reduction and noise reduction.

FUNCTIONAL DESCRIPTION (continued)

Operation (continued)

In the direct video mode no processing of memory data is performed and the PEP is instructed to pass unprocessed video data direct. The memories are controlled in such a way that they are reloaded with each new field of video.

Store/recall and still picture modes hold a field of video in the memories. If noise or cross-colour reduction was previously active then a processed picture will be stored. Once a picture has been fully stored the PEP is instructed to pass direct unprocessed video. The stored picture will be brought into view on the command 'recall picture', this is a toggle function and may be used to 'restore' this picture and display direct video or to display the stored picture. Freeze picture is the combined operation of store and recall.

The cross-colour reduction mode causes the PEP and memories to be controlled as a transversal filter for the U and V samples of the video. The mode can be for PAL or NTSC in that the memory data is either compared with the video line spatially above or spatially below. It is only active for standard length fields.

In the noise reduction mode recursive filtering is established for all video samples. The option for high-level or low-level noise reduction has no influence on the functioning of the FMC. Noise reduction is only active for the number of active video lines stored in memory, otherwise direct video is passed through.

In the cross-colour and noise reduction modes the memories have to be synchronized with the incoming video to ensure the correct processing and display of the data.

The FMC ensures that during any change of operating mode the correct synchronism is obtained before instructing the PEP to change mode. The mode change will be forced in extreme cases where synchronism cannot be obtained within 32 fields.

I^2C write mode

The I^2C message to the FMC comprises three or more bytes. The first contains the FMC address (0 0 1 0 1 A1 A0, where A1 and A0 are hard-wired externally). This byte is always acknowledged when the correct address is received. The second byte addresses one of three data registers, receipt of the correct address is acknowledged unless the FMC is busy with a status change. The third and subsequent bytes are data bytes which, if received, will only be acknowledged and loaded if the FMC is not busy with a requested status change initiated via bits S3 to S0.

The first data byte is loaded into the addressed register. The address is incremented for each data byte received until the third register is loaded, then the address remains at the third register until a new address is specified at the start of a new transmission.

FMC register address	contents msb							lsb	status after power-on-reset
0 0 0 0 0 0 0 0	TVL	VW	B2	B1	B0	H2	H1	H0	0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 1	Y4	Y3	Y2	Y1	Y0	TST	INT	FTST	0 0 0 0 1 0 0 0
0 0 0 0 0 0 1 0	FA	MBL	F1	F0	S3	S2	S1	S0	0 0 0 0 1 0 0 0

New data for TVL and VW will only be acted upon on the rising edge of VSO. The bits Y4 to Y0, TST, FA, MBL, F1 and F0 are copied into the FIBI message. The FMC responds to the other bits as follows:

bit	FMC response
TVL	set to "1" for 625-lines per frame set to "0" for 525-lines per frame
VW	vertical sync acceptance window limits are set as follows: VW = "0", TVL = "0" window is from video line 25 to 289; VW = "0", TVL = "1" window is from video line 25 to 342; VW = "1", TVL = "0" window is from video line 240 to 289; VW = "1", TVL = "1" window is from video line 281 to 342.
B2 to B0	set the programmable input delay (PID). B2 is the msb. The delay can be incremented to make the rising edge of PBK earlier in 7 steps of 6 LL2 cycles.
H2 to H0	set the programmable output delay (POD). H2 is the msb. The delay can be incremented to make the falling edge of DHS later in 7 steps of 6 LL2 cycles. DHS and DBK remain in a fixed relationship to each other (all edges move with the POD).
INT	selects mode of display of memory picture: INT = "1" = interlaced; INT = "0" = non-interlaced.
S3 to S0	status control bits. Used as follows: S3 S2 S1 S0 0 0 0 0 direct video — no memory processing 0 0 0 1 store picture in memory and display direct video 0 0 1 0 recall picture from store and view, or re-store the displayed memory picture 0 0 1 1 freeze picture by storing and displaying 0 1 0 0 cross-colour reduction (PAL mode) 0 1 0 1 cross-colour reduction (NTSC mode) 0 1 1 0 noise reduction (low level) 0 1 1 1 noise reduction (high level) 1 0 0 0 background memory active No other codes are permitted.
FTST	test bit, normally set to "0". When set to "1" causes the FIBI output to float.

FUNCTIONAL DESCRIPTION (continued)

I²C read mode

If the correct FMC address is received and the R/$\overline{W}$ bit is set to "1" then the following status byte is returned:

msb							lsb
PUD	BUSY	CM3	CM2	CM1	CM0	M25L	V25L

The bits of the status byte have the following meanings:

bit	meaning
PUD	power-up detection. This bit is set to "1" when a power-up has been detected since this register was last read. The bit is reset to "0" when the register is read
BUSY	"1" indicates that the FMC is busy with a change of status
CM3 to CM0	presents the contents of the current-mode latch and are normally the same as bits S3 to S0, exceptions are after power-on and in background memory mode when the contents are equal to 1 0 0 1
M25L	goes to "1" when the memory line counter is in 'position 0' through to 'position 24'
V25L	goes to "1" when the video line counter is in 'position 0' through to 'position 24'

FIBI (Fig. 3)

The FIBI signal indicates the positions of samples in the video data streams and carries commands to the PEP. Data is transmitted in the normally-HIGH time of FIBI whenever the video counter is reset or, in certain modes, when the last valid memory line is reached. Each transmission is repeated for two lines and each data bit of the message is followed by its inverse. Data sent is acted upon at the next rising edge of FIBI.

FIBI data	description
start bit	"0" sent at the beginning of each message
FA	copied from I²C bit FA
MBL	copied from I²C bit MBL
F1, F0	copied from I²C bits F1, F0
M3 to M0	mode control bits. Normally a copy of the I²C bits S3 to S0. Modified so that direct video is passed through during mode changes and in those cases where the requested mode is not possible
Y4 to Y0	copied from I²C bits Y4 to Y0
TST	copied from I²C bit TST, set internally to "0" at power-on

Data is inserted into the HIGH-period of FIBI 24 LL2 cycles after the rising edge. Each data bit (or its complement) is sent for a period of 6 LL2 cycles. For the description of the timing relative to other outputs see 'signal timing'.

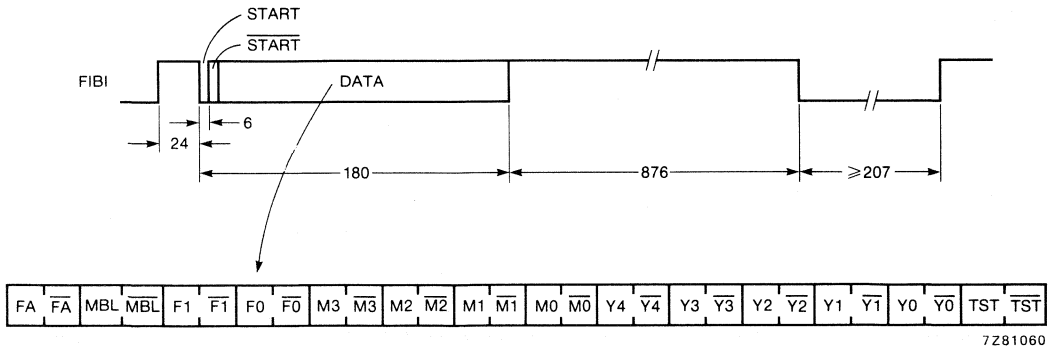


Fig. 3 FIBI timing and order of data (all numbers indicate LL2 cycles).

Signal timing

VSI

This is accepted only during the specified vertical acceptance window if it has an integrated HIGH time $\geqslant 16\ \mu s$ (342 LL2 cycles). When accepted, the VSI pulse resets the video line counter to video line 1. After acceptance at least 324 LL2 clock cycles must elapse before another VSI pulse can be accepted. If a VSI pulse is not accepted an internal vertical synchronizing pulse will be generated at the end of the vertical window.

VSO

In modes where VSO is derived from the incoming video (VSI) the rising edge of VSO follows 344 LL2 cycles after the rising edge of VSI. When VSO is derived from the internal memory counters the timing of VSO depends on the line system in use and the internal bit INT.

line system	line number in which VSO rising edge occurs	number of LL2 cycles from rising edge of FIBI to start of VSO rise
625 non-interlace	313	292
	312	292
625 interlace	312	940
	313	292
525 non-interlace	263	292
	262	292
525 interlace	262	940
	263	292

In all cases VSO will remain HIGH until at least 172 (163) LL2 cycles after the 14th FIBI (non-data) falling edge to occur in the current VSO = HIGH time as shown in Fig. 7.

MRN, MDV

These signals switch during the LOW time of MG, remain valid for at least 4 LL2 cycles after the MG falling edge and are valid at least one LL2 cycle before MG rising edge.

Signal timing (continued)

LFRE, MAV

When these signals are active they will start to change no sooner than 172 (163) LL2 cycles after the first FIBI falling edge in the VSO = HIGH time (see Fig. 7).

BLNO, DBK, DHS, FIBI, LRSTN, PBK

The relationships between these signals are shown in Fig. 4 in which all horizontal timings are shown in relation to one line of active video.

MG

This signal has four modes of operation; normal, refresh, slow and fast gating. The timing in normal and refresh modes is shown in Fig. 4. In the slow gating mode, MG may remain LOW for as many as 16 line periods and then be active for at least 3 line periods. In the fast gating mode the edges of this signal are not synchronized with the other line-rate signals, MG then has a nominal LOW time of 40 LL2 cycles and a nominal HIGH time of 362 LL2 cycles (either time may be extended once by 3 LL2 cycles during the FIBI LOW time in 525-line mode).

BLNI

A rising edge of this signal resets the horizontal timing of the FMC, which results in a falling edge of FIBI 1026 LL2 cycles later. When BLNI is held LOW or HIGH the horizontal timing will run free with a period of 1296 LL2 cycles (625-line working), or 1287 LL2 cycles (525-line working).

Note

In analogue environments the horizontal synchronization is achieved by phase comparison between the phase-reference and analogue burst keys (PBK and ABK, see Fig. 4)and the result is used to control the frequency of a VCO.

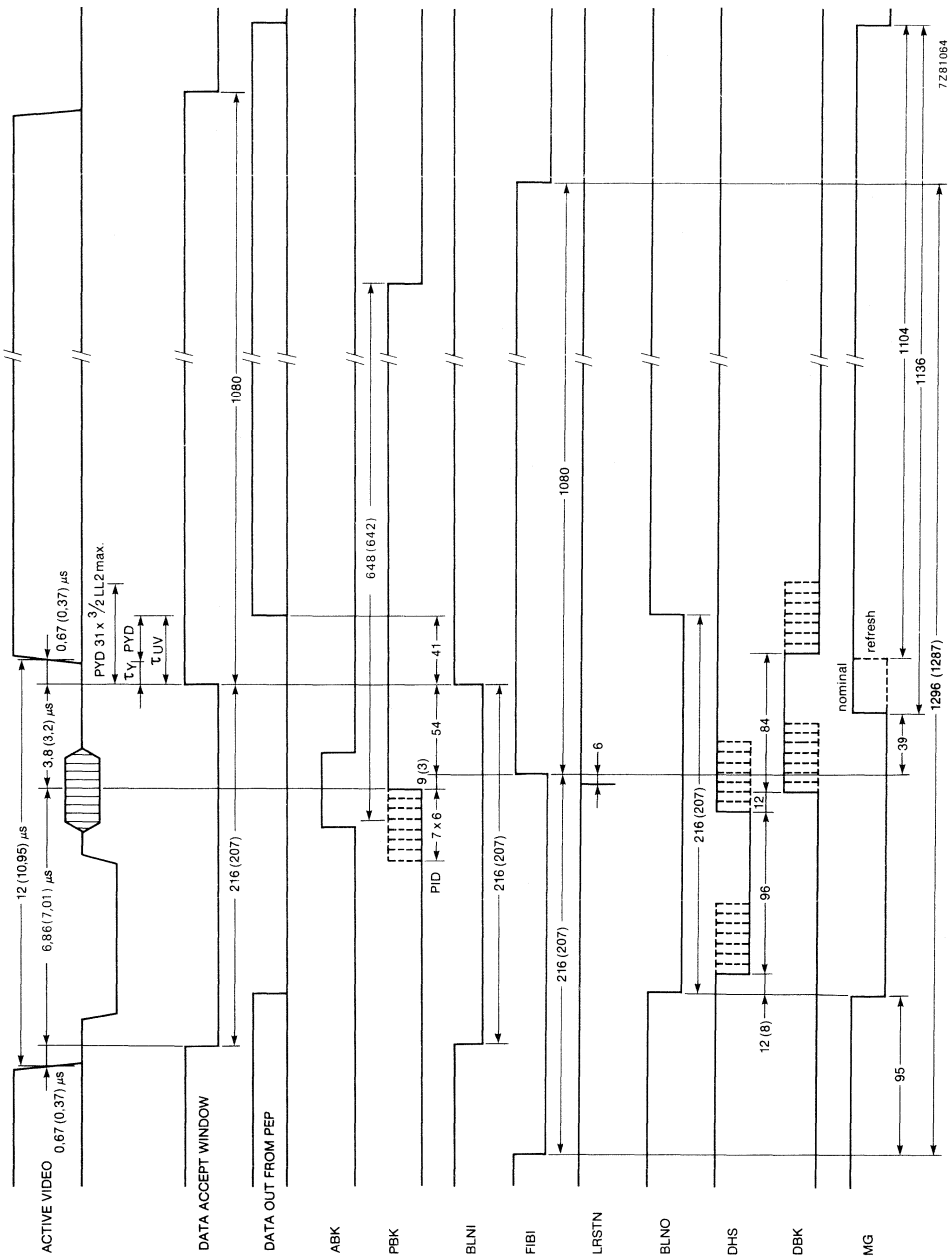


Fig. 4 Horizontal timing signals (all numbers indicate LL2 clock cycles unless otherwise specified, numbers in parentheses are for 525-line systems).

RATINGS

Limiting values in accordance with the Absolute Maximum Rating System (IEC 134)

Supply voltage range	V_{DD}	−0,5 to 6,5	V
D.C. input diode current			
at $V_I < V_{SS}$	$-I_{IK}$	20	mA
at $V_I > V_{DD}$	I_{IK}	20	mA
D.C. input voltage range	V_I	−0,5 to V_{DD}+ 0,5	V
D.C. output diode current			
at $V_O < V_{SS}$	$-I_{OK}$	20	mA
at $V_O > V_{DD}$	I_{OK}	20	mA
D.C. output voltage range	V_O	−0,5 to V_{DD}+ 0,5	V
D.C. output source or sink current per output pin	I_O, $-I_O$	25	mA
D.C. current V_{DD} or V_{SS}	I_{DD}, I_{SS}	50	mA
Storage temperature range	T_{stg}	−65 to 150	°C

HANDLING

Inputs and outputs are protected against electrostatic charge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see 'Handling MOS Devices').

RECOMMENDED OPERATING CONDITIONS

Supply voltage range	V_{DD}	4,5 to 5,5	V
Input voltage range	V_I	−0,5 to V_{DD}+ 0,5	V
Output voltage range	V_O	−0,5 to V_{DD}+ 0,5	V
Operating ambient temperature range	T_{amb}	0 to + 70	°C

CHARACTERISTICS

T_{amb} = 0 to + 70 °C; V_{DD} = 4,5 to 5,5 V; V_{SS} = 0 V; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supplies					
Supply voltage range	V_{DD}	4,5	5,0	5,5	V
Supply current	I_{DD}	*	7,0	*	mA
Inputs (except SDA, SCL)					
Input voltage HIGH	V_{IH}	2,0	–	V_{DD}+ 0,5	V
Input voltage LOW	V_{IL}	0,0	–	0,8	V
Input capacitance:					
LL2 (pin 20)	C_I	–	–	15	pF
all other inputs	C_I	–	–	5	pF
Inputs SDA, SCL					
Input voltage HIGH	V_{IH}	3,0	–	V_{DD}+ 0,5	V
Input voltage LOW	V_{IL}	0,0	–	1,5	V
Input capacitance	C_I	–	–	5	pF
Outputs (except SDA)					
Output voltage HIGH at $-I_O$ = 2,0 mA	V_{OH}	2,2	–	V_{DD}+ 0,5	V
Output voltage LOW at I_O = 2,0 mA	V_{OL}	0,0	–	0,6	V
Output SDA					
Output voltage LOW at I_O = 3,0 mA	V_{OL}	0,0	–	0,4	V
Clock LL2 timing (Fig. 5)					
Cycle time	t_C	47	–	52	ns
HIGH time	t_{CH}	20	–	–	ns
LOW time	t_{CL}	20	–	–	ns
Rise/fall time	t_r, t_f	–	–	3,0	ns
Input BLNI timing (Fig. 5)					
Input set-up time	t_{SU}	12	–	–	ns
Input hold time	t_{HD}	3,0	–	–	ns

* Values under investigation.

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Outputs BLNO, DBK, DHS, FIBI, LRSTN, MG, PBK timing (Fig. 5)					
Output hold time	t_{OH}	3,0	–	–	ns
Output delay time	t_{OD}	–	–	33	ns
Load capacitance	C_L	15	–	25	pF
Output MRN timing (Fig. 6)					
Output hold time	t_{OH}	0,0	–	–	ns
Output delay time	t_{OD}	–	–	600	ns
Load capacitance	C_L	10	–	100	pF
Outputs VSO, LFRE, MAV, MDV (Figs 6 and 7)					
Output hold time	t_{OH}	0,0	–	–	ns
Output delay time	t_{OD}	–	–	300	ns
Load capacitance	C_L	15	–	50	pF
I^2C bus timing (Fig. 8)					
SCL frequency	f_{SCL}	0	–	100	kHz
SCL LOW time	t_{LOW}	4,7	–	–	μs
SCL HIGH time	t_{HIGH}	4,0	–	–	μs
SCL and SDA rise times	t_R	–	–	1	μs
SCL and SDA fall times	t_F	–	–	300	ns
Time the bus must be free before a new transmission can start	t_{BUF}	4,7	–	–	μs
Start condition hold time (after this period the first clock pulse may be generated)	$t_{HD;STA}$	4,0	–	–	μs
Start condition set-up time (repeated start condition only)	$t_{SU;STA}$	4,7	–	–	μs
Data hold time	$t_{HD;DAT}$	0,0	–	–	μs
Data set-up time	$t_{SU;DAT}$	250	–	–	ns
Stop condition set-up time	$t_{SU;STO}$	4,7	–	–	μs

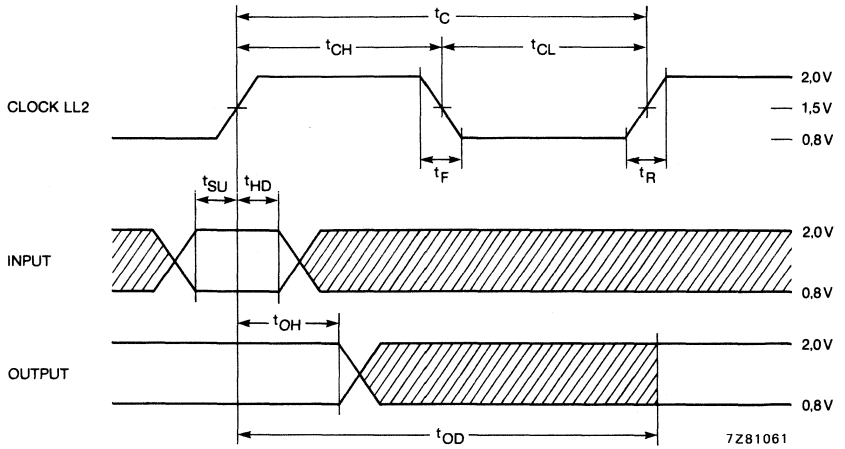


Fig. 5 Clock LL2 timing.

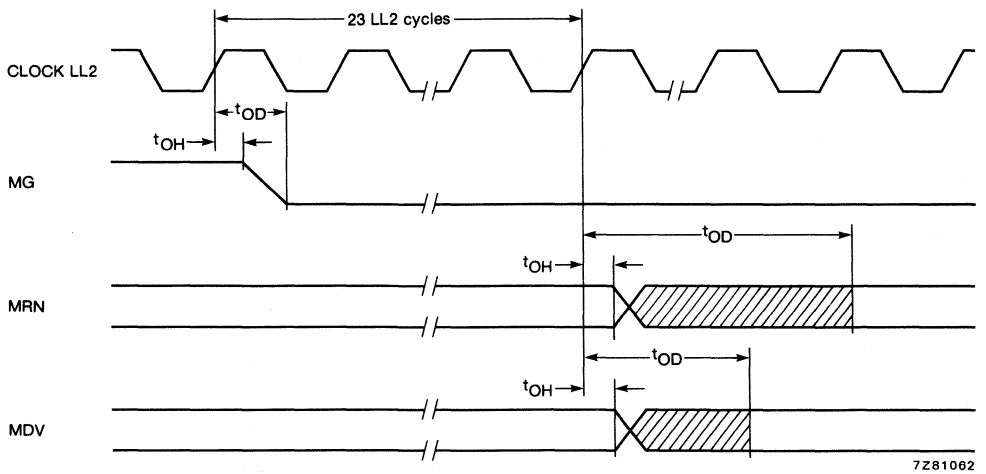


Fig. 6 MG, MRN, and MDV timing.

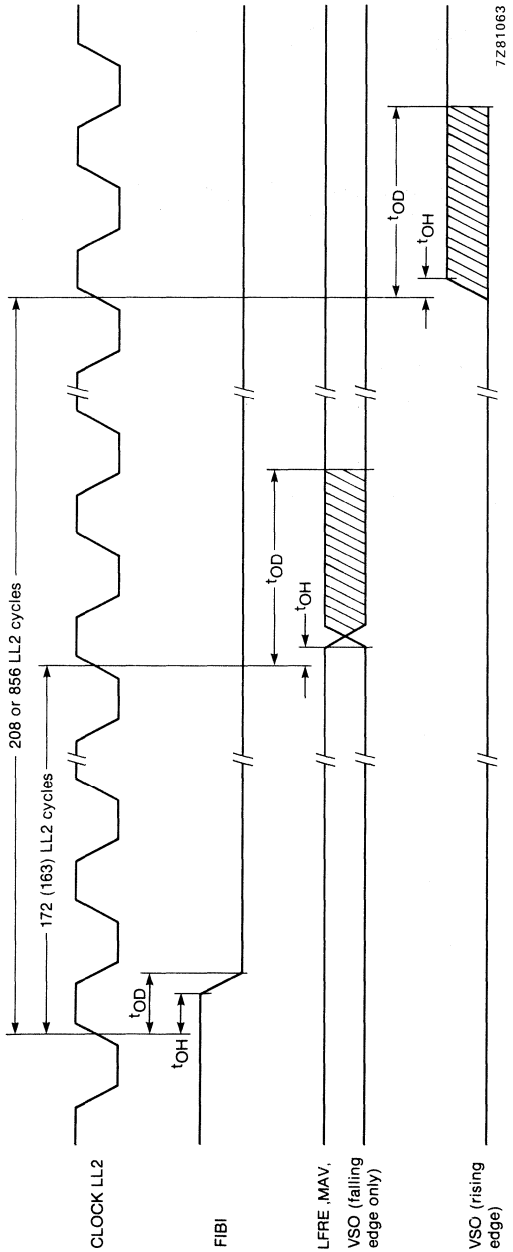


Fig. 7 FIBI, LFRE, MAV, VSO timing (numbers in parentheses are for 525-line working).

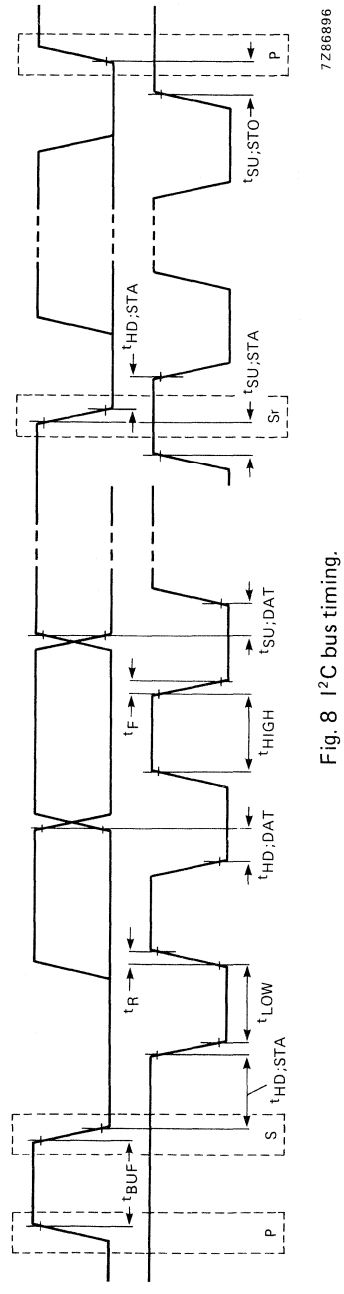


Fig. 8 I^2C bus timing.

DIGITAL MULTISTANDARD TV DECODER

GENERAL DESCRIPTION

The SAA9050 digital multistandard decoder (DMSD) performs demodulation and decoding of all quadrature modulated colour tv standards, and contains luminance and part-synchronization processing for all tv standards.

Features

- Luminance signal processing for all tv standards (PAL, NTSC, SECAM, B/W)
- Horizontal and vertical sync detection for all standards (525/625 lines)
- Chrominance signal processing for all quadrature amplitude modulated colour-carrier signals (PAL-B, G, H, I, M, N; NTSC-M)
- Requires only one crystal (24,576 MHz), which may also be used for audio processing
- Functions, settings and adjustments programmable under software control via the I^2C bus
- User-programmable aperture correction (horizontal peaking)
- Compatible with memory-based features (line-locked clock)
- Multiplexed output format selectable (U, V, Y, Y, Y, Y)
- Parallel (nibble) output format selectable (Y/U6, U5, V6, V5; U4, U3, V4, V3; U2, U1, V2, V1; U0, CS, V0, X)
- SECAM interface
- Cross-colour reduction by chrominance comb-filtering (NTSC)
- Comb-filters adapt automatically to line frequency
- Internal overflow protection
- Selectable chrominance amplitude control protection for non-standard signals
- Programmable horizontal position of the active video signal in each line
- Indirect I^2C control capability to select input from one of four video sources
- Indirect I^2C control capability for automatic flesh-tone correction
- Wide range hue control
- Internal coincidence detection

PACKAGE OUTLINE

40-lead DIL; plastic with internal heat spreader (SOT-129).

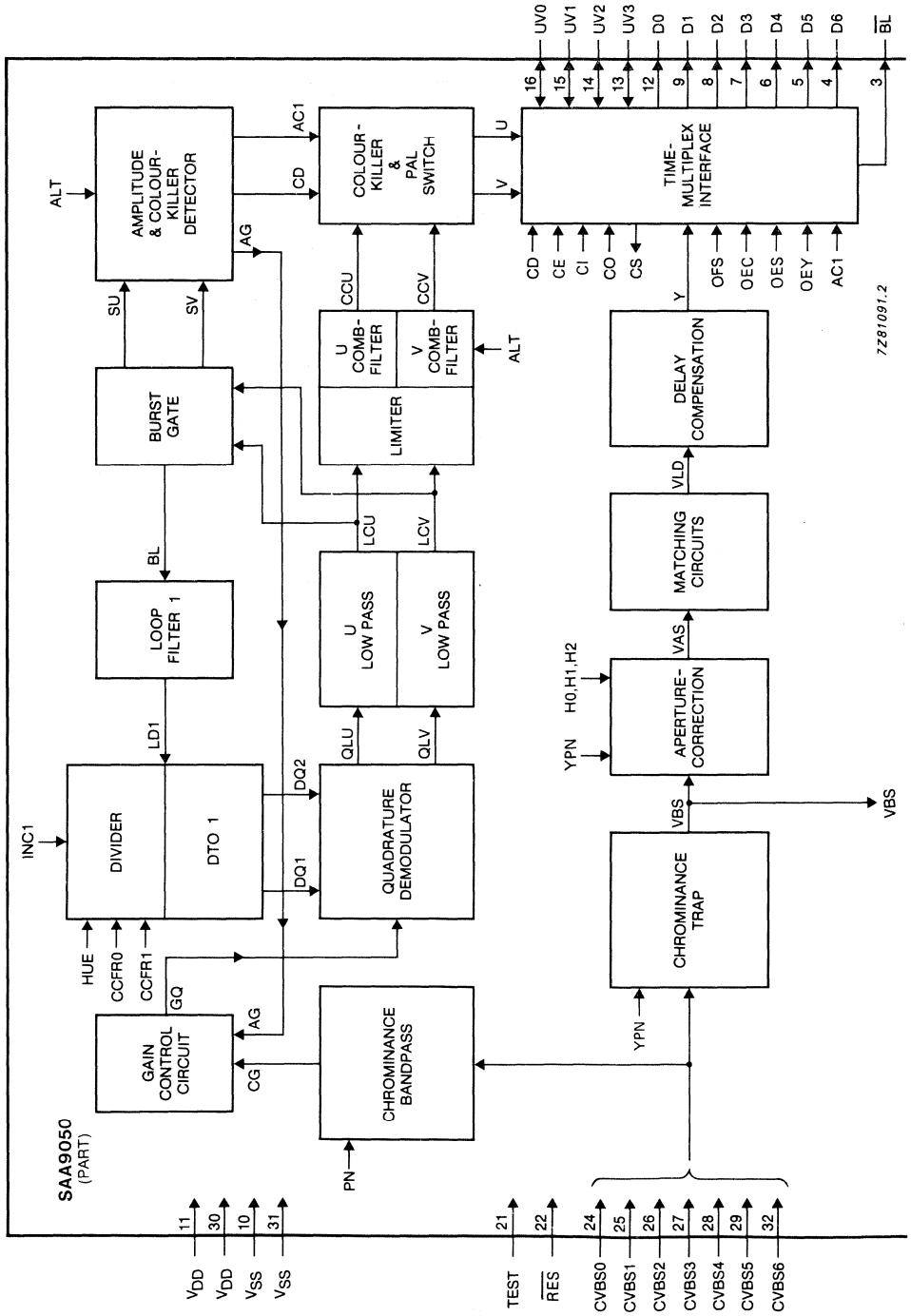


Fig. 1a Block diagram; continued in Fig. 1b.

DEVELOPMENT DATA

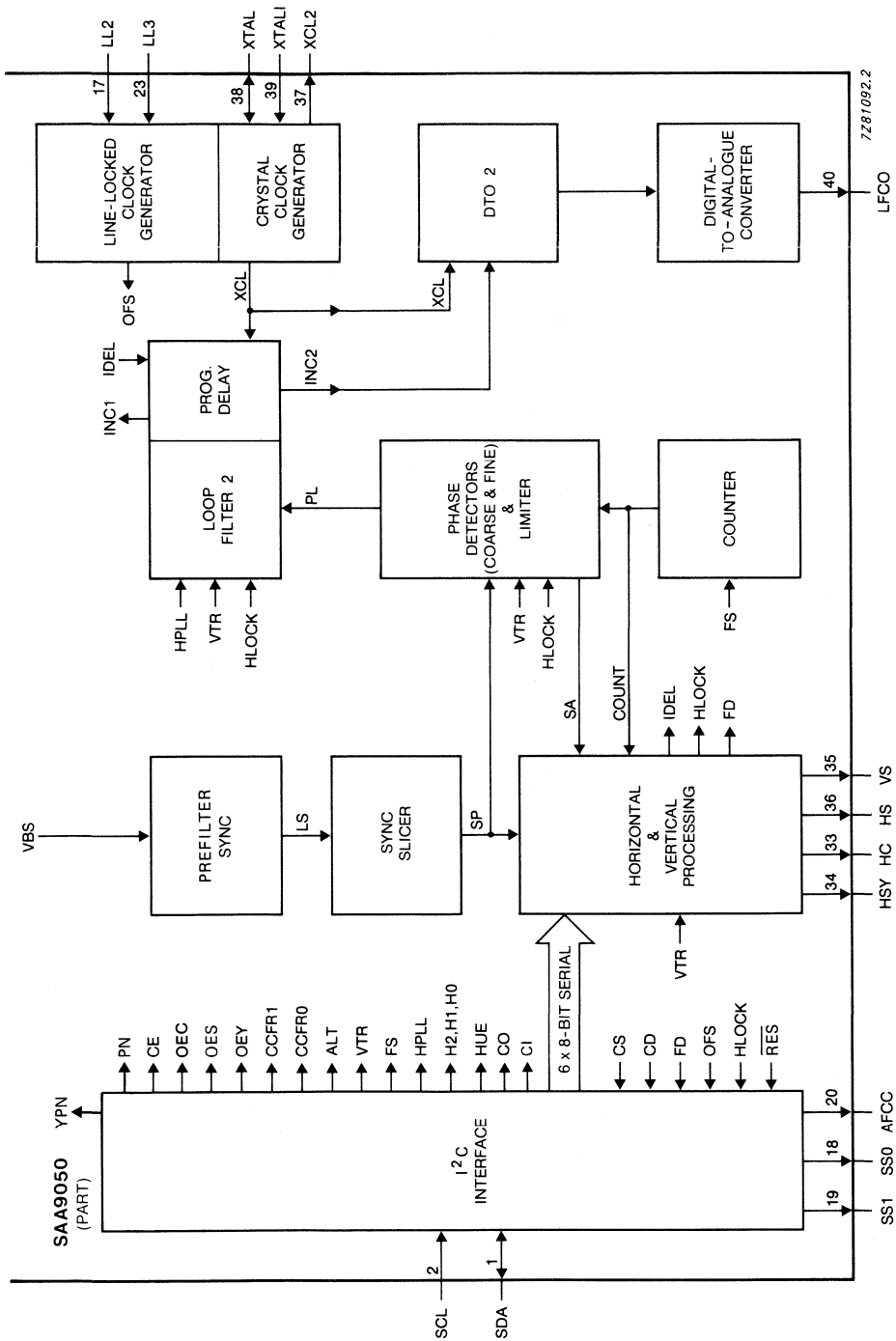


Fig. 1b Block diagram; from Fig. 1a.

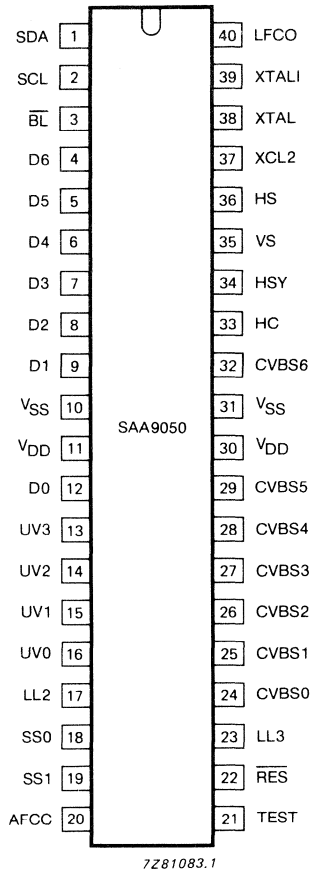


Fig. 2 Pinning diagram.

1	SDA	I^2C bus serial data input/output
2	SCL	I^2C bus serial clock input
3	$\overline{BL}$	Blanking output to indicate the active video and line blanking periods. Active LOW
4	D6(MSB)	Colour difference outputs (U, V) with positive polarity plus luminance (Y)
5	D5	outputs, transmitted in a 20,25 MHz data stream with U, V, Y, Y, Y, Y serial
6	D4	format. The chrominance data is two's complement and luminance is unipolar.
7	D3	The transmission is synchronized externally by $\overline{BL}$. The delay from CVBS
8	D2	input to D0-D6 output is 55 LL3 + 2 LL2 clocks in multiplexed format, and
9	D1	58 LL3 clocks in semi-parallel format. Luminance only is transmitted when
12	D0(LSB)	LL2 = LL3 = 13,5 MHz
10; 31	V_{SS}	Ground (0 V)
11; 30	V_{DD}	Positive supply voltage (+ 5 V)

DEVELOPMENT DATA

13 14 15 16	UV3 UV2 UV1 UV0	SECAM colour difference signal input/PAL or NTSC colour difference signal output. In the input mode, SECAM U, V and CS (colour-SECAM) signals are received from the SECAM decoder. The output mode occurs when LL2 = LL3, then U and V signals are transmitted at 13,5 MHz. Input and output data formats are two's complement with positive polarity
17	LL2	20,25 MHz line-locked clock input used for multiplexed UVY format. LL2 frequency is 13,5 MHz for semi-parallel format
18 19	SS0 SS1	Source select output signals, set via the I^2C bus to control the input switch (e.g. TDA9045)
20	AFCC	Automatic flesh-tone correction control activated via the I^2C bus to control the colour track circuit of NTSC systems
21	TEST	Test input, when HIGH enables the scan-test mode
22	$\overline{RES}$	Reset input, active LOW, causes control registers 1 and 2 to be reset during the reset phase. The minimum LOW period of $\overline{RES}$ is 120 LL3 clocks
23	LL3	13,5 MHz line-locked system clock
24 25 26 27 28 29 32	CVBS0(LSB) CVBS1 CVBS2 CVBS3 CVBS4 CVBS5 CVBS6(MSB)	Digitized composite video, blanking and synchronization signal containing luminance, chrominance and all synchronization information. Two's complement format
33	HC	Horizontal clamping signal that indicates the black-level position before analogue-to-digital conversion. The start and stop time is programmable via the I^2C bus in the range of −9,4 to + 9,5 μs in steps of 74 ns
34	HSY	Horizontal synchronization signal that indicates the sync pulse position before analogue-to-digital conversion. The start and stop time is programmable via the I^2C bus in the range of −14,2 to + 4,7 μs in steps of 74 ns
35	VS	Vertical synchronization output that indicates the vertical position of the picture for 50 or 60 Hz field frequency
36	HS	Horizontal synchronization pulse output. Duration = 16 LL3 clocks. Synchronizes the horizontal position of the active video signal in each line and is programmable via the I^2C bus in the range of −32 to + 32 μs in steps of 300 ns
37	XCL2	Clock output at half the crystal clock frequency (12,288 MHz). In phase with XTAL (pin 38)
38	XTAL	Crystal input/output. Input to the internal clock generator (from an external oscillator, when used), or output of the inverting amplifier to an external crystal (24,576 MHz)
39	XTALI	Input to the inverting amplifier from the external crystal (24,576 MHz); connected to ground when an external oscillator is used
40	LFCO	Line frequency control. Analogue output representing a multiple of the line frequency (6,75 MHz) with a 4-bit resolution, the phase of which is compared with the system clock by the clock generator circuit (SAA9057)

FUNCTIONAL DESCRIPTION (Fig. 1)

The DMSD performs demodulation and decoding for PAL-B, G, H, I, M, N, NTSC-M tv standards and contains luminance and parts of the synchronization processing for all PAL, NTSC and SECAM tv standards. All of the controllable functions of the DMSD, user controls as well as factory adjustments, are accessed via the two-line, bidirectional I^2C bus, so enhancing the adaptability of the digital tv concept.

Operation is based on a line-locked sampling frequency of 13,5 MHz, making the system fully adaptable to all line frequencies and requiring only one crystal for all tv standards.

Output formats (Fig. 3)

There are two output formats available via the time-multiplex interface that are controlled by the LL2 and LL3 clocks. The interface can also be used to incorporate an optional SECAM decoder.

LL2 = 20,25 MHz LL3 = 13,5 MHz	A multiplexed output data stream in the format U, V, Y, Y, Y, Y is transmitted from D0-D6 at a sample rate of 20,25 MHz, giving full compatibility with memory-based feature tv concepts.
LL2 = LL3 = 13,5 MHz	The Y and U, V signals are transmitted separately, the Y signals in a data stream of 13,5 MHz from D0-D6 and the U, V signals in a nibble format from UV0-UV3. The SECAM-decoder option also uses this clock mode.

Processing

The digital CVBS input is separated into its luminance (VBS) and chrominance (CG) parts by chrominance trap and chrominance bandpass circuits, which can be switched by the standard identification signals (PN/YPN) according to the detected PN centre frequency (3,58 or 4,43 MHz). The range of binary values for input/output signals are shown in Fig. 4.

The separated luminance signal (VBS) is passed to an aperture-correction circuit that has programmable horizontal peaking. The corrected signal (VAS) is then matched to the full-scale of the appropriate word-width and limited to prevent overflow. The signal (now VLD) undergoes delay compensation to equalize the delays of the luminance and chrominance channels. Differences of delay compensation requirements in PAL and NTSC modes are catered for when switching is performed by the standard identification signal (PN).

In the chrominance channel, the amplitude of the chrominance signal (CG) is controlled to give a signal with constant burst amplitude (CQ). The control signal (AG) for gain-control is derived in the amplitude and colour-killer detection circuit. If there is a non-standard ratio between burst and chrominance amplitudes (−17% in the NTSC mode), an automatic colour-levelling circuit takes the function of amplitude detection to ensure correct chrominance amplitude and to avoid overflow and limiter defects.

Demodulation of the square-modulated chrominance signal (CQ) is performed by the quadrature demodulator which gives the baseband colour difference signals (LCU and LCV). The comb-filter stage then separates remaining luminance components from these signals and (for PAL) corrects their phase to give the signals CCU and CCV. The number of delay elements required in the comb-filter is minimized by the use of a reduced, blanked, line-locked clock. The comb-filter structure is changeable under the control of the standard-identification signal (ALT).
The colour-killer, under the control of amplitude and colour-killer detection (AC1 and CD), removes incoming signals that do not comply with the chosen standard. The PAL switch restores the correct phasing of the V signal when in PAL mode.

Regeneration of the colour carrier frequency is done by the phase-locked-loop comprising quadrature modulator, low pass filter, burst gate, loop filter 1 and discrete time oscillator (DTO 1). The latter is controlled by standard identification signals (CCFR0, CCFR1) and a signal (HUE) that influences the demodulation phase of the chrominance signal.

In the synchronization circuit, prefilter synchronization is implemented to normalize sync slopes. A sync-slicer provides the detected sync pulses (SP) to the H, V processing and phase detector stages.

The H and V processing comprises part of a PLL circuit for the regeneration of the horizontal synchronization (HS) and an adaptive filter for the detection of vertical sync (VS), see Fig. 5. The H, V processing also generates the coincidence signal (HLOCK) which controls the mute function, and a standard identification signal (FD) which identifies nominal 625 or 525 lines per picture.

The phase detectors that receive the SP signal, also part of the PLL, control the generation of the line-locked clock (PL). Loop filter 2, which has a changeable bandwidth controlled by the video recorder/tv time constant signal (VTR), generates two increment signals (INC1 and INC2) with different delays. INC2 is programmable via the increment-delay signal (IDEL). INC1 corrects the regenerated subcarrier frequency at DTO 1 and INC2 performs phase incrementing of DTO 2. The crystal clock generator provides a stable 24,576 MHz clock input to DTO 2 which in turn supplies the 4-bit DAC with a digital control signal of 432 or 429-times the line frequency. The analogue output (LFCO) from the DAC goes to the clock generator (SAA9057).

The output signals D0-D6 can be multiplexed under the control of an internal blanking and format signal. It is a time-multiplex interface that also provides an external blanking and format signal ($\overline{BL}$).

For real-time inputs to the DMSD, the line-locked clocks LL2 and LL3 are required as well as the digital CVBS signal (CVBS0-CVBS6). As an option, a nibble-format colour difference input to UV0-UV3 can be used for interfacing a digital SECAM decoder. Under the control of the I^2C bus this interface can be switched into an output mode for outward transmission of colour difference signals U, V (LL2 = LL3 = 13,5 MHz).

DEVELOPMENT DATA

PAL-B, G, H, I and NTSC detection

The current version of the DSMD is unable to distinguish between the PAL-B, G, H, I and NTSC 4,4 standards, if the NTSC 4,4 standard is chosen. To overcome this problem in automatic standard routine it is necessary to:

- check the NTSC 4,4 standard before the PAL-B, G, H and I standards

or

- cross check the PAL-B, G, H and I, if the NTSC 4,4 standard is detected.

FUNCTIONAL DESCRIPTION (continued)

I²C bus interface

The following control signals are received via the I²C bus (SDA and SCL) and the I²C bus interface:

- standard identification signals (CCFR0, CCFR1, ALT, FS, CE, YPN)
- time constant VTR/TV (VTR)
- hue control (HUE)
- delay programming of the horizontal signals (HS, HC, HSY)
- increment-delay (IDEL)
- aperture-correction control (H0, H1, H2)
- fixed clock generation command (HPLL)
- internal colour ON/OFF (CO)
- internal colour forced ON for test purposes (CI)
- sync output enable (OES)
- luminance output enable (OEY)
- chrominance output enable (OEC)
- source select signal (SS0, SS1)
- automatic flesh-tone control (AFCC)

Signals transmitted from the DMSD via the I²C bus are:

- standard identification signals (FD, CS)
- colour-killer status signal (CD)
- coincidence information (HLOCK)
- selected output format indicator (OFS)
- power-on-reset of DMSD (PONRES)

Time-multiplex interface (Fig. 6)

The UV0-UV3 signals from the SECAM decoder are received in a 13,5 MHz data stream in the following format:

input signal	sample 0	1	2	3	0	1	2	3
UV3	U6	U4	U2	U0		repeating		
UV2	U5	U3	U1	CS		repeating		
UV1	V6	V4	V2	V0		repeating		
UV0	V5	V3	V1	X		repeating		

The signal CS is an information bit from the SECAM decoder:

CS = logic 0 indicates colour not detected in SECAM
CS = logic 1 indicates colour detected in SECAM
X = don't care

This bit is latched in the DMSD. The CS bit is transmitted to control circuits via the I²C bus.

Commands that control the outputs of the time-multiplex interface are OES, OEY, OEC, CO and CI which are received via the I^2C bus, and CD which is detected in the DMSD. The start condition of OES, OEY, OEC, CO and CI after initialization is always zero. The outputs are controlled as follows:

OES	OEY	OEC	outputs	output status
0 1	X X	X X	HS and VS	HIGH-impedance OFF-state active
X X	0 1	X X	D0-D6 and $\overline{BL}$	HIGH-impedance OFF-state active
X X	X X	0 1	UV0-UV3	HIGH-impedance OFF-state active

CO	CI	CD	outputs	output status
0	X	X	UV0-UV3 or UV samples of 'multiplexed output format (U, V, Y, Y, Y, Y)'	colour OFF (zero)
1 1	0 0	0 1		colour OFF } controlled colour ON } by CD
1	1	X		colour forced ON

X = don't care.

DEVELOPMENT DATA

FUNCTIONAL DESCRIPTION (continued)

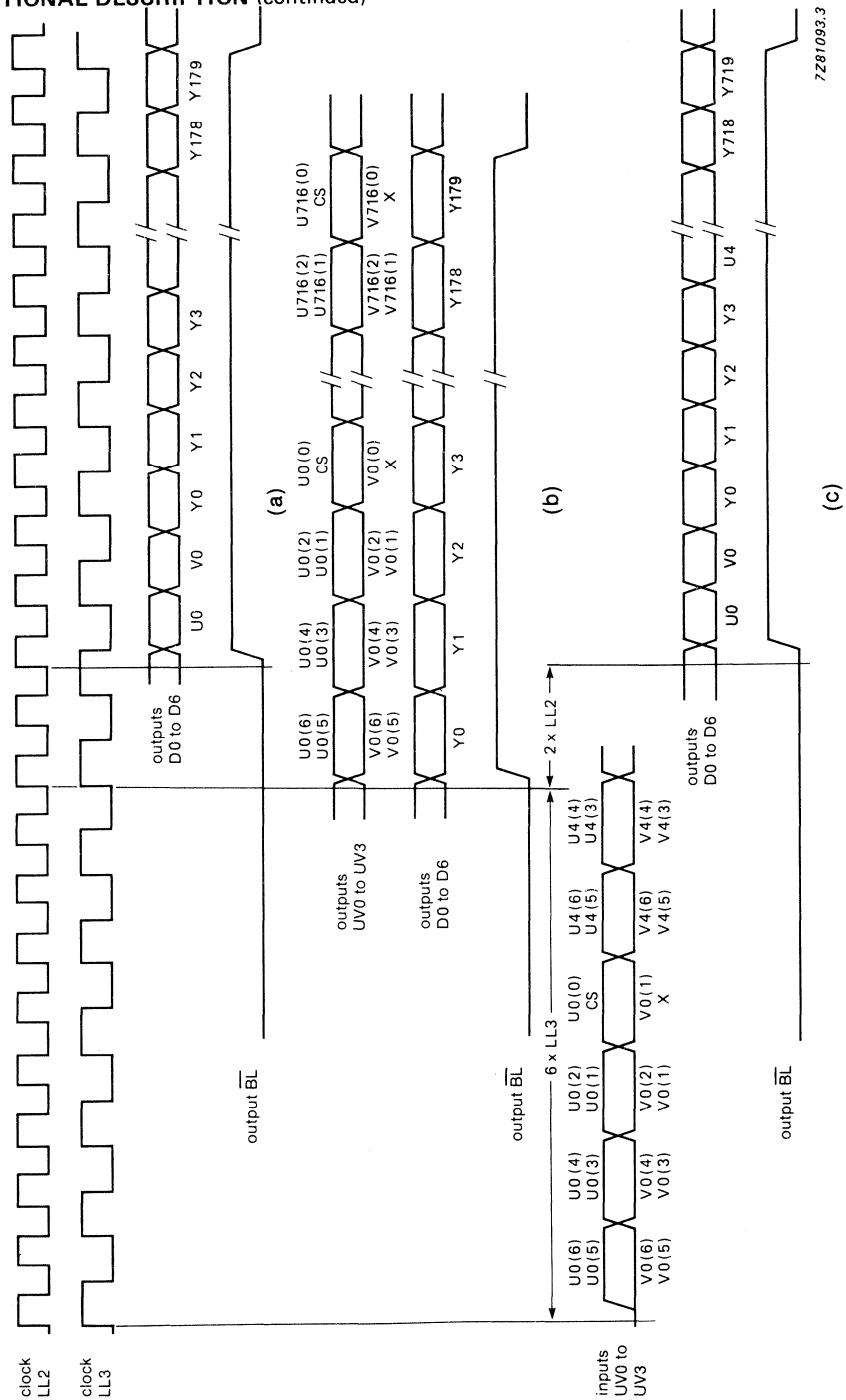
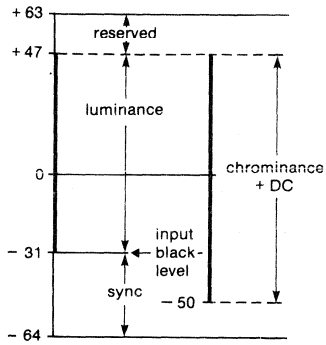
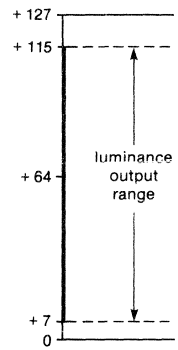


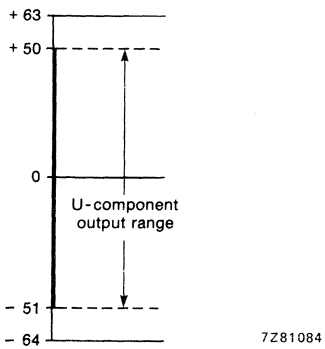
Fig. 3 Correlation of signals: (a) serial mode; (b) parallel (nibble) mode when LL2 = LL3 = 13,5 MHz; (c) serial mode in which SECAM chrominance signals (received via UV0-UV3 from a SECAM decoder) are combined with DMSD luminance signals.



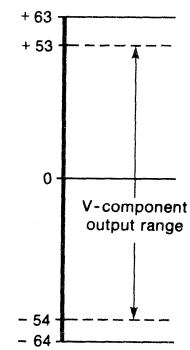
(a) CVBS0 to CVBS6 input range with 75% colour bar.



(b) Y output range.



(c) U output range (B–Y).



(d) V output range (R–Y).

Fig. 4 Diagram showing input/output range of the DMSD (levels are given in binary values).

FUNCTIONAL DESCRIPTION (continued)

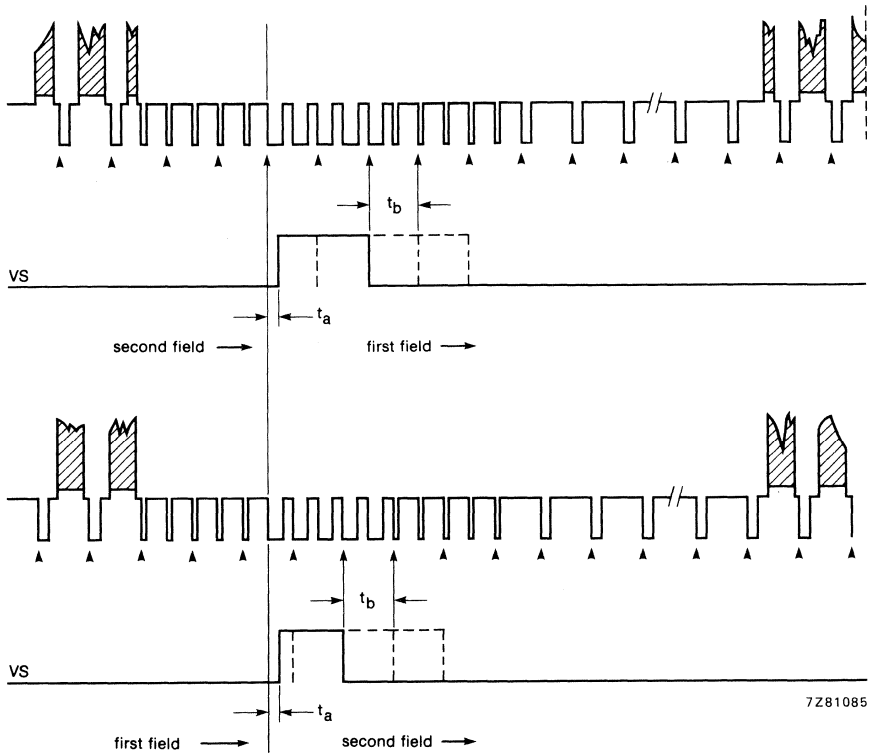
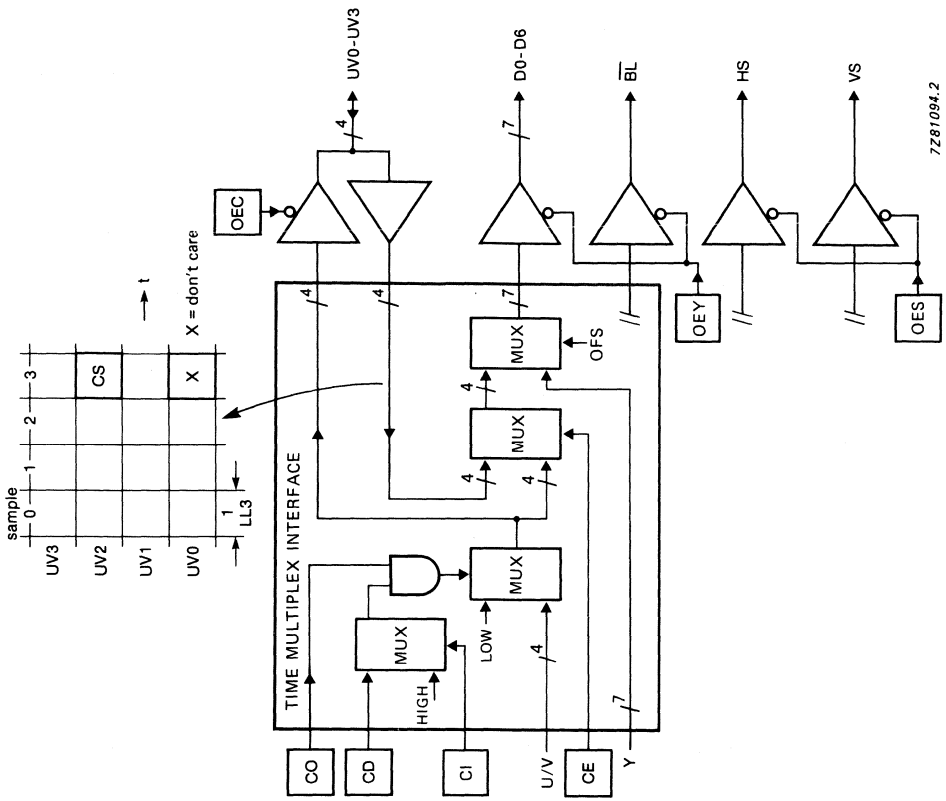


Fig. 5 Vertical sync (VS): time t_a is approximately 24 μs; time t_b = 64 μs (the minimum vertical sync pulse length is 75 μs).

DEVELOPMENT DATA



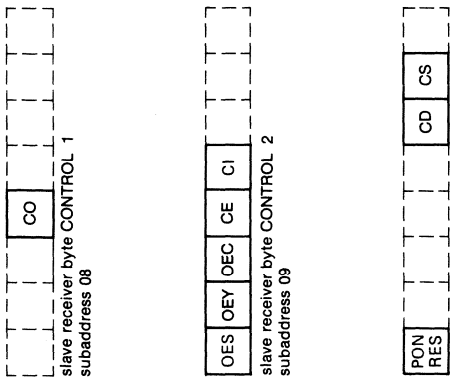


Fig. 6 Schematic diagram of control signals at the time-multiplex interface and output stages.

SLAVE RECEIVER ORGANIZATION

Slave address and receiver format

Slave address for the digital multistandard decoder is:

1	0	0	0	1	0	1

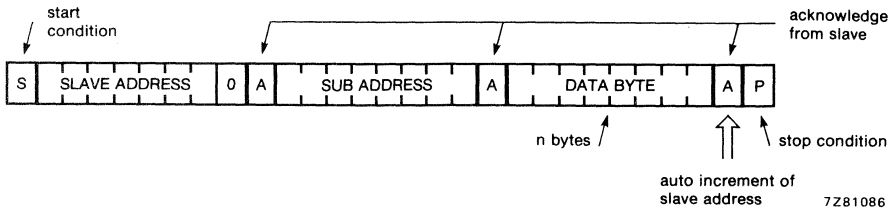


Fig. 7 Slave receiver format.

Subaddress byte and data byte formats

register function	sub address	data byte D7	D6	D5	D4	D3	D2	D1	D0
Increment delay IDEL	00	A07	A06	A05	A04	A03	A02	A01	A00
Horizontal sync									
HSY start time	01	A17	A16	A15	A14	A13	A12	A11	A10
HSY stop time	02	A27	A26	A25	A24	A23	A22	A21	A20
Horizontal clamp									
HC start time	03	A37	A36	A35	A34	A33	A32	A31	A30
HC stop time	04	A47	A46	A45	A44	A43	A42	A41	A40
Horiz. sync after PHI1									
HS start time	05	A57	A56	A55	A54	A53	A52	A51	A50
Horizontal peaking	06	X	X	X	X	X	H2	H1	H0
Hue control	07	A77	A76	A75	A74	A73	A72	A71	A70
Control 1	08	HPLL	FS	VTR	CO	ALT	YPN	CCFR1	CCFR0
Control 2	09	OES	OEY	OEC	CE	CI	AFCC	SS1	SS0
Reserved	0A to 0F	X	X	X	X	X	X	X	X

Notes

The subaddress is automatically incremented. This enables quick initialization by the I^2C bus controller within one transmission.

All eight bits of the subaddress have to be decoded by the device.

The subaddresses shown are acknowledged by the device. Subaddresses 10 to 1F (reserved for the SECAM decoder SAA9055) are not acknowledged. The subaddress counter wraps-around from 1F to 00. Subaddresses 20 to FF are not allowed.

X = don't care.

After power-on-reset the control registers 1 and 2 (subaddresses 08 and 09) are set to logic 0, all other registers are undefined.

The least significant bit of an analogue control or alignment register is defined as AX0.

Increment delay control IDEL (application dependent)

decimal multiplier	delay time (step size = 2/13,5 MHz = 148 ns)	control bits* A07	A06	A05	A04	A03	A02	A01	A00
−1 to −110	−148 ns (min. value)	1	1	1	1	1	1	1	1
	−16,3 μs (outside available range)	1	0	0	1	0	0	1	0
−111 to −214	−16,44 μs	1	0	0	1	0	0	0	1
	−31,7 μs (max. value if FS = logic 1)	0	0	1	0	1	0	1	0
−215	−31,85 μs (outside central counter if FS = logic 1)**	0	0	1	0	1	0	0	1
−216	−32 μs (max. value if FS = logic 0)	0	0	1	0	1	0	0	0
−217	−32,148 μs (outside central counter if FS = logic 0)**	0	0	1	0	0	1	1	1
to −256	−37,9 μs (outside central counter)**	0	0	0	0	0	0	0	0

* A sign bit, designated A08 and internally set to HIGH, indicates values are always negative.

** The horizontal PLL does not function in this condition: the system clock frequency is set to a value fixed by the last update and is within ± 7,1% of the nominal frequency.

Horizontal sync HSY start time (application dependent)

decimal multiplier	delay time (step size = 1/13,5 MHz = 74 ns)	control bits A17	A16	A15	A14	A13	A12	A11	A10
+ 191	−14,2 μs (max. negative value)	1	0	1	1	1	1	1	1
to + 1	−0,074 μs	0	0	0	0	0	0	0	1
0	0 μs reference point	0	0	0	0	0	0	0	0
−1 to −64	+ 0,074 μs	1	1	1	1	1	1	1	1
	+ 4,7 μs (max. positive value)	1	1	0	0	0	0	0	0

DEVELOPMENT DATA

SLAVE RECEIVER ORGANIZATION (continued)

Horizontal sync HSY stop time (application dependent)

decimal multiplier	delay time (step size = 1/13,5 MHz = 74 ns)	control bits A27	A26	A25	A24	A23	A22	A21	A20
+ 191	−14,2 μs (max. negative value)	1	0	1	1	1	1	1	1
to									
+ 1	−0,074 μs	0	0	0	0	0	0	0	1
0	0 μs reference point	0	0	0	0	0	0	0	0
−1	+ 0,074 μs	1	1	1	1	1	1	1	1
to									
−64	+ 4,7 μs (max. positive value)	1	1	0	0	0	0	0	0

Horizontal clamp HC start time (application dependent)

decimal multiplier	delay time (step size = 1/13,5 MHz = 74 ns)	control bits A37	A36	A35	A34	A33	A32	A31	A30
+ 127	−9,4 μs (max. negative value)	0	1	1	1	1	1	1	1
to									
+ 1	−0,074 μs	0	0	0	0	0	0	0	1
0	0 μs reference point	0	0	0	0	0	0	0	0
−1	+ 0,074 μs	1	1	1	1	1	1	1	1
to									
−128	+ 9,5 μs (max. positive value)	1	0	0	0	0	0	0	0

Horizontal clamp HC stop time (application dependent)

decimal multiplier	delay time (step size = 1/13,5 MHz = 74 ns)	control bits A47	A46	A45	A44	A43	A42	A41	A40
+ 127	−9,4 μs (max. negative value)	0	1	1	1	1	1	1	1
to									
+ 1	−0,074 μs	0	0	0	0	0	0	0	1
0	0 μs reference point	0	0	0	0	0	0	0	0
−1	+ 0,074 μs	1	1	1	1	1	1	1	1
to									
−128	+ 9,5 μs (max. positive value)	1	0	0	0	0	0	0	0

Horizontal sync after PHI1 HS start time (application dependent)

50 Hz; 625-line mode and FS = logic 0

decimal multiplier	delay time (step size = 4/13,5 MHz = 296 ns)	control bits A57	A56	A55	A54	A53	A52	A51	A50
+127	forbidden;	0	1	1	1	1	1	1	1
to	outside available								
+109	central counter range	0	1	1	0	1	1	0	1
+108	−32 μs (max. neg. value)	0	1	1	0	1	1	0	0
to									
+1	−0,296 μs	0	0	0	0	0	0	0	1
0	0 μs reference point	0	0	0	0	0	0	0	0
−1	+0,296 μs	1	1	1	1	1	1	1	1
to									
−107	+31,7 μs (max. pos. value)	1	0	0	1	0	1	0	1
−108	forbidden;	1	0	0	1	0	1	0	0
to	outside available								
−128	central counter range	1	0	0	0	0	0	0	0

60 Hz; 525-line mode and FS = logic 1

decimal multiplier	delay time (step size = 4/13,5 MHz = 296 ns)	control bits A57	A56	A55	A54	A53	A52	A51	A50
+127	forbidden;	0	1	1	1	1	1	1	1
to	outside available								
+107	central counter range	0	1	1	0	1	0	1	1
+106	−31,8 μs (max. neg. value)	0	1	1	0	1	1	0	0
to									
+1	−0,294 μs	0	0	0	0	0	0	0	1
0	0 μs reference point	0	0	0	0	0	0	0	0
−1	+0,294 μs	1	1	1	1	1	1	1	1
to									
−107	+31,5 μs (max. pos. value)	1	0	0	1	0	1	0	1
−108	forbidden;	1	0	0	1	0	1	0	0
to	outside available								
−128	central counter range	1	0	0	0	0	0	0	0

DEVELOPMENT DATA

SLAVE RECEIVER ORGANIZATION (continued)

Horizontal peaking H2, H1, H0, PN (user dependent) (see Fig. 13)

aperture factor (af)	control bits H2	H1	H0	YPN
0	0	0	0	0
1	0	0	1	0
2	0	1	0	0
3	0	1	1	0
4	1	0	0	0
5	1	0	1	0
6	1	1	0	0
7	1	1	1	0
0	0	0	0	1
1	0	0	1	1
2	0	1	0	1
3	0	1	1	1
4	1	0	0	1
5	1	0	1	1
6	1	1	0	1
7	1	1	1	1

Chrominance trap select (system mode dependent)

YPN	chrominance trap
0	4,43 MHz
1	3,58 MHz

Hue phase (user dependent)

hue phase	control bits A77	A76	A75	A74	A73	A72	A71	A70
+ 178,6 deg to	1	1	1	1	1	1	1	1
0 deg to	1	0	0	0	0	0	0	0
−180 deg	0	0	0	0	0	0	0	0

Step size per least-significant bit (A70) = 1,4 deg.

Reference point for positive colour difference signals = 0 deg.

The hue phase may be shifted ± 180 deg from the reference point using bit A77, the colour difference signals are then switched from normal positive to negative polarity.

Horizontal clock PLL (application dependent)

function	HPLL control bit
horizontal clock PLL open, horizontal frequency fixed	1
horizontal clock PLL closed	0

Field frequency select (system mode dependent)

function	FS control bit
60 Hz; 525-line mode	1
50 Hz; 625-line mode	0

VTR/TV mode select (system mode dependent)

function	VTR control bit
VTR mode	1
TV mode	0

DEVELOPMENT DATA

SLAVE RECEIVER ORGANIZATION (continued)

Colour-on control (system mode dependent)

function	CO control bit
colour ON	1
colour OFF (all colour output samples zero)	0

Alternate/non-alternate mode (system mode dependent)

function	ALT control bit
alternate mode (PAL)	1
non-alternate mode (NTSC)	0

Colour carrier frequency control (system mode dependent)

colour carrier frequency	control bits CCFR1	CCFR0
4 433 618,75 Hz (PAL-B, G, H, I; NTSC-4,43)	0	0
3 575 611,49 Hz (PAL-M)	0	1
3 582 056,25 Hz (PAL-N)	1	0
3 579 545 Hz (NTSC-M)	1	1

Colour decoding table

colour standard	control bits FS				ALT		CCFR1	CCFR0
PAL-B, G, H, I		0			1		0	0
NTSC-4,43; 50 Hz		0			0		0	0
NTSC-4,43; 60 Hz		1			0		0	0
PAL-M	HPLL	1	VTR	CO	1	YPN	0	1
PAL-N		0			1		1	0
NTSC-M		1			0		1	1

Sync output enable (system mode dependent)

function	control bit OES
outputs HS and VS active	1
outputs HS and VS HIGH-Z	0

Y output enable (system mode dependent)

function	control bit OEY
outputs D0-D6 and $\overline{BL}$ active	1
outputs D0-D6 and $\overline{BL}$ HIGH-Z	0

Chrominance output enable (system mode dependent)

function	control bit OEC
outputs UV0-UV3 active; chrominance signal when CD = logic 1; zero signal when CD = logic 0	1
outputs UV0-UV3 HIGH-Z	0

External colour select (system mode dependent)

function	control bit CE
select external colour channel; serial format via inputs UV0-UV3	1
select internal colour channel	0

Internal colour forced ON/OFF (for test or service requirements only)

function	control bit CI
colour forced ON if CO = logic 1 (CD = X) colour OFF if CO = logic 0 (CD = X)	1
colour OFF if CO = logic 0 (CD = X) colour controlled by CD if CO = logic 1	0

X = don't care

Automatic flesh-tone corrector (colour track) (user dependent)

function	AFCC control bit
colour track ON	1
colour track OFF	0

Source select (system mode dependent)

function	control bits SS1	SS0
select input CVBS0	0	0
select input CVBS1*	0	1
select input CVBS2	1	0
select input CVBS3	1	1

* not allowed when operating with TDA9045.

DEVELOPMENT DATA

SLAVE TRANSMITTER ORGANIZATION

Slave transmitter format

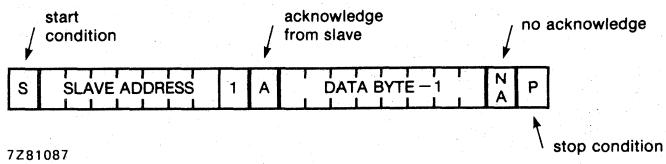


Fig. 8 Slave transmitter format (a general call address is not acknowledged).

The format of data byte 1 is:

PONRES	HLOCK	OFS	FD	0	CD	CS	0

PONRES Status bit for power-on-reset ($\overline{RES}$) and after a power failure:

logic 1 after the first power-on-reset and after a power failure. Also set to logic 1 after a severe voltage dip that may have disturbed slave receiver data in the PAL/NTSC decoder (SAA9050). PONRES sets all data bits of control registers 1 and 2 to zero.

logic 0 after a successful read of the PAL/NTSC decoder status byte.

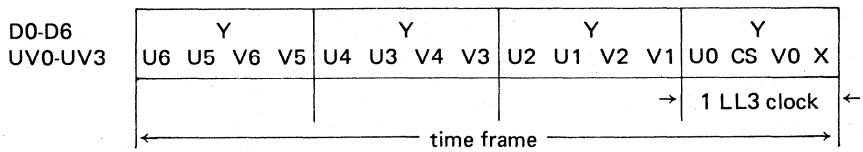
HLOCK Status bit for horizontal frequency lock (transmitter identification, stop or mute bit):

logic 1 if horizontal frequency is not locked (no transmitter available);

logic 0 if horizontal frequency is locked (transmitter received).

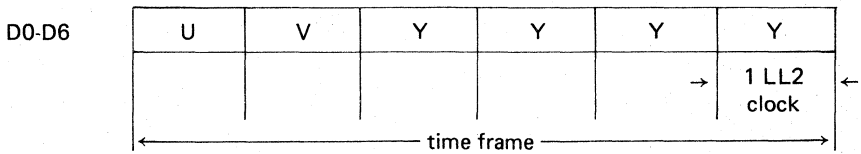
OFS Status bit for output format selection:

logic 1 when quasi-parallel format is selected:



X = don't care

logic 0 when serial output format is selected:



FD — Detected field frequency status bit:
logic 1 when received signal has 60 Hz sync pulses;
logic 0 when received signal has 50 Hz sync pulses.

CD — PAL/NTSC colour-detected status bit:
logic 1 when PAL/NTSC colour signal is detected;
logic 0 when no PAL/NTSC colour signal is detected.

CS — SECAM colour-detected status bit:
logic 1 when SECAM colour signal is detected;
logic 0 when no SECAM colour signal is detected.

PROGRAMMING IDEL, HSY, HC and HS

These variables are programmed via data words on the I²C bus. In the following examples decreasing numbers correspond to increasing time.

IDEL (Fig. 9)

The IDEL data word compensates for the time delays in data processing between loop filter 2 and the quadrature demodulator and includes internal and external (system) signal paths. The internal path from loop filter 2 takes INC1 to the divider and DTO 1. This delay (t_{REF}) corrects the relationship between the subcarrier frequency and the line frequency. The external path accounts for the following time delays:

t_{IDEL}	programmable delay time	in LL3 periods
t_a	processing time of DTO 2 and the D-A converter	
t_b	chrominance bandpass and gain control stage delay times	
t_{CGC}	clock generator circuit delay time	
t_{ADC}	analogue-to-digital converter delay time	
t_{SRC}	sample-rate converter delay time	
t_{SECAM}	SECAM colour decoder delay time	

As the delays t_a and t_b are known constants, t_{IDEL} is programmed as follows:

$$t_{IDEL} = -115 - 0{,}5\,(99 - t_{CGC} - t_{ADC} - t_{SRC}{}^{*} - t_{SECAM}{}^{*})$$

Programming range: −115 to −214/−216.

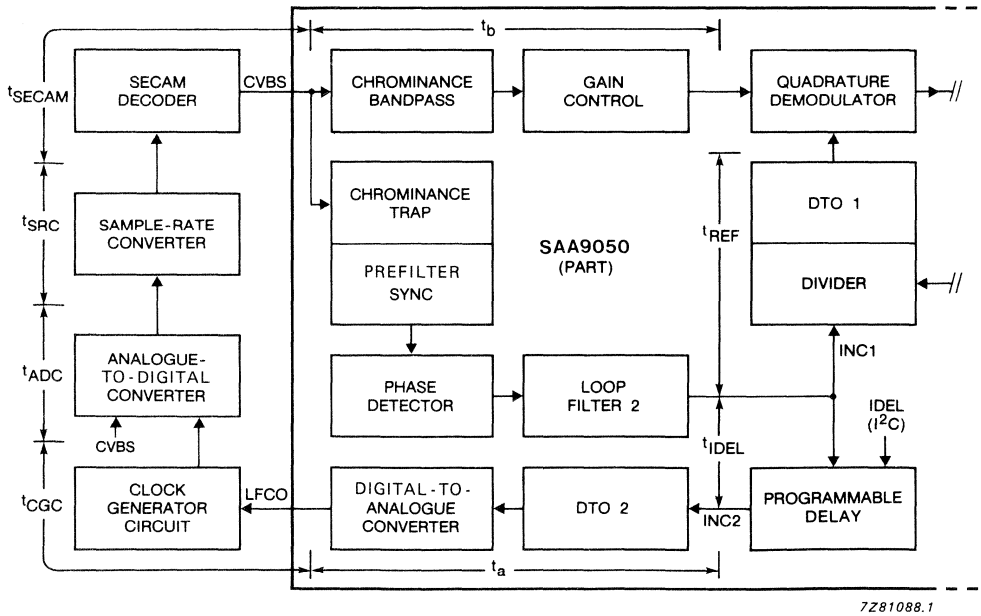


Fig. 9 Compensation of delay times by increment delay control IDEL.

* When included in the application.

PROGRAMMING IDEL, HSY, HC and HS (continued)

HSY (Fig. 10)

Referring to Fig. 10 points (1), (2) and periods a, b:

HSY start time $= T_{(1)-(2)} + 42 - a$ LL3 clock periods

HSY stop time $= T_{(1)-(2)} + 42 - b$ LL3 clock periods

Programming range of HSY start/stop time: + 191 to −64 LL3 clock periods.

HC (Fig. 10)

Referring to Fig. 10 points (1), (2) and periods c, d:

HC start time $= T_{(1)-(2)} + 42 - c$ LL3 clock periods

HC stop time $= T_{(1)-(2)} + 42 - d$ LL3 clock periods

Programming range of HC start/stop time: + 127 to −128 LL3 clock periods.

HS (Fig. 10)

The reference positions of HS in PAL and NTSC modes are shown in Fig. 10 at points (4) and (5) respectively. To move the HS pulse to the centre of blanking pulse $\overline{BL}$ the following equation is used:

$$\text{HS (NTSC)} : \frac{-[\text{position of HS relative to point (3)} + 17\ \text{LL3}]}{4\ \text{LL3}}$$

$$\text{HS (PAL)} : \frac{-[\text{position of HS relative to point (3)} + 14\ \text{LL3}]}{4\ \text{LL3}}$$

In the example given in Fig. 10:

HS (NTSC) : $-[55 + 17]/4 = -18$ (decimal) = 1110 1110 (binary)

HS (PAL) : $-[62 + 14]/4 = -19$ (decimal) = 1110 1101 (binary)

DEVELOPMENT DATA

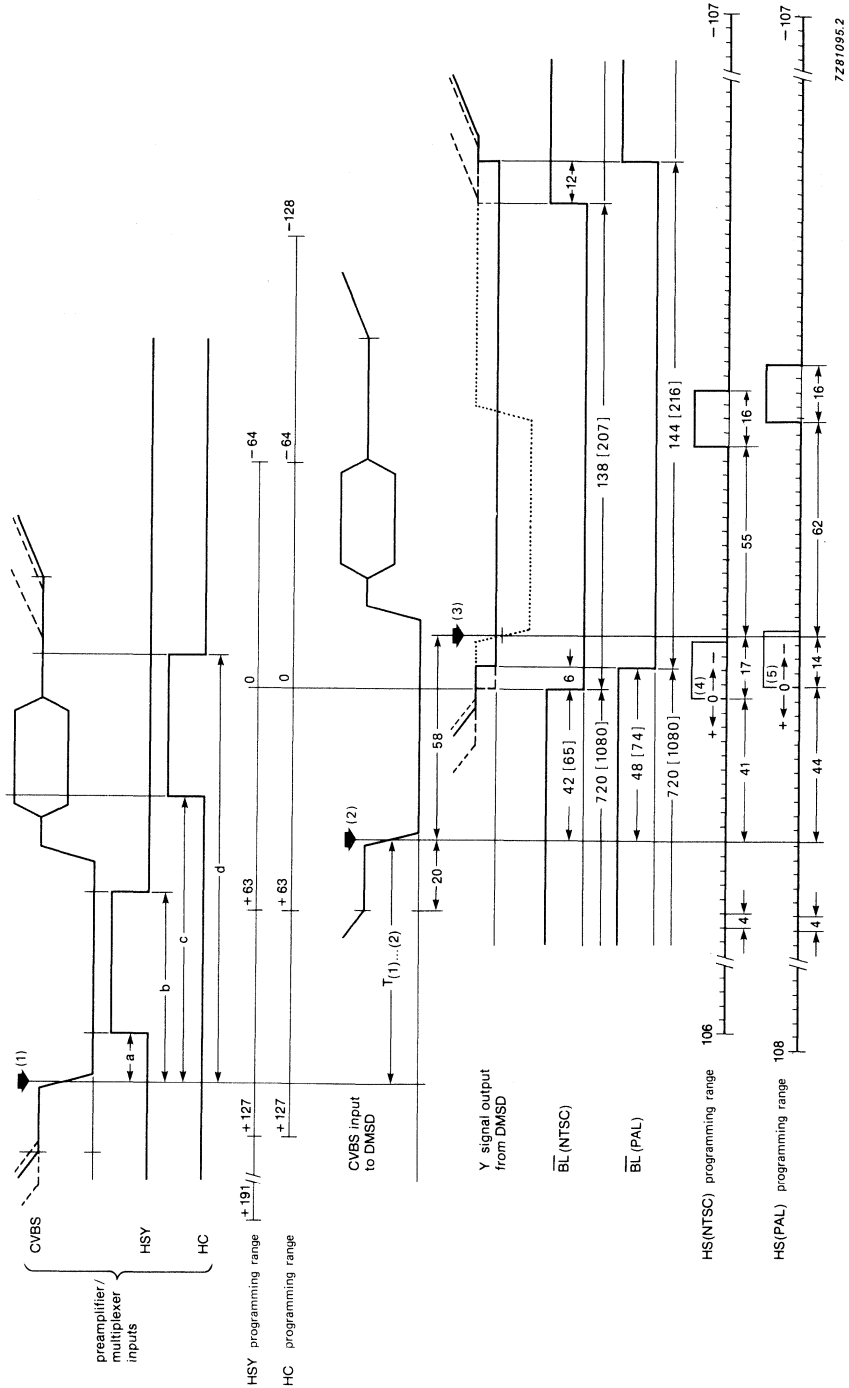


Fig. 10 Signal correlation (see notes on next page).

Notes to Fig. 10

———— represents PAL signals

– – – – – represents NTSC signals (showing tolerance of active video)

HSY and HC inputs are referenced to the analogue input CVBS (1)

$\overline{BL}$ and HS outputs are referenced to the digital input CVBS (2) or to the DMSD output (3).

Waveform timing is indicated in numbers (n) of LL3 cycles (n x $1/f_{LL3}$), where n = 1 for HSY, HC, CVBS input to DMSD and $\overline{BL}$, and n = 4 for HS. In the serial mode the waveform is indicated in numbers of LL2 cycles written in square brackets.

RATINGS

Limiting values in accordance with the Absolute Maximum Rating System (IEC 134)

Supply voltage range	V_{DD}	−0,5 to + 7,0 V
Input voltage range	V_I	−0,5 to + 7,0 V
Output voltage range (max. output current $I_{O\ max}$ = 20 mA)	V_O	−0,5 to + 7,0 V
Maximum power dissipation per package	P_{tot}	* W
Operating ambient temperature range	T_{amb}	0 to + 70 °C
Storage temperature range	T_{stg}	−65 to + 150 °C

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is good practice to take normal precautions appropriate to handling MOS devices (see 'Handling MOS Devices').

CHARACTERISTICS

V_{DD} = 4,5 to 5,5 V; T_{amb} = 0 to + 70 °C; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supplies					
Supply voltage	V_{DD}	4,5	5,0	5,5	V
Supply current	I_{DD}	–	350	*	mA
Inputs					
Input voltage LOW:					
pins 13 to 17, 21 to 29, 32 and 38	V_{IL}	−0,5	–	+ 0,8	V
pins 1 and 2	V_{IL}	−0,5	–	+ 1,5	V
Input voltage HIGH:					
pins 13 to 16, 21, 22, 24 to 29 and 32	V_{IH}	2,0	–	V_{DD}	V
pins 1, 2 and 38	V_{IH}	3	–	V_{DD}	V
pins 17 and 23	V_{IH}	2,4	–	V_{DD}	V
Input leakage current:					
pins 1, 2, 13 to 17, 21 to 29 and 32	I_I	–	–	10	μA
Input capacitance:					
pins 13 to 16	C_I	–	–	5	pF
pin 17	C_I	–	–	15	pF
pin 23	C_I	–	–	30	pF
pin 38	C_I	8	–	–	pF
pins 1, 2, 21, 22, 24 to 29 and 32	C_I	–	–	7,5	pF
Outputs					
Output capacitance pins 4 to 9 and 12	C_O		*		pF
Output voltage LOW:					
pins 3 to 9, 12 to 16, 18 to 20 and 33 to 37 at I_{OL} = 2,0 mA	V_{OL}	0	–	0,6	V
pin 1 at I_{OL} = 5 mA	V_{OL}	0	–	0,45	V

* Value to be fixed

DEVELOPMENT DATA

parameter	symbol	min.	typ.	max.	unit
Outputs (continued)					
Output voltage HIGH: pins 1, 3 to 9, 12 to 16, 18 to 20 and 33 to 37 at I_{OH} = –0,5 mA	V_{OH}	2,2	–	V_{DD}	V
LFCO output (pin 40, AC coupled) 4-bit triangular waveform clocked at 24,576 MHz (peak-to-peak value):					
$R_L \geqslant 10\ k\Omega$; $C_L < 15$ pF	$V_{O(p-p)}$	1	–	–	V
$R_L \geqslant 1\ k\Omega$; $C_L < 15$ pF	$V_{O(p-p)}$	0,5	–	–	V
Timing (Fig. 11)					
LL2 cycle time	t_{C2}	46**	–	53**	ns
LL2 duty factor	t_{C2H}/t_{C2}	45	–	55	%
LL2 rise and fall times▲	t_r, t_f	–	–	6	ns
LL3 cycle time	t_{C3}	69**	–	80**	ns
LL3 duty factor	t_{C3H}/t_{C3}	45	–	55	%
LL3 rise and fall times▲	t_r, t_f	–	–	6	ns
Skew time LL2/LL3	t_{skew}	–2	–	+ 2	ns
Input set-up time	t_{SU}	12	–	–	ns
Input hold time	t_{IH}	3	–	–	ns
Output hold time at C_L = 7,5 to 15 pF	t_{OH}	3	–	–	ns
Output delay time at C_L = 7,5 to 15 pF	t_{OD}	–	–	33	ns
Crystal oscillator (Fig. 12)					
Nominal frequency (third harmonic)	f_n	–	24,576	–	MHz
Permissible deviation from nominal frequency (adjustment tolerance)	$\Delta f/f_n$	–50	–	+ 50	10^{-6}
Temperature deviation	$\Delta f/f_n$	–20	–	+ 20	10^{-6}
Temperature range	T_{XTAL}	0	–	+ 70	°C
Load capacitance	C_L	8	–	–	pF
Resonance resistance	R_r	–	40	–	Ω
Motional inductance	L_1	–	*	–	mH
Motional capacitance	C_1	–	*	–	fF
Parallel capacitance	C_0	–	*	–	pF

* Value to be fixed.

** For min. and max. cycle times $\Delta f = \pm 7{,}1\%$ of typical frequency value.

▲ Difference between t_r and t_f of LL3 must be less than 1 ns; rising and falling edge are assumed to be smooth due to low pass filtering.

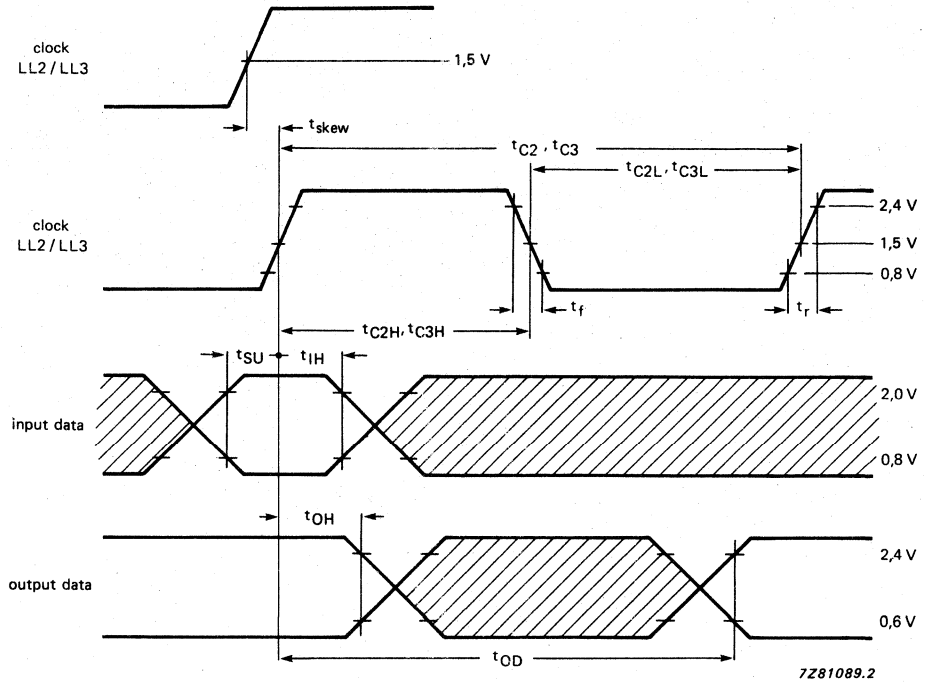


Fig. 11 Timing diagram.

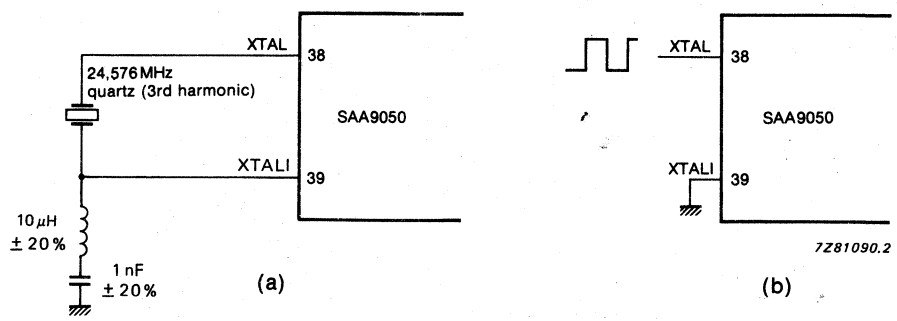
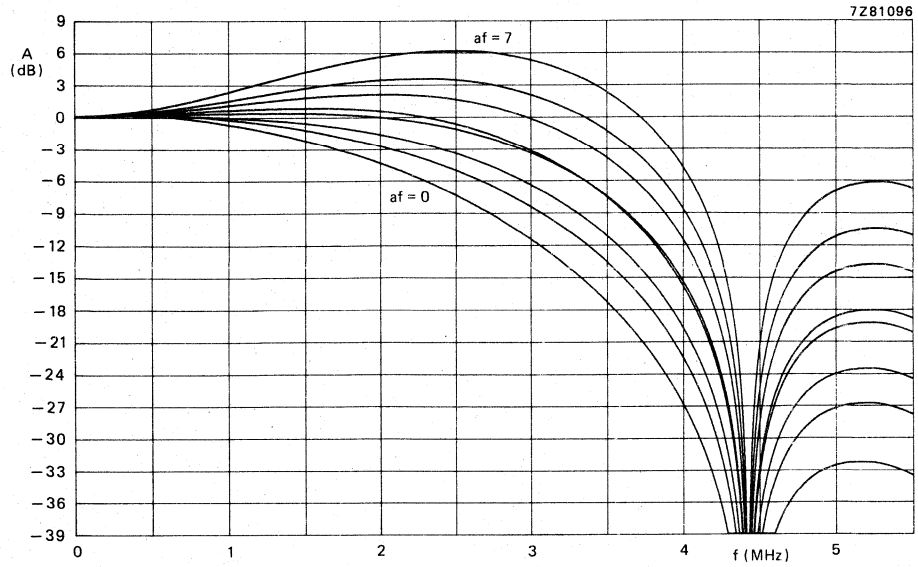


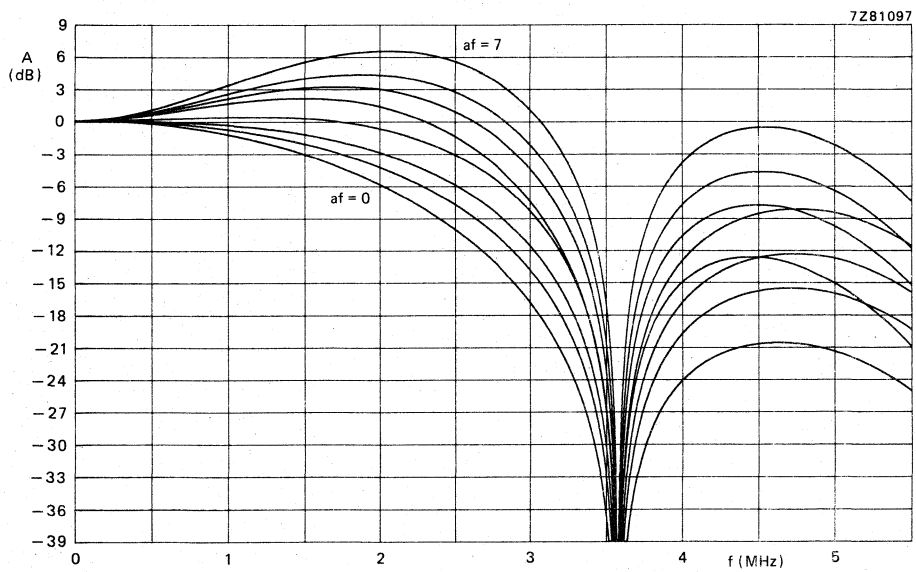
Fig. 12 Oscillator circuit requirements: (a) with quartz crystal; (b) with external clock.

DEVELOPMENT DATA

(a)



(b)



Aperture factor selection:

af	H2	H1	H0
0	0	0	0
---- through to ----			
7	1	1	1

Fig. 13 Horizontal peaking aperture factors (af): (a) YPN = logic 0 (colour subcarrier = 4,43 MHz); (b) YPN = logic 1 (colour subcarrier = 3,58 MHz).

PICTURE-IN-PICTURE CONTROLLER (PIPCO)

GENERAL DESCRIPTION

The SAA9068 is a controller for picture-in-picture applications. The PIPCO receives time multiplexed YUV data from an external analogue-to-digital converter (ADC) or from the Digital Vertical Filter (SAA9069). The device provides YUV data, via an internal digital-to-analogue converter (DAC), to the external filters. The device automatically detects the 50/60 Hz acquisition. Picture data is stored in an external 10 k by 8-bit SRAM. The device also produces the control signal for the SAA9069 (DVF). All features of the PIPCO are software controlled via an I^2C bus.

Features

- Automatic detection of acquisition signals
- Automatic detection of display signals
- The following features are software controlled via an I^2C bus:
  PIP ON/OFF
  border colour, one out of eight
  freeze PIP
  PIP top or bottom of screen
  PIP left or right of screen
  blank PIP
- Y-delay to compensate for delay differences in the pre-filters

QUICK REFERENCE DATA

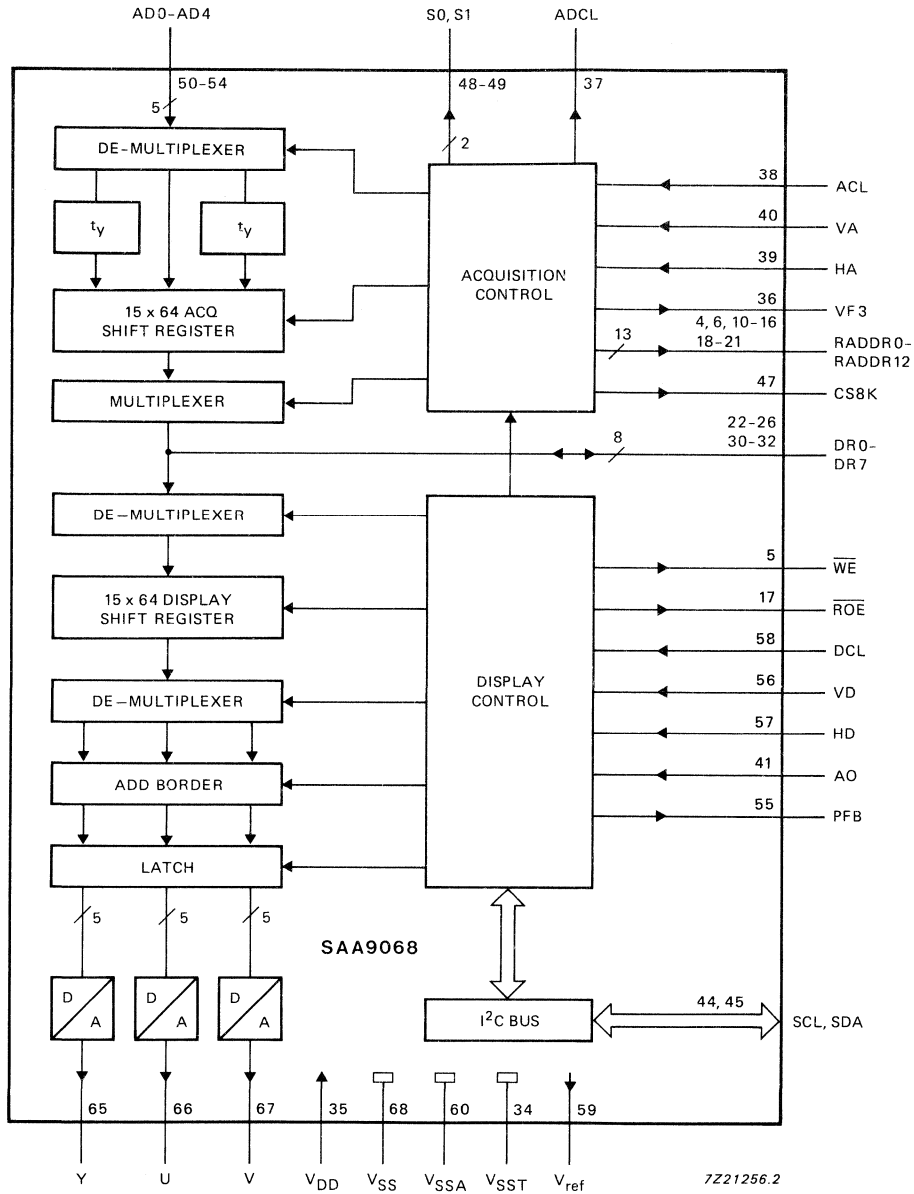
parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage range		V_{DD}	−0,5	–	7,0	V
Input voltage range	note 1	V_I	−0,5	–	V_{DD}+0,5	V
Maximum input current		I_{IM}	–	–	±10	mA
Maximum output current		I_{OM}	–	–	±10	mA
Inputs						
Input voltage LOW		V_{IL}	0	–	0,8	V
Input voltage HIGH		V_{IH}	2,0	–	V_{DD}	V
Input leakage current	T_{amb} = 25 °C	$\pm I_I$	–	–	1	μA
Outputs	except analogue outputs					
Output voltage LOW	I_{OL} = 0,8 mA	V_{OL}	0	–	0,4	V
Output voltage HIGH	I_{OH} = 0,8 mA	V_{OH}	V_{DD}−0,4	–	V_{DD}	V

Note to the Quick Reference Data

1. V_{DD} + 0,5 V must not exceed 7,0 V

PACKAGE OUTLINE

68-lead plastic leaded chip-carrier (SOT-188)



t_y = 3 periods of ADCL

Fig. 1 Block diagram.

DEVELOPMENT DATA

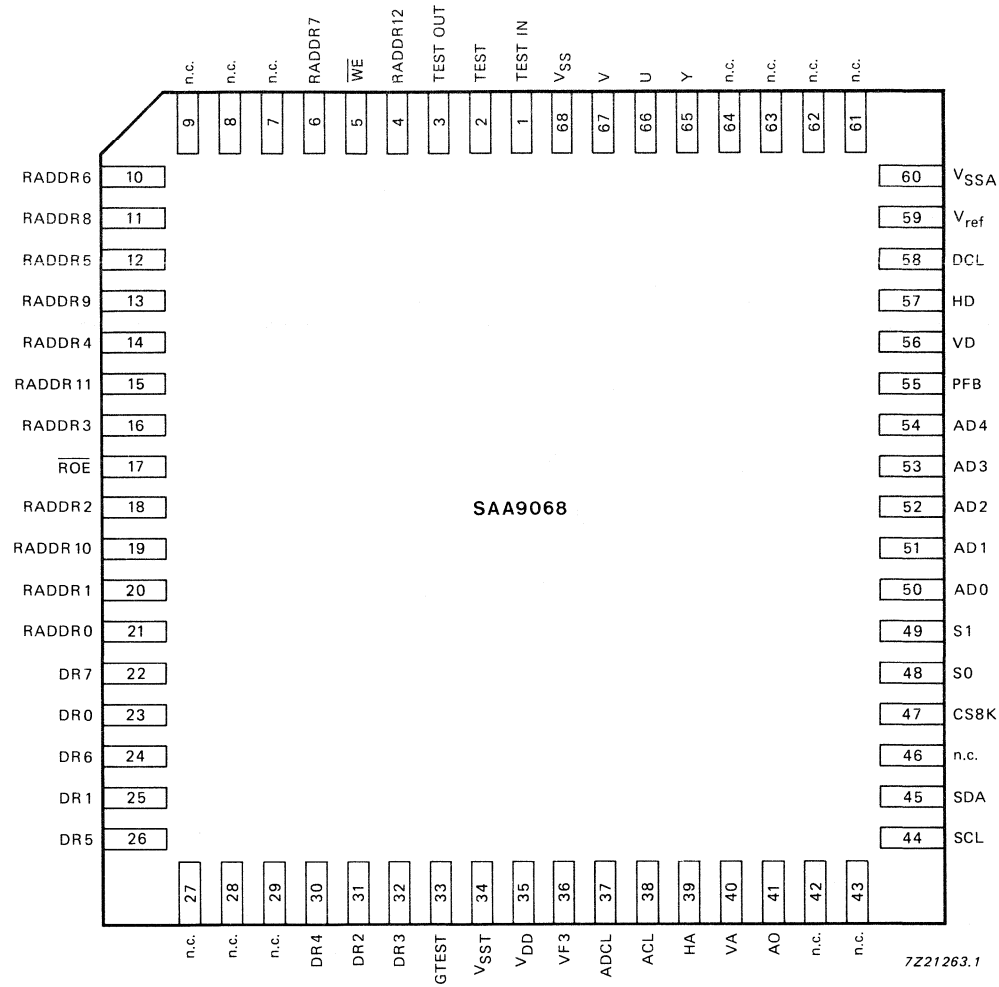


Fig. 2 Pinning diagram.

PINNING

pin	mnemonic	description
Power supplies		
34	V_{SST}	ground for dynamic shift registers
35	V_{DD}	positive supply voltage
60	V_{SSA}	ground for digital-to-analogue converters
68	V_{SS}	ground (0 V)
Inputs		
1	TEST IN	data input for testing the DAC
2	TEST	when HIGH, test mode for DAC enabled
33	GTEST	when LOW GTEST returns all memory elements to a known state, except for line memories
38	ACL	acquisition clock, typ. 10,9 MHz
39	HA	start of line in acquisition mode
40	VA	start of field in acquisition mode
41	A0	programming of I^2C bus slave address
50 to 54	AD0 to AD4	YUV data stream from ADC or SAA9069
56	VD	start of field in display mode
57	HD	start of line in display mode
58	DCL	display clock, typ. 15,8 MHz
Outputs		
3	TEST OUT	test data to DAC
4	RADDR12	SRAM address output
5	$\overline{WE}$	write enable (active LOW)
6	RADDR7	SRAM address output
10	RADDR6	SRAM address output
11	RADDR8	SRAM address output
12	RADDR5	SRAM address output
13	RADDR9	SRAM address output
14	RADDR4	SRAM address output
15	RADDR11	SRAM address output
16	RADDR3	SRAM address output
17	$\overline{ROE}$	RAM output enable (active LOW)
18	RADDR2	SRAM address output
19	RADDR10	SRAM address output
20	RADDR1	SRAM address output
21	RADDR0	SRAM address output
36	VF3	line selection to SAA9069
37	ADCL	acquisition clock signal (ACL/2) to ADC or SAA9069
47	CS8k	chip select for 8 k SRAM
48 to 49	S0 and S1	Y, U and V selection signal to analogue switch or SAA9069
55	PFB	picture-in-picture fast blanking
Inputs/outputs		
22 to 26, 30 to 32	DR0 to DR7	data to and from SRAM
44	SCL	I^2C bus clock
45	SDA	I^2C bus data signals

Analogue outputs

59	V_{ref}	voltage reference level for DAC
65	Y	analogue video signal from 5-bit DAC
66	U	analogue video signal from 5-bit DAC
67	V	analogue video signal from 5-bit DAC

Others

7 to 9, 27 to 29, 42, 43, 62 to 64	n.c.	not internally connected

FUNCTIONAL DESCRIPTION (see Fig. 1)

The YUV data stream is converted from analogue-to-digital data by the 5-bit ADC, this data is then stored in an acquisition line memory every third line. When enabled by the display section of the PIPCO, the data is transferred to the external SRAM. Data from the SRAM is transferred to the display line memory after which it is converted from digital to analogue by the DAC.

I²C bus (SDA; SCL)

The I²C bus provides bidirectional 2-line communication between different ICs or modules. The SDA is the serial data line; SCL is the serial clock line. Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

I²C bus format (slave address and receiver formats)

All 8 bits of the subaddress have to be decoded by the device. After power-on reset all control bits are set to zero. This device does not respond to the general call address.

0	0	1	0	0	1	A0	0

Fig. 3 Slave address.

DETAILED INFORMATION ON I²C BUS SPECIFICATION IS AVAILABLE ON REQUEST.

Table 1 Data byte format

	function							
	D7	D6	D5	D4	D3	D2	D1	D0
control	PIPON	STILL	BLPIP	TOP	LEFT	BOC2	BOC1	BOC0

Table 2 Definition of bits D7 to D3

bit	definition
PIPON	PIPON = 1, picture-in-picture is ON PIPON = 0, picture-in-picture is OFF
STILL	STILL = 1, still picture-in-picture STILL = 0, moving picture-in-picture
BLPIP	BLPIP = 1, blanking of picture-in-picture BLPIP = 0, display picture-in-picture
TOP	TOP = 1, picture-in-picture in upper part of screen TOP = 0, picture-in-picture in lower part of screen
LEFT	LEFT = 1, picture-in-picture in left part of screen LEFT = 0, picture-in-picture in right part of screen

Table 3 Colour reproduction

colour	BOC2	BOC1	BOC0	−U	−V
dark pink	0	0	0	0,00	−0,50
reddish brown	0	0	1	0,25	−0,50
light brown	0	1	0	0,50	−0,50
light purple	0	1	1	−0,25	−0,50
dark grey	1	0	0	0,00	0,00
dark green	1	0	1	0,25	0,00
green	1	1	0	0,50	0,00
medium blue	1	1	1	−0,20	0,00

If a function is not implemented, the bit related to this function is transmitted as a logic 0 and the general call address is not accepted. If no supply voltage is present, inputs SCL and SDA are in a high ohmic state.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage range		V_{DD}	−0,5	7,0	V
Input voltage range	note 1	V_I	−0,5	V_{DD}+0,5	V
Input current		I_I	−	±10	mA
Output current		I_O	−	±10	mA
Supply current in V_{SS}		I_{SS}	−	60	mA
Supply current in V_{DD}		I_{DD}	−	60	mA
Power dissipation per output		P	−	40	mW
Total power dissipation		P_{tot}	−	300	mW
Storage temperature range		T_{stg}	−55	+ 150	°C
Operating ambient temperature range		T_{amb}	−25	+ 70	°C

Note

1. V_{DD}+0,5 must not exceed 7,0 V.

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see 'Handling MOS Devices').

DEVELOPMENT DATA

DC CHARACTERISTICS

V_{DD} = 5 V ± 5%; T_{amb} = 0 to 70 °C; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply current						
Quiescent current	T_{amb} = 25 °C; all inputs to V_{DD} or V_{SS}	I_{DD}	–	–	175	μA
Inputs						
Input voltage LOW		V_{IL}	0	–	0,8	V
Input voltage HIGH		V_{IH}	2,0	–	V_{DD}	V
Input leakage current	T_{amb} = 25 °C; except GTEST	$\pm I_I$	–	–	1	μA
Input leakage current	GTEST	$\pm I_I$	–	–	30	μA
Outputs	except analogue outputs					
Output voltage LOW	I_{OL} = 0,8 mA	V_{OL}	0	–	0,4	V
Output voltage HIGH	I_{OH} = 0,8 mA	V_{OH}	V_{DD}–0,4	–	V_{DD}	V
Analogue outputs	Y, U, V at output load = 22 kΩ					
Output voltage LOW		V_{OL}	0,80	–	1,45	V
Output voltage HIGH		V_{OH}	3,75	–	4,75	V
Output level n+1 (step)	note 1	V_n	level n	level n + V_s	level n + 2V_s	V
Output voltage HIGH to output voltage LOW with 1 kΩ load		V_{OH}-V_{OL}	1,75	1,95	2,15	V
Voltage reference						
Output voltage	V_{DD} = 5 V	V_O	0,7	–	1,3	V

Note to the DC characteristics

1. $V_s = \frac{V_{OH}-V_{OL}}{31}$

AC CHARACTERISTICS

V_{DD} = 5 V ± 5%; T_{amb} = 0 to 70 °C; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Input capacitance		C_i	–	–	3	pF
AD0 - AD4 to ACL	Fig. 8					
data set-up time		$t_{SU;DAT}$	30	–	–	ns
data hold time		$t_{HD;DAT}$	10	–	–	ns
DR0 - DR7 to DCL	Fig. 7					
data set-up time		$t_{SU;DAT}$	30	–	–	ns
data hold time		$t_{HD;DAT}$	10	–	–	ns
HA, HD, VA, VD	notes 1 to 4					
ACL	note 5					
pulse width LOW		t_{WL}	25	–	–	ns
pulse width HIGH		t_{WH}	25	–	–	ns
rise time		t_r	–	–	7	ns
fall time		t_f	–	–	7	ns
frequency		f_{ACL}	–	10,9	–	MHz
DCL	note 6					
pulse width LOW		t_{WL}	18	–	–	ns
pulse width HIGH		t_{WH}	18	–	–	ns
rise time		t_r	–	–	4	ns
fall time		t_f	–	–	4	ns
frequency		f_{DCL}	–	15,8	–	MHz
Outputs	DCL = 15,8 MHz					
Load capacitance		C_L	–	–	20	pF
DCL to DR0 - DR7						
propagation delay	Fig. 6	t_d	10	–	135	ns
DCL to RADDR0 - RADDR12 and CS8K						
propagation delay	Fig. 6	t_d	0	–	70	ns
DCL to $\overline{ROE}$						
propagation delay	Fig. 6	t_d	0	–	150	ns
DCL to $\overline{WE}$ (falling edge)						
propagation delay	Fig. 6	t_d	70	–	105	ns
DCL to $\overline{WE}$ (rising edge)						
propagation delay	Fig. 6	t_d	195	–	235	ns
DCL to PFB						
propagation delay	Fig. 7	t_d	0	–	50	ns
ACL to ADCL						
propagation delay	Fig. 8	t_d	0	–	115	ns
ACL to S0 and S1						
propagation delay	Fig. 8	t_d	0	–	115	ns

DEVELOPMENT DATA

Notes to the AC characteristics

1. Pulse width HA (typ. 250 ns): the first sample of a line occurs after approximately 124 periods of ACL (counted on the negative edge of HA). The internal horizontal acquisition off-set value is chosen in such a way that ACL = 10,9 MHz, when this condition is satisfied the acquired picture is centralized within the PIP. The off-set value is dependent upon the acquisition frequency, 50 Hz or 60 Hz (124 ACL periods of 50 Hz and 108 ACL periods of 60 Hz). If the pulse width of HA increases, the acquired picture will shift to the left within the PIP picture (see Fig. 4).

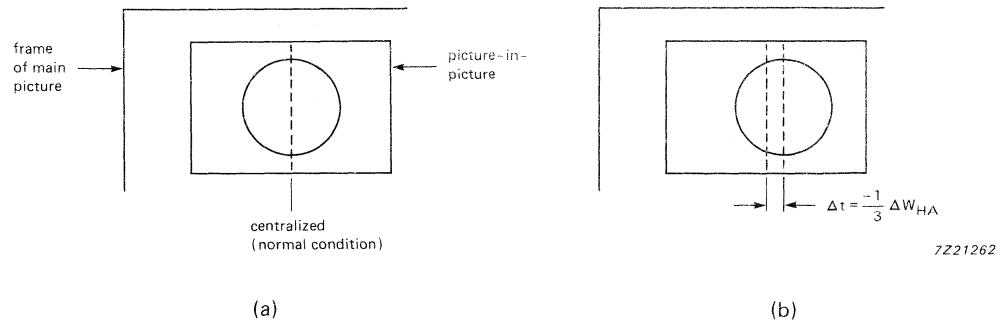


Fig. 4 PIP position; (a) ACL = 10,9 MHz, (b) $\Delta t = -1/3\ \Delta W_{HA}$.

2. Pulse width HD (typ. 250 ns): the first sample of a line is displayed after XXX periods of DCL with respect to the negative edge of HD. The internal horizontal display off-set is fixed in the hardware and depends upon the frequency (50 Hz or 60 Hz) and the right/left position of the display.
   The following values are implemented:

   - 50 Hz; position of display, right; t = 574 periods of DCL
   - 50 Hz; position of display, left; t = 134 periods of DCL
   - 60 Hz; position of display, right; t = 558 periods of DCL
   - 60 Hz; position of display, left; t = 126 periods of DCL

   If the pulse width of HD increases the distance between screen border and the left border of the PIP will enlarge and the picture will shift to the right. The width of the complete PIP, inclusive of border, is 268 clock pulses.

3. VA pulse width, minimum 8 pulses of ACL.

4. VD pulse width, minimum 5 pulses of DCL.

5. If ACL = k x 10,9 MHz, the effects are shown in Fig. 5:
   - if $k > 1$ then the acquired picture will be expanded horizontally and its centre will shift to the right.
   - if $k < 1$ then the acquired picture will be reduced horizontally and its center will shift to the left.

Fig. 5 PIP geometry; (a) $k > 1$, (b) $k < 1$.

6. DCL: if DCL $\neq$ 15,8 MHz but DCL = k x 15,8 MHz the effects are:
   - all horizontal sizes and values are multiplied by k.

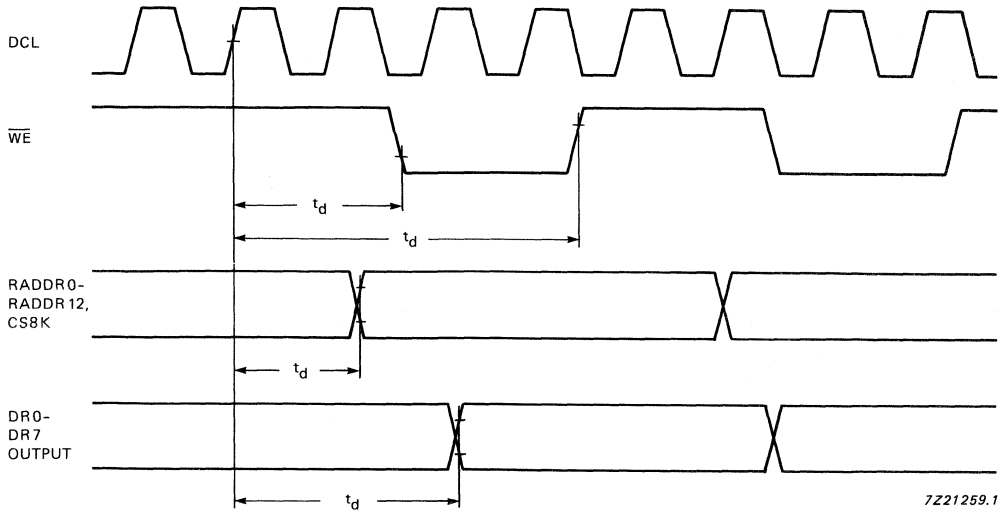


Fig. 6 Data and display clock timing waveform.

DEVELOPMENT DATA

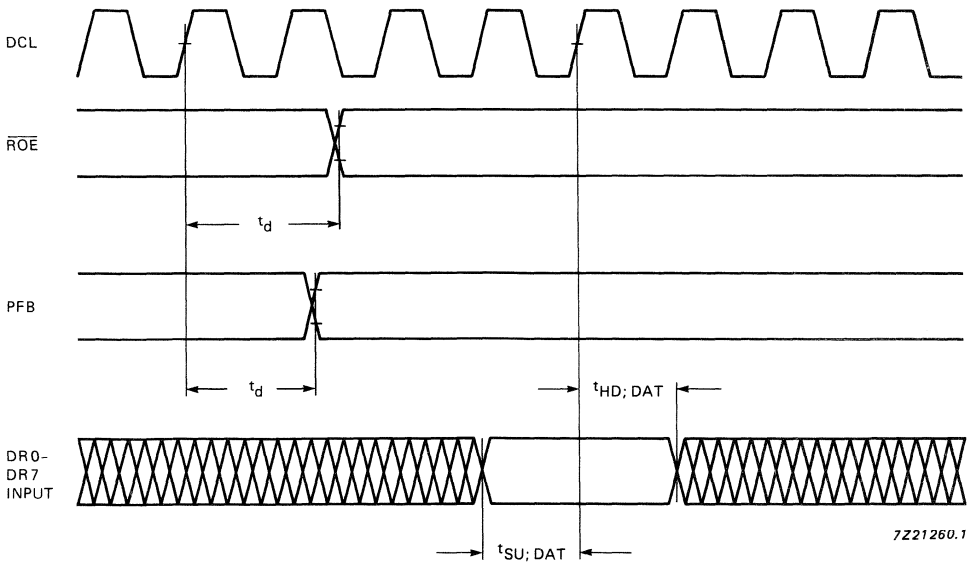


Fig. 7 Data and display clock timing waveform.

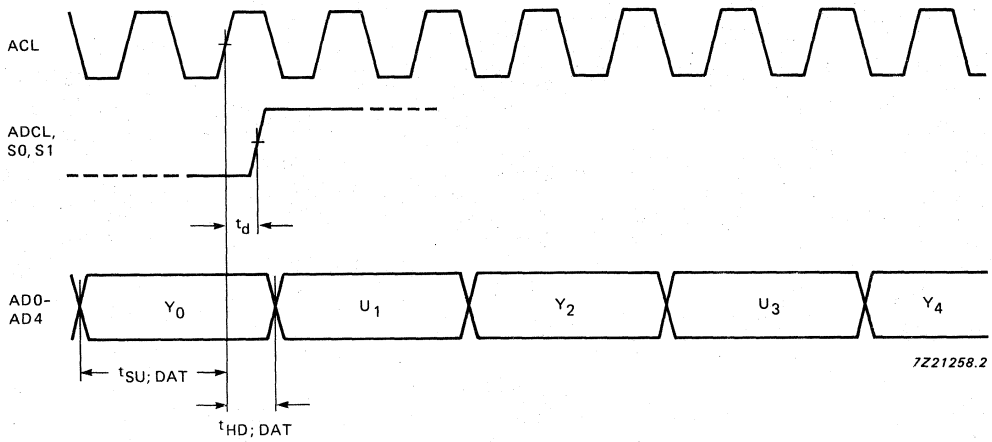


Fig. 8 Input data and acquisition clock waveform.

APPLICATION INFORMATION

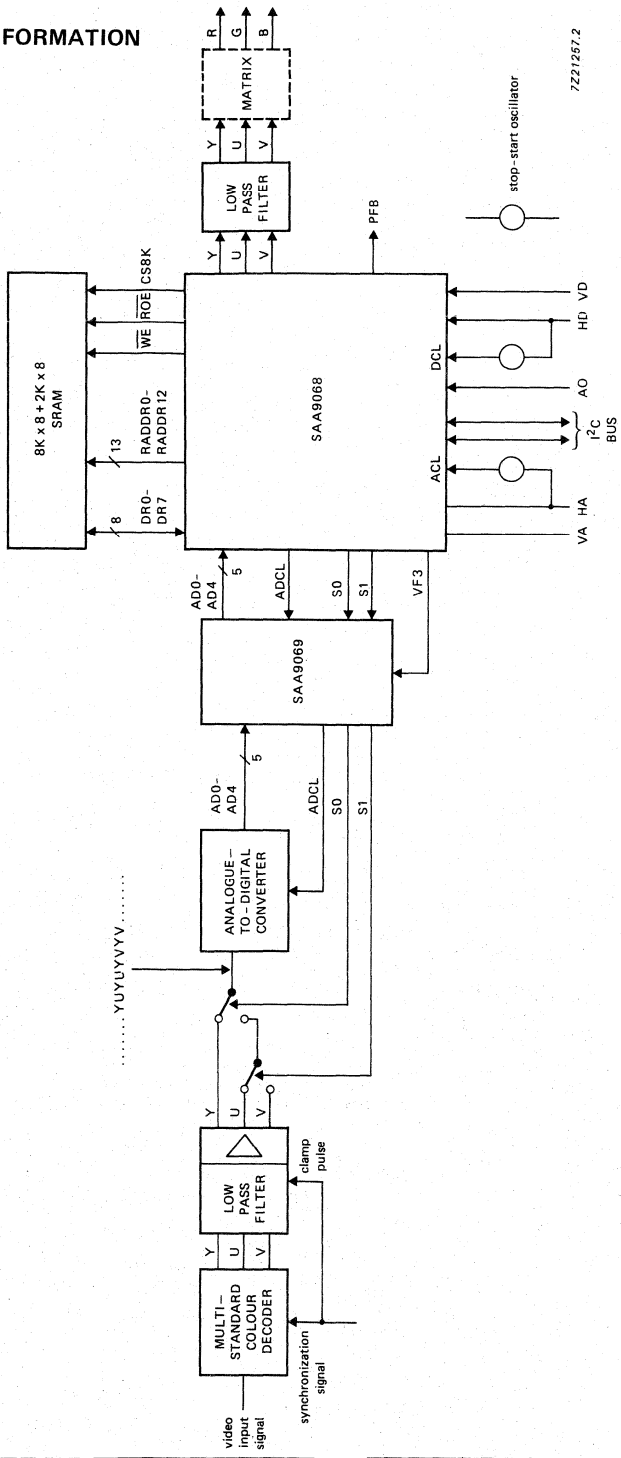


Fig. 9 Application diagram, using SAA9069.

DEVELOPMENT DATA

COMPUTER INTERFACE FOR TUNING AND CONTROL (CITAC)

GENERAL DESCRIPTION

The SAB3035 provides closed-loop digital tuning of TV receivers, with or without a.f.c., as required. It also controls up to 8 analogue functions, 4 general purpose I/O ports and 4 high-current outputs for tuner band selection.

The IC is used in conjunction with a microcomputer from the MAB8400 family and is controlled via a two-wire, bidirectional I^2C bus.

Features

- Combined analogue and digital circuitry minimizes the number of additional interfacing components required
- Frequency measurement with resolution of 50 kHz
- Selectable prescaler divisor of 64 or 256
- 32 V tuning voltage amplifier
- 4 high-current outputs for direct band selection
- 8 static digital to analogue converters (DACs) for control of analogue functions
- Four general purpose input/output (I/O) ports
- Tuning with control of speed and direction
- Tuning with or without a.f.c.
- Single-pin, 4 MHz on-chip oscillator
- I^2C bus slave transceiver

QUICK REFERENCE DATA

Supply voltages			
(pin 16)	V_{P1}	typ.	12 V
(pin 22)	V_{P2}	typ.	13 V
(pin 17)	V_{P3}	typ.	32 V
Supply currents (no outputs loaded)			
(pin 16)	I_{P1}	typ.	32 mA
(pin 22)	I_{P2}	typ.	0,1 mA
(pin 17)	I_{P3}	typ.	0,6 mA
Total power dissipation	P_{tot}	typ.	400 mW
Operating ambient temperature range	T_{amb}	−20 to +70	°C

PACKAGE OUTLINE

28-lead DIL; plastic (SOT-117).

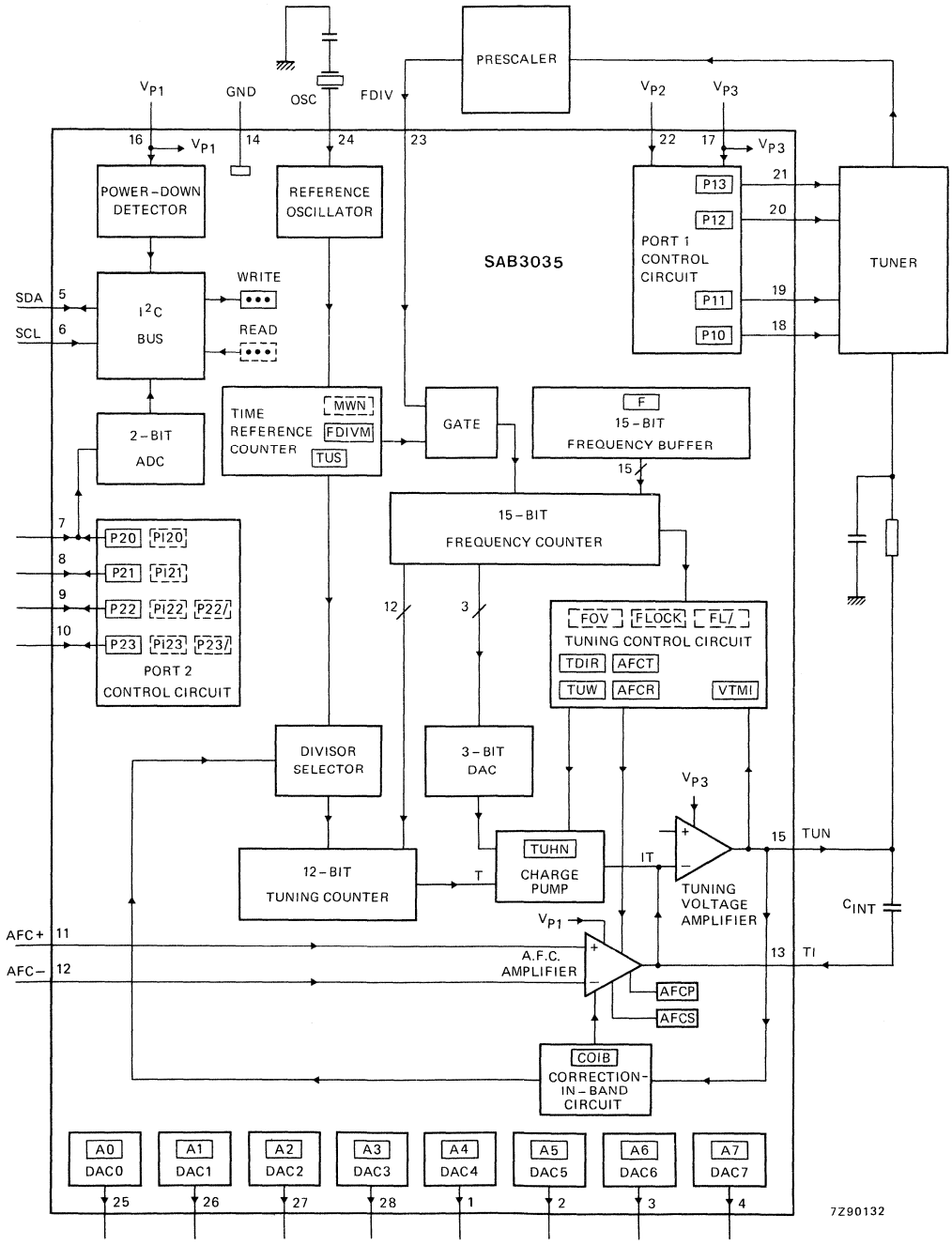


Fig. 1 Block diagram.

DEVELOPMENT DATA

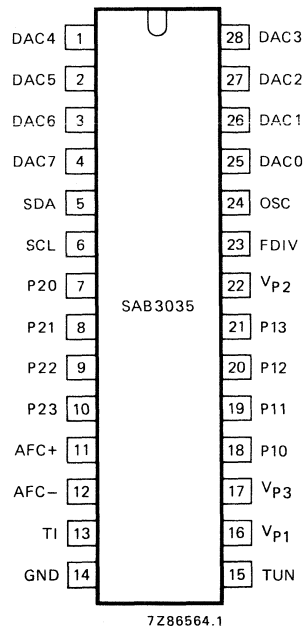


Fig. 2 Pinning diagram.

PINNING

1	DAC4	outputs of static DACs
2	DAC5	
3	DAC6	
4	DAC7	
5	SDA	serial data line (I²C bus)
6	SCL	serial clock line (I²C bus)
7	P20	general purpose input/output ports
8	P21	
9	P22	
10	P23	
11	AFC+	a.f.c. inputs
12	AFC−	
13	TI	tuning voltage amplifier inverting input
14	GND	ground
15	TUN	tuning voltage amplifier output
16	V_{P1}	+12 V supply voltage
17	V_{P3}	+32 V supply for tuning voltage amplifier
18	P10	High-current band-selection output ports
19	P11	
20	P12	
21	P13	
22	V_{P2}	positive supply for high-current band-selection output circuits
23	FDIV	input from prescaler
24	OSC	crystal oscillator input
25	DAC0	outputs of static DACs
26	DAC1	
27	DAC2	
28	DAC3	

FUNCTIONAL DESCRIPTION

The SAB3035 is a monolithic computer interface which provides tuning and control functions and operates in conjunction with a microcomputer via an I^2C bus.

Tuning

This is performed using frequency-locked loop digital control. Data corresponding to the required tuner frequency is stored in a 15-bit frequency buffer. The actual tuner frequency, divided by a factor of 256 (or by 64) by a prescaler, is applied via a gate to a 15-bit frequency counter. This input (FDIV) is measured over a period controlled by a time reference counter and is compared with the contents of the frequency buffer. The result of the comparison is used to control the tuning voltage so that the tuner frequency equals the contents of the frequency buffer multiplied by 50 kHz within a programmable tuning window (TUW).

The system cycles over a period of 6,4 ms (or 2,56 ms), controlled by the time reference counter which is clocked by an on-chip 4 MHz reference oscillator. Regulation of the tuning voltage is performed by a charge pump frequency-locked loop system. The charge IT flowing into the tuning voltage amplifier is controlled by the tuning counter, 3-bit DAC and the charge pump circuit. The charge IT is linear with the frequency deviation Δf in steps of 50 kHz. For loop gain control, the relationship $\Delta IT/\Delta f$ is programmable. In the normal mode (when control bits TUHN0 and TUHN1 are both at logic 1, see OPERATION), the minimum charge IT at $\Delta f = 50$ kHz equals 250 $\mu A\ \mu s$ (typical).

By programming the tuning sensitivity bits (TUS), the charge IT can be doubled up to 6 times. If correction-in-band (COIB) is programmed, the charge can be further doubled up to three times in relation to the tuning voltage level. From this, the maximum charge IT at $\Delta f = 50$ kHz equals $2^6 \times 2^3 \times 250\ \mu A\ \mu s$ (typical).

The maximum tuning current I is 875 μA (typical). In the tuning-hold (TUHN) mode (TUHN is active LOW), the tuning current I is reduced and as a consequence the charge into the tuning amplifier is also reduced.

An in-lock situation can be detected by reading FLOCK. When the tuner oscillator frequency is within the programmable tuning window (TUW), FLOCK is set to logic 1. If the frequency is also within the programmable a.f.c. hold range (AFCR), which always occurs if AFCR is wider than TUW, control bit AFCT can be set to logic 1. When set, digital tuning will be switched off, a.f.c. will be switched on and FLOCK will stay at logic 1 as long as the oscillator frequency is within AFCR. If the frequency of the tuning oscillator does not remain within AFCR, AFCT is cleared automatically and the system reverts to digital tuning. To be able to detect this situation, the occurrence of positive and negative transitions in the FLOCK signal can be read (FL/1N and FL/0N). AFCT can also be cleared by programming the AFCT bit to logic 0.

The a.f.c. has programmable polarity and transconductance; the latter can be doubled up to 3 times, depending on the tuning voltage level if correction-in-band is used.

The direction of tuning is programmable by using control bits TDIRD (tuning direction down) and TDIRU (tuning direction up). If a tuner enters a region in which oscillation stops, then, providing the prescaler remains stable, no FDIV signal is supplied to CITAC. In this situation the system will tune up, moving away from frequency lock-in. This situation is avoided by setting TDIRD which causes the system to tune down. In normal operation TDIRD must be cleared.

If a tuner stops oscillating and the prescaler becomes unstable by going into self-oscillation at a very high frequency, the system will react by tuning down, moving away from frequency lock-in. To overcome this, the system can be forced to tune up at the lowest sensitivity (TUS) value, by setting TDIRU.

Setting both TDIRD and TDIRU causes the digital tuning to be interrupted and a.f.c. to be switched on.

The minimum tuning voltage which can be generated during digital tuning is programmable by VTMI to prevent the tuner being driven into an unspecified low tuning voltage region.

Control

For tuner band selection there are four outputs P10 to P13 which are capable of sourcing up to 50 mA at a voltage drop of less than 600 mV with respect to the separate power supply input V_{P2}.

For additional digital control, four open collector I/O ports P20 to P23 are provided. Ports P22 and P23 are capable of detecting positive and negative transitions in their input signals. With the aid of port P20, up to three independent module addresses can be programmed.

Eight 6-bit digital-to-analogue converters DAC0 to DAC7 are provided for analogue control.

Reset

CITAC goes into the power-down-reset mode when V_{P1} is below 8,5 V (typical). In this mode all registers are set to a defined state. Reset can also be programmed.

OPERATION

Write

CITAC is controlled via a bidirectional two-wire I^2C bus; the I^2C bus is specified in our data handbook "ICs for digital systems in radio, audio, and video equipment". For programming, a module address, R/$\overline{W}$ bit (logic 0), an instruction byte and a data/control byte are written into CITAC in the format shown in Fig. 3.

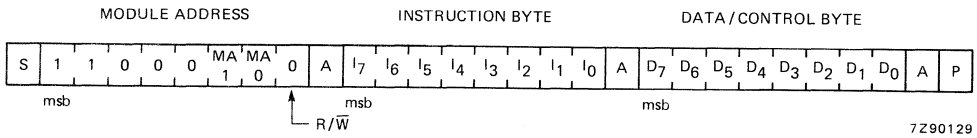


Fig. 3 I^2C bus write format.

The module address bits MA1, MA0 are used to give a 2-bit module address as a function of the voltage at port P20 as shown in Table 1.

Acknowledge (A) is generated by CITAC only when a valid address is received and the device is not in the power-down-reset mode ($V_{P1} > 8,5$ V (typical)).

Table 1 Valid module addresses

MA1	MA0	P20
0	0	don't care
0	1	GND
1	0	$\frac{1}{2}V_{P1}$
1	1	V_{P1}

OPERATION (continued)

Tuning

Tuning is controlled by the instruction and data/control bytes as shown in Fig. 4.

	INSTRUCTION BYTE								DATA/CONTROL BYTE							
	I_7	I_6	I_5	I_4	I_3	I_2	I_1	I_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
freq.	1	F14	F13	F12	F11	F10	F9	F8	F7	F6	F5	F4	F3	F2	F1	F0
TCD0	0	0	1	0	1	0	0	1	AFCT	VTMI0	AFCR1	AFCR0	TUHN1	TUHN0	TUW1	TUW0
TCD1	0	0	1	0	1	0	1	0	VTMI1	COIB1	COIB0	AFCS1	AFCS0	TUS2	TUS1	TUS0
TCD2	0	0	1	0	1	0	1	1	0	0	0	0	AFCP	FDIVM	TDIRD	TDIRU

7Z90125

Fig. 4 Tuning control format.

Frequency

Frequency is set when bit I_7 of the instruction byte is set to logic 1; the remainder of this byte together with the data/control byte are loaded into the frequency buffer. The frequency to which the tuner oscillator is regulated equals the decimal representation of the 15-bit word multiplied by 50 kHz. All frequency bits are set to logic 1 at reset.

Tuning hold

The TUHN bits are used to decrease the maximum tuning current and, as a consequence, the minimum charge IT (at Δf = 50 kHz) into the tuning amplifier.

Table 2 Tuning current control

TUHN1	TUHN0	typ. I_{max} μA	typ. IT_{min} $\mu A\ \mu s$	typ. ΔV_{TUNmin} at C_{INT} = 1 μF μV
0	0	3,5*	1*	1*
0	1	29	8	8
1	0	110	30	30
1	1	875	250	250

* Values after reset.

During tuning but before lock-in, the highest current value should be selected.
After lock-in the current may be reduced to decrease the tuning voltage ripple.

The lowest current value should not be used for tuning due to the input bias current of the tuning voltage amplifier (max. 5 nA). However it is good practice to program the lowest current value during tuner band switching.

Tuning sensitivity

To be able to program an optimum loop gain, the charge IT can be programmed by changing T using tuning sensitivity (TUS). Table 3 shows the minimum charge IT obtained by programming the TUS bits at Δf = 50 kHz; TUHN0 and TUHN1 = logic 1.

Table 3 Minimum charge IT as a function of TUS

Δf = 50 kHz; TUHN0 = logic 1; TUHN1 = logic 1

TUS2	TUS1	TUS0	typ. IT_{min} mA μs	typ. ΔV_{TUNmin} at C_{INT} = 1 μF mV
0	0	0	0,25*	0,25*
0	0	1	0,5	0,5
0	1	0	1	1
0	1	1	2	2
1	0	0	4	4
1	0	1	8	8
1	1	0	16	16

* Values after reset.

Correction-in-band

This control is used to correct the loop gain of the tuning system to reduce in-band variations due to a non-linear voltage/frequency characteristic of the tuner. Correction-in-band (COIB) controls the time T of the charge equation IT and takes into account the tuning voltage V_{TUN} to give charge multiplying factors as shown in Table 4.

DEVELOPMENT DATA

Table 4 Programming correction-in-band

COIB1	COIB0	charge multiplying factors at typical values of V_{TUN} at:			
		< 12 V	12 to 18 V	18 to 24 V	> 24 V
0	0	1*	1*	1*	1*
0	1	1	1	1	2
1	0	1	1	2	4
1	1	1	2	4	8

* Values after reset.

The transconductance multiplying factor of the a.f.c. amplifier is similar when COIB is used, except for the lowest transconductance which is not affected.

Tuning window

Digital tuning is interrupted and FLOCK is set to logic 1 (in-lock) when the absolute deviation $|\Delta f|$ between the tuner oscillator frequency and the programmed frequency is smaller than the programmed TUW value (see Table 5). If $|\Delta f|$ is up to 50 kHz above the values listed in Table 5, it is possible for the system to be locked depending on the phase relationship between FDIV and the reference counter.

Table 5 Tuning window programming

TUW1	TUW0	$\|\Delta f\|$ (kHz)	tuning window (kHz)
0	0	0*	0*
0	1	50	100
1	0	150	300

* Values after reset.

OPERATION (continued)

A.F.C.

When AFCT is set to logic 1 it will not be cleared and the a.f.c. will remain on as long as $|\Delta f|$ is less than the value programmed for the a.f.c. hold range AFCR (see Table 6). It is possible for the a.f.c. to remain on for values of up to 50 kHz more than the programmed value depending on the phase relationship between FDIV and the reference counter.

Table 6 A.F.C. hold range programming

AFCR1	AFCR0	$\|\Delta f\|$ (kHz)	a.f.c. hold range (kHz)
0	0	0*	0*
0	1	350	700
1	0	750	1500

* Values after reset.

Transconductance

The transconductance (g) of the a.f.c. amplifier is programmed via the a.f.c. sensitivity bits AFCS as shown in Table 7.

Table 7 Transconductance programming

AFCS1	AFCS0	typ. transconductance (μA/V)
0	0	0,25*
0	1	25
1	0	50
1	1	100

* Value after reset.

A.F.C. polarity

If a positive differential input voltage is applied to the (switched on) a.f.c. amplifier, the tuning voltage V_{TUN} falls when the a.f.c. polarity bit AFCP is at logic 0 (value after reset). At AFCP = logic 1, V_{TUN} rises.

Minimum tuning voltage

Both minimum tuning voltage control bits, VTMI1 and VTMI0, are at logic 0 after reset. Further details are given in CHARACTERISTICS.

Frequency measuring window

The frequency measuring window which is programmed must correspond with the division factor of the prescaler in use (see Table 8).

Table 8 Frequency measuring window programming

FDIVM	prescaler division factor	cycle period (ms)	measuring window (ms)
0	256	6,4*	5,12*
1	64	2,56	1,28

* Values after reset.

Tuning direction

Both tuning direction bits, TDIRU (up) and TDIRD (down), are at logic 0 after reset.

Control

The instruction bytes POD (port output data) and DACX (digital-to-analogue converter control) are shown in Fig. 5, together with the corresponding data/control bytes. Control is implemented as follows:

P13, P12, P11, P10 — Band select outputs. If a logic 1 is programmed on any of the POD bits D_3 to D_0, the relevant output goes HIGH. All outputs are LOW after reset.

P23, P22, P21, P20 — Open collector I/O ports. If a logic 0 is programmed on any of the POD bits D_7 to D_4, the relevant output is forced LOW. All outputs are at logic 1 after reset (high impedance state).

DACX — Digital-to-analogue converters. The digital-to-analogue converter selected corresponds to the decimal equivalent of the DACX bits X2, X1, X0. The output voltage of the selected DAC is set by programming the bits AX5 to AX0; the lowest output voltage is programmed with all data AX5 to AX0 at logic 0, or after reset has been activated.

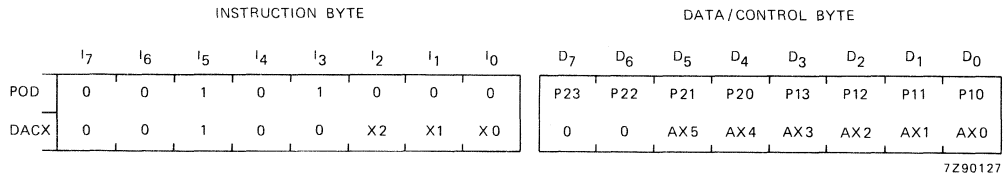


Fig. 5 Control programming.

Read

Information is read from CITAC when the R/$\overline{W}$ bit is set to logic 1. An acknowledge must be generated by the master after each data byte to allow transmission to continue. If no acknowledge is generated by the master the slave (CITAC) stops transmitting. The format of the information bytes is shown in Fig. 6.

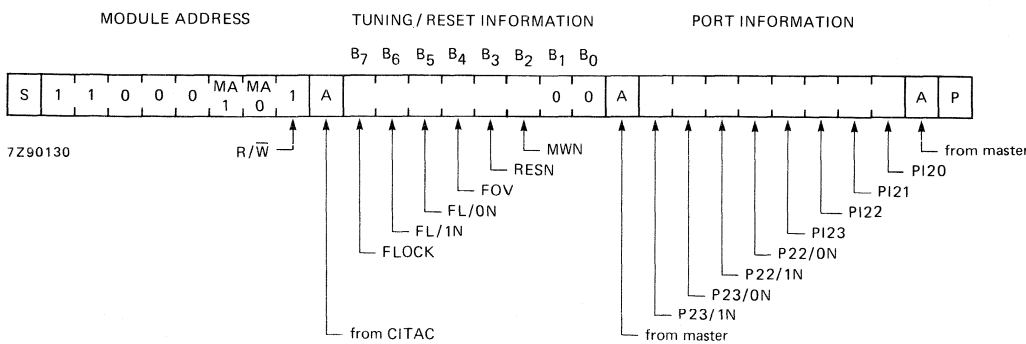


Fig. 6 Information byte format.

OPERATION (continued)

Tuning/reset information bits

FLOCK	Set to logic 1 when the tuning oscillator frequency is within the programmed tuning window.
FL/1N	Set to logic 0 (active LOW) when FLOCK changes from 0 to 1 and is reset to logic 1 automatically after tuning information has been read.
FL/0N	As for FL/1N but is set to logic 0 when FLOCK changes from 1 to 0.
FOV	Indicates frequency overflow. When the tuner oscillator frequency is too high with respect to the programmed frequency, FOV is at logic 1, and when too low, FOV is at logic 0. FOV is not valid when TDIRU and/or TDIRD are set to logic 1.
RESN	Set to logic 0 (active LOW) by a programmed reset or a power-down-reset. It is reset to logic 1 automatically after tuning/reset information has been read.
MWN	MWN (frequency measuring window, active LOW) is at logic 1 for a period of 1,28 ms, during which time the results of frequency measurement are processed. This time is independent of the cycle period. During the remaining time, MWN is at logic 0 and the received frequency is measured. When slightly different frequencies are programmed repeatedly and a.f.c. is switched on, the received frequency can be measured using FOV and FLOCK. To prevent the frequency counter and frequency buffer being loaded at the same time, frequency should be programmed only during the period of MWN = logic 0.

Port information bits

P23/1N, P22/1N	Set to logic 0 (active LOW) at a LOW-to-HIGH transition in the input voltage on P23 and P22 respectively. Both are reset to logic 1 after the port information has been read.
P23/0N, P22/0N	As for P23/1N and P22/1N but are set to logic 0 at a HIGH-to-LOW transition.
PI23, PI22, PI21, PI20	Indicate input voltage levels at P23, P22, P21 and P20 respectively. A logic 1 indicates a HIGH input level.

Reset

The programming to reset all registers is shown in Fig. 7. Reset is activated only at data byte HEX 06. Acknowledge is generated at every byte, provided that CITAC is not in the power-down-reset mode. After the general call address byte, transmission of more than one data byte is not allowed.

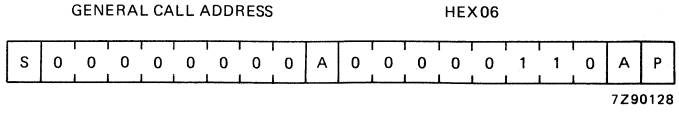


Fig. 7 Reset programming.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage ranges:			
(pin 16)	V_{P1}	−0,3 to +18	V
(pin 22)	V_{P2}	−0,3 to +18	V
(pin 17)	V_{P3}	−0,3 to +36	V
Input/output voltage ranges:			
(pin 5)	V_{SDA}	−0,3 to +18	V
(pin 6)	V_{SCL}	−0,3 to +18	V
(pins 7 to 10)	V_{P2X}	−0,3 to +18	V
(pins 11 and 12)	$V_{AFC+,AFC-}$	−0,3 to V_{P1}*	V
(pin 13)	V_{TI}	−0,3 to V_{P1}*	V
(pin 15)	V_{TUN}	−0,3 to V_{P3}*	V
(pins 18 to 21)	V_{P1X}	−0,3 to V_{P2}**	V
(pin 23)	V_{FDIV}	−0,3 to V_{P1}*	V
(pin 24)	V_{OSC}	−0,3 to +5	V
(pins 1 to 4 and 25 to 28)	V_{DACX}	−0,3 to V_{P1}*	V
Total power dissipation	P_{tot}	max. 1000	mW
Storage temperature range	T_{stg}	−55 to +125	°C
Operating ambient temperature range	T_{amb}	−20 to +70	°C

DEVELOPMENT DATA

* Pin voltage may exceed supply voltage if current is limited to 10 mA.

** Pin voltage must not exceed 18 V but may exceed V_{P2} if current is limited to 200 mA.

CHARACTERISTICS

T_{amb} = 25 °C; V_{P1}, V_{P2}, V_{P3} at typical voltages, unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply voltages	V_{P1}	10,5	12	13,5	V
	V_{P2}	4,7	13	16	V
	V_{P3}	30	32	35	V
Supply currents (no outputs loaded)	I_{P1}	20	32	50	mA
	I_{P2}	0	–	0,1	mA
	I_{P3}	0,2	0,6	2	mA
Additional supply currents (A)	I_{P2A}	−2	–	I_{OHP1X}	mA
(note 1)	I_{P3A}	0,2	–	2	mA
Total power dissipation	P_{tot}	–	400	–	mW
Operating ambient temperature	T_{amb}	−20	–	+70	°C
I^2C bus inputs/outputs					
SDA input (pin 5); SCL input (pin 6)					
Input voltage HIGH (note 2)	V_{IH}	3	–	$V_{P1}-1$	V
Input voltage LOW	V_{IL}	−0,3	–	1,5	V
Input current HIGH (note 2)	I_{IH}	–	–	10	μA
Input current LOW (note 2)	I_{IL}	–	–	10	μA
SDA output (pin 5, open collector)					
Output voltage LOW at I_{OL} = 3 mA	V_{OL}	–	–	0,4	V
Maximum output sink current	I_{OL}	–	5	–	mA
Open collector I/O ports					
P20, P21, P22, P23 (pins 7 to 10, open collector)					
Input voltage HIGH	V_{IH}	2	–	16	V
Input voltage LOW	V_{IL}	−0,3	–	0,8	V
Input current HIGH	I_{IH}	–	–	25	μA
Input current LOW	$-I_{IL}$	–	–	25	μA
Output voltage LOW at I_{OL} = 2 mA	V_{OL}	–	–	0,4	V
Maximum output sink current	I_{OL}	–	4	–	mA

parameter	symbol	min.	typ.	max.	unit
A.F.C. amplifier					
Inputs AFC+, AFC– (pins 11, 12)					
Transconductance for input voltages up to 1 V differential:					
AFCS1 AFCS2					
0 0	g_{00}	100	250	800	nA/V
0 1	g_{01}	15	25	35	μA/V
1 0	g_{10}	30	50	70	μA/V
1 1	g_{11}	60	100	140	μA/V
Tolerance of transconductance multiplying factor (2, 4 or 8) when correction-in-band is used	ΔM_g	–20	–	+20	%
Input offset voltage	V_{Ioff}	–75	–	+75	mV
Common mode input voltage	V_{com}	3	–	$V_{P1}-2,5$	V
Common mode rejection ratio	CMRR	–	50	–	dB
Power supply (V_{P1}) rejection ratio	PSRR	–	50	–	dB
Input current	I_I	–	–	500	nA
Tuning voltage amplifier					
Input TI, output TUN (pins 13, 15)					
Maximum output voltage at $I_{load} = \pm 2,5$ mA	V_{TUN}	$V_{P3}-1,6$	–	$V_{P3}-0,4$	V
Minimum output voltage at $I_{load} = \pm 2,5$ mA:					
VTMI1 VTMI0					
0 0	V_{TM00}	300	–	500	mV
1 0	V_{TM10}	450	–	650	mV
1 1	V_{TM11}	650	–	900	mV
Maximum output source current	$-I_{TUNH}$	2,5	–	8	mA
Maximum output sink current	I_{TUNL}	–	40	–	mA
Input bias current	I_{TI}	–5	–	+5	nA
Power supply (V_{P3}) rejection ratio	PSRR	–	60	–	dB

DEVELOPMENT DATA

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Tuning voltage amplifier (continued)					
Minimum charge IT to tuning voltage amplifier					
TUHN1 TUHN0					
0 0	CH_{00}	0,4	1	1,7	μA μs
0 1	CH_{01}	4	8	14	μA μs
1 0	CH_{10}	15	30	48	μA μs
1 1	CH_{11}	130	250	370	μA μs
Tolerance of charge (or ΔV_{TUN}) multiplying factor when COIB and/or TUS are used	ΔCH	−20	–	+20	%
Maximum current I into tuning amplifier					
TUHN1 TUHN0					
0 0	I_{T00}	1,7	3,5	5,1	μA
0 1	I_{T01}	15	29	41	μA
1 0	I_{T10}	65	110	160	μA
1 1	I_{T11}	530	875	1220	μA
Correction-in-band					
Tolerance of correction-in-band levels 12 V, 18 V and 24 V	ΔV_{CIB}	−15	–	+15	%
Band-select output ports					
P10, P11, P12, P13 (pins 18 to 21)					
Output voltage HIGH at $-I_{OH}$ = 50 mA (note 3)	V_{OH}	V_{P2}−0,6	–	–	V
Output voltage LOW at I_{OL} = 2 mA	V_{OL}	–	–	0,4	V
Maximum output source current (note 3)	$-I_{OH}$	–	130	200	mA
Maximum output sink current	I_{OL}	–	5	–	mA
FDIV input (pin 23)					
Input voltage (peak-to-peak value) (t_{rise} and $t_{fall} \leqslant 40$ ns)	$V_{FDIV(p-p)}$	0,1	–	2	V
Duty cycle	–	40	–	60	%
Maximum input frequency	f_{max}	14,5	–	–	MHz
Input impedance	Z_i	–	8	–	kΩ
Input capacitance	C_i	–	5	–	pF

parameter	symbol	min.	typ.	max.	unit
OSC input (pin 24)					
Crystal resistance at resonance (4 MHz)	R_X	–	–	150	Ω
DAC outputs 0 to 7 (pins 25 to 28 and 1 to 4)					
Maximum output voltage (no load) at V_{P1} = 12 V (note 4)	V_{DH}	10	–	11,5	V
Minimum output voltage (no load) at V_{P1} = 12 V (note 4)	V_{DL}	0,1	–	1	V
Positive value of smallest step (1 least-significant bit)	ΔV_D	0	–	350	mV
Deviation from linearity	–	–	–	0,5	V
Output impedance at $I_{load} = \pm 2$ mA	Z_o	–	–	70	Ω
Maximum output source current	$-I_{DH}$	–	–	6	mA
Maximum output sink current	I_{DL}	–	8	–	mA
Power-down-reset					
Maximum supply voltage V_{P1} at which power-down-reset is active	V_{PD}	7,5	–	9,5	V
V_{P1} rise-time during power-up (up to V_{PD})	t_r	5	–	–	μs
Voltage level for valid module address					
Voltage level at P20 (pin 7) for valid module address as a function of MA1, MA0					
MA1 MA0					
0 0	V_{VA00}	−0,3	–	16	V
0 1	V_{VA01}	−0,3	–	0,8	V
1 0	V_{VA10}	2,5	–	$V_{P1}-2$	V
1 1	V_{VA11}	$V_{P1}-0,3$	–	V_{P1}	V

DEVELOPMENT DATA

Notes to the characteristics

1. For each band-select output which is programmed at logic 1, sourcing a current I_{OHP1X}, the additional supply currents (A) shown must be added to I_{P2} and I_{P3} respectively.
2. If $V_{P1} < 1$ V, the input current is limited to 10 μA at input voltages up to 16 V.
3. At continuous operation the output current should not exceed 50 mA. When the output is short-circuited to ground for several seconds the device may be damaged.
4. Values are proportional to V_{P1}.

I^2C BUS TIMING (Fig. 8)

I^2C bus load conditions are as follows:
4 kΩ pull-up resistor to +5 V; 200 pF capacitor to GND.

All values are referred to V_{IH} = 3 V and V_{IL} = 1,5 V.

parameter	symbol	min.	typ.	max.	unit
Bus free before start	t_{BUF}	4	–	–	μs
Start condition set-up time	$t_{SU,STA}$	4	–	–	μs
Start condition hold time	$t_{HD,STA}$	4	–	–	μs
SCL, SDA LOW period	t_{LOW}	4	–	–	μs
SCL HIGH period	t_{HIGH}	4	–	–	μs
SCL, SDA rise time	t_R	–	–	1	μs
SCL, SDA fall time	t_F	–	–	0,3	μs
Data set-up time (write)	$t_{SU,DAT}$	1	–	–	μs
Data hold time (write)	$t_{HD,DAT}$	1	–	–	μs
Acknowledge (from CITAC) set-up time	$t_{SU,CAC}$	–	–	2	μs
Acknowledge (from CITAC) hold time	$t_{HD,CAC}$	0	–	–	μs
Stop condition set-up time	$t_{SU,STO}$	4	–	–	μs
Data set-up time (read)	$t_{SU,RDA}$	–	–	2	μs
Data hold time (read)	$t_{HD,RDA}$	0	–	–	μs
Acknowledge (from master) set-up time	$t_{SU,MAC}$	1	–	–	μs
Acknowledge (from master) hold time	$t_{HD,MAC}$	2	–	–	μs

Note

Timings $t_{SU,DAT}$ and $t_{HD,DAT}$ deviate from the I^2C bus specification .
After reset has been activated, transmission may only be started after a 50 μs delay.

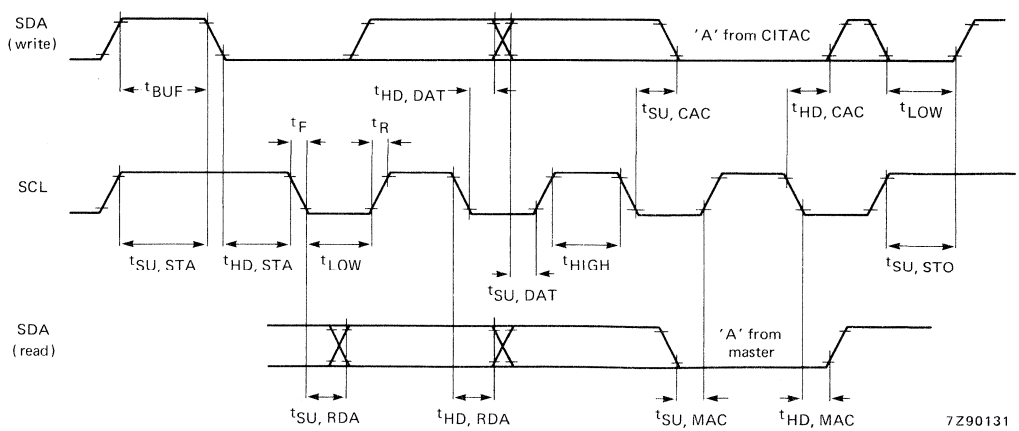


Fig. 8 I^2C bus timing SAB3035.

COMPUTER INTERFACE FOR TUNING AND CONTROL (CITAC)

GENERAL DESCRIPTION

The SAB3036 provides closed-loop digital tuning of TV receivers, with or without a.f.c., as required. It also controls 4 general purpose I/O ports and 4 high-current outputs for tuner band selection.

The IC is used in conjunction with a microcomputer from the MAB8400 family and is controlled via a two-wire, bidirectional I²C bus.

Features

- Combined analogue and digital circuitry minimizes the number of additional interfacing components required
- Frequency measurement with resolution of 50 kHz
- Selectable prescaler divisor of 64 or 256
- 32 V tuning voltage amplifier
- 4 high-current outputs for direct band selection
- Four general purpose input/output (I/O) ports
- Tuning with control of speed and direction
- Tuning with or without a.f.c.
- Single-pin, 4 MHz on-chip oscillator
- I²C bus slave transceiver

QUICK REFERENCE DATA

Supply voltages			
(pin 5)	V_{P1}	typ.	12 V
(pin 14)	V_{P2}	typ.	13 V
(pin 9)	V_{P3}	typ.	32 V
Supply currents (no outputs loaded)			
(pin 5)	I_{P1}	typ.	23 mA
(pin 14)	I_{P2}	typ.	0,1 mA
(pin 9)	I_{P3}	typ.	0,6 mA
Total power dissipation	P_{tot}	typ.	300 mW
Operating ambient temperature range	T_{amb}	−20 to + 70	°C

PACKAGE OUTLINE

18-lead DIL; plastic (SOT-102H).

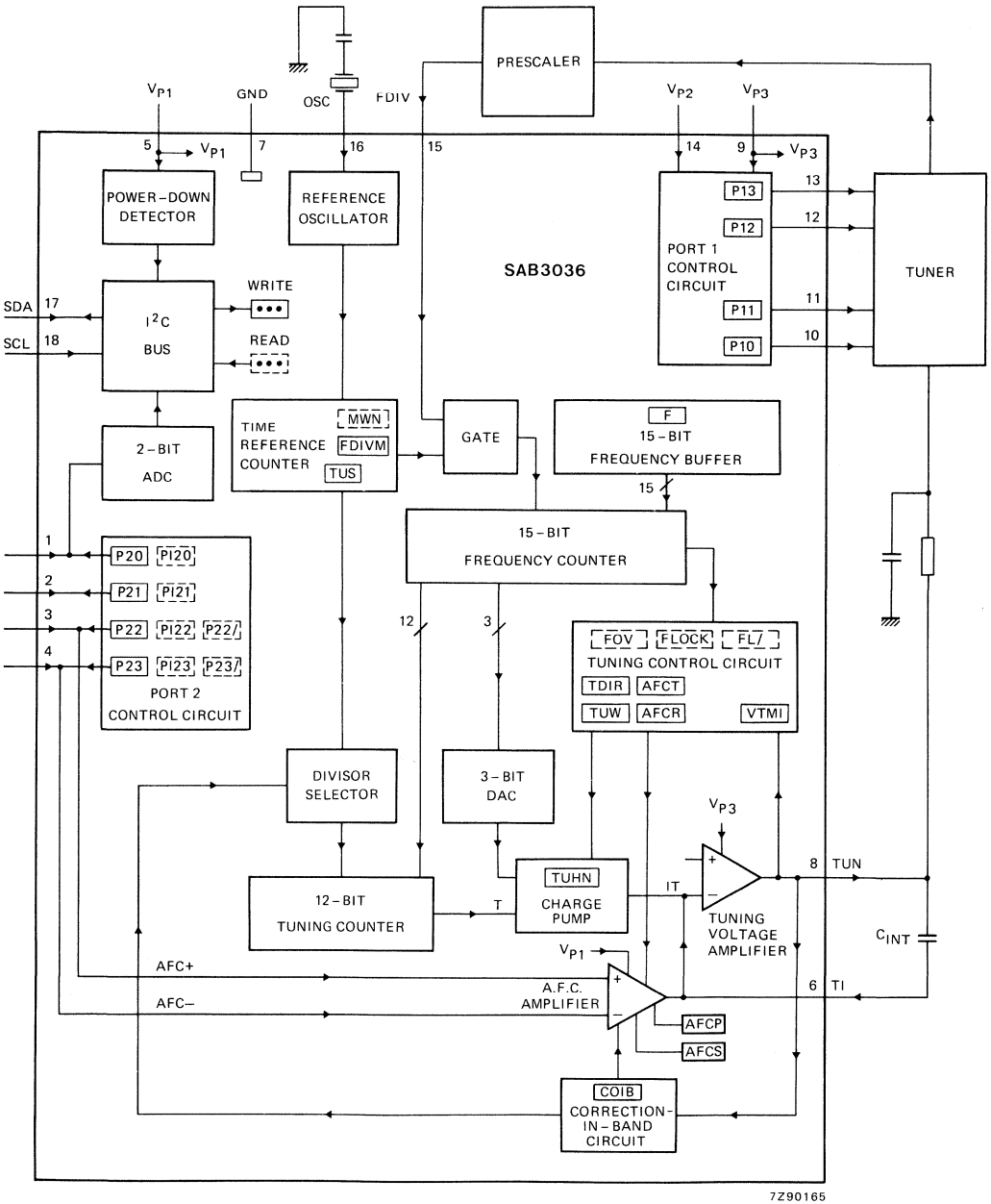


Fig. 1 Block diagram.

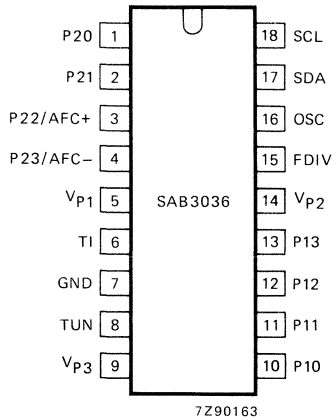


Fig. 2 Pinning diagram.

PINNING

1	P20	general purpose input/output ports
2	P21	
3	P22/AFC+	general purpose input/output ports and a.f.c. inputs
4	P23/AFC–	
5	V_{P1}	+ 12 V supply voltage
6	TI	tuning voltage amplifier inverting input
7	GND	ground
8	TUN	tuning voltage amplifier output
9	V_{P3}	+ 32 V supply for tuning voltage amplifier
10	P10	high-current band-selection output ports
11	P11	
12	P12	
13	P13	
14	V_{P2}	positive supply for high-current band-selection output circuits
15	FDIV	input from prescaler
16	OSC	crystal oscillator input
17	SDA	serial data line, I^2C bus
18	SCL	serial clock line, I^2C bus

DEVELOPMENT DATA

Purchase of Philips I^2C components conveys a licence under the Philips' I^2C patent to use the components in the I^2C system provided the system conforms to the I^2C specifications defined by Philips.

FUNCTIONAL DESCRIPTION

The SAB3036 is a monolithic computer interface which provides tuning and control functions and operates in conjunction with a microcomputer via an I^2C bus.

Tuning

This is performed using frequency-locked loop digital control. Data corresponding to the required tuner frequency is stored in a 15-bit frequency buffer. The actual tuner frequency, divided by a factor of 256 (or by 64) by a prescaler, is applied via a gate to a 15-bit frequency counter. This input (FDIV) is measured over a period controlled by a time reference counter and is compared with the contents of the frequency buffer. The result of the comparison is used to control the tuning voltage so that the tuner frequency equals the contents of the frequency buffer multiplied by 50 kHz within a programmable tuning window (TUW).

The system cycles over a period of 6,4 ms (or 2,56 ms), controlled by the time reference counter which is clocked by an on-chip 4 MHz reference oscillator. Regulation of the tuning voltage is performed by a charge pump frequency-locked loop system. The charge IT flowing into the tuning voltage amplifier is controlled by the tuning counter, 3-bit DAC and the charge pump circuit. The charge IT is linear with the frequency deviation Δf in steps of 50 kHz. For loop gain control, the relationship $\Delta IT/\Delta f$ is programmable. In the normal mode (when control bits TUHN0 and TUHN1 are both at logic 1, see OPERATION), the minimum charge IT at Δf = 50 kHz equals 250 μA μs (typical).

By programming the tuning sensitivity bits (TUS), the charge IT can be doubled up to 6 times. If correction-in-band (COIB) is programmed, the charge can be further doubled up to three times in relation to the tuning voltage level. From this, the maximum charge IT at Δf = 50 kHz equals $2^6 \times 2^3 \times 250$ μA μs (typical).

The maximum tuning current I is 875 μA (typical). In the tuning-hold (TUHN) mode (TUHN is active LOW), the tuning current I is reduced and as a consequence the charge into the tuning amplifier is also reduced.

An in-lock situation can be detected by reading FLOCK. When the tuner oscillator frequency is within the programmable tuning window (TUW), FLOCK is set to logic 1. If the frequency is also within the programmable a.f.c. hold range (AFCR), which always occurs if AFCR is wider than TUW, control bit AFCT can be set to logic 1. When set, digital tuning will be switched off, a.f.c. will be switched on and FLOCK will stay at logic 1 as long as the oscillator frequency is within AFCR. If the frequency of the tuning oscillator does not remain within AFCR, AFCT is cleared automatically and the system reverts to digital tuning. To be able to detect this situation, the occurrence of positive and negative transitions in the FLOCK signal can be read (FL/1N and FL/0N). AFCT can also be cleared by programming the AFCT bit to logic 0.

The a.f.c. has programmable polarity and transconductance; the latter can be doubled up to 3 times, depending on the tuning voltage level if correction-in-band is used.

The direction of tuning is programmable by using control bits TDIRD (tuning direction down) and TDIRU (tuning direction up). If a tuner enters a region in which oscillation stops, then, providing the prescaler remains stable, no FDIV signal is supplied to CITAC. In this situation the system will tune up, moving away from frequency lock-in. This situation is avoided by setting TDIRD which causes the system to tune down. In normal operation TDIRD must be cleared.

If a tuner stops oscillating and the prescaler becomes unstable by going into self-oscillation at a very high frequency, the system will react by tuning down, moving away from frequency lock-in. To overcome this, the system can be forced to tune up at the lowest sensitivity (TUS) value, by setting TDIRU.

Setting both TDIRD and TDIRU causes the digital tuning to be interrupted and a.f.c. to be switched on.

The minimum tuning voltage which can be generated during digital tuning is programmable by VTMI to prevent the tuner being driven into an unspecified low tuning voltage region.

Control

For tuner band selection there are four outputs P10 to P13 which are capable of sourcing up to 50 mA at a voltage drop of less than 600 mV with respect to the separate power supply input V_{P2}.

For additional digital control, four open collector I/O ports P20 to P23 are provided. Ports P22 and P23 are capable of detecting positive and negative transitions in their input signals and are connected with the AFC+ and AFC− inputs respectively. The a.f.c. amplifier must be switched off when P22 and/or P23 are used. When a.f.c. is used, P22 and P23 must be programmed HIGH (high impedance state). With the aid of port P20, up to three independent module addresses can be programmed.

Reset

CITAC goes into the power-down-reset mode when V_{P1} is below 8,5 V (typical). In this mode all registers are set to a defined state. Reset can also be programmed.

OPERATION

Write

CITAC is controlled via a bidirectional two-wire I^2C bus; the I^2C bus is specified in our data handbook "ICs for digital systems in radio, audio, and video equipment". For programming, a module address, R/$\overline{W}$ bit (logic 0), an instruction byte and a data/control byte are written into CITAC in the format shown in Fig. 3.

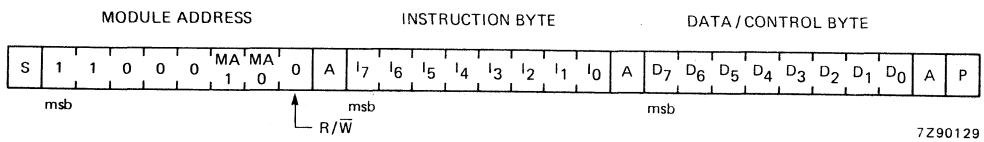


Fig. 3 I^2C bus write format.

The module address bits MA1, MA0 are used to give a 2-bit module address as a function of the voltage at port P20 as shown in Table 1.

Acknowledge (A) is generated by CITAC only when a valid address is received and the device is not in the power-down-reset mode ($V_{P1} > 8,5$ V (typical)).

OPERATION (continued)

Table 1 Valid module addresses

MA1	MA0	P20
0	0	don't care
0	1	GND
1	0	$\frac{1}{2}V_{P1}$
1	1	V_{P1}

Tuning

Tuning is controlled by the instruction and data/control bytes as shown in Fig. 4.

INSTRUCTION BYTE

	I_7	I_6	I_5	I_4	I_3	I_2	I_1	I_0
freq.	1	F14	F13	F12	F11	F10	F9	F8
TCD0	0	0	1	0	1	0	0	1
TCD1	0	0	1	0	1	0	1	0
TCD2	0	0	1	0	1	0	1	1

DATA/CONTROL BYTE

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
F7	F6	F5	F4	F3	F2	F1	F0
AFCT	VTMI0	AFCR1	AFCR0	TUHN1	TUHN0	TUW1	TUW0
VTMI1	COIB1	COIB0	AFCS1	AFCS0	TUS2	TUS1	TUS0
0	0	0	0	AFCP	FDIVM	TDIRD	TDIRU

7Z90125

Fig. 4 Tuning control format.

Frequency

Frequency is set when bit I_7 of the instruction byte is set to logic 1; the remainder of this byte together with the data/control byte are loaded into the frequency buffer. The frequency to which the tuner oscillator is regulated equals the decimal representation of the 15-bit word multiplied by 50 kHz. All frequency bits are set to logic 1 at reset.

Tuning hold

The TUHN bits are used to decrease the maximum tuning current and, as a consequence, the minimum charge IT (at Δf = 50 kHz) into the tuning amplifier.

Table 2 Tuning current control

TUHN1	TUHN0	typ. I_{max} μA	typ. IT_{min} $\mu A\ \mu s$	typ. ΔV_{TUNmin} at C_{INT} = 1 μF μV
0	0	3,5*	1*	1*
0	1	29	8	8
1	0	110	30	30
1	1	875	250	250

* Values after reset.

During tuning but before lock-in, the highest current value should be selected.
After lock-in the current may be reduced to decrease the tuning voltage ripple.

The lowest current value should not be used for tuning due to the input bias current of the tuning voltage amplifier (max. 5 nA). However it is good practice to program the lowest current value during tuner band switching.

Tuning sensitivity

To be able to program an optimum loop gain, the charge IT can be programmed by changing T using tuning sensitivity (TUS). Table 3 shows the minimum charge IT obtained by programming the TUS bits at $\Delta f = 50$ kHz; TUHN0 and TUHN1 = logic 1.

Table 3 Minimum charge IT as a function of TUS

$\Delta f = 50$ kHz; TUHN0 = logic 1; TUHN1 = logic 1

TUS2	TUS1	TUS0	typ. IT_{min} mA μs	typ. ΔV_{TUNmin} at $C_{INT} = 1\ \mu F$ mV
0	0	0	0,25*	0,25*
0	0	1	0,5	0,5
0	1	0	1	1
0	1	1	2	2
1	0	0	4	4
1	0	1	8	8
1	1	0	16	16

* Values after reset.

DEVELOPMENT DATA

Correction-in-band

This control is used to correct the loop gain of the tuning system to reduce in-band variations due to a non-linear voltage/frequency characteristic of the tuner. Correction-in-band (COIB) controls the time T of the charge equation IT and takes into account the tuning voltage V_{TUN} to give charge multiplying factors as shown in Table 4.

Table 4 Programming correction-in-band

COIB1	COIB0	charge multiplying factors at typical values of V_{TUN} at:			
		< 12 V	12 to 18 V	18 to 24 V	> 24 V
0	0	1*	1*	1*	1*
0	1	1	1	1	2
1	0	1	1	2	4
1	1	1	2	4	8

* Values after reset.

The transconductance multiplying factor of the a.f.c. amplifier is similar when COIB is used, except for the lowest transconductance which is not affected.

Tuning window

Digital tuning is interrupted and FLOCK is set to logic 1 (in-lock) when the absolute deviation $|\Delta f|$ between the tuner oscillator frequency and the programmed frequency is smaller than the programmed TUW value (see Table 5). If $|\Delta f|$ is up to 50 kHz above the values listed in Table 5, it is possible for the system to be locked depending on the phase relationship between FDIV and the reference counter.

OPERATION (continued)

Table 5 Tuning window programming

TUW1	TUW0	|Δf| (kHz)	tuning window (kHz)
0	0	0*	0*
0	1	50	100
1	0	150	300

* Values after reset.

A.F.C.

When AFCT is set to logic 1 it will not be cleared and the a.f.c. will remain on as long as |Δf| is less than the value programmed for the a.f.c. hold range AFCR (see Table 6). It is possible for the a.f.c. to remain on for values of up to 50 kHz more than the programmed value depending on the phase relationship between FDIV and the reference counter.

Table 6 A.F.C. hold range programming

AFCR1	AFCR0	|Δf| (kHz)	a.f.c. hold range (kHz)
0	0	0*	0*
0	1	350	700
1	0	750	1500

* Values after reset.

Transconductance

The transconductance (g) of the a.f.c. amplifier is programmed via the a.f.c. sensitivity bits AFCS as shown in Table 7.

Table 7 Transconductance programming

AFCS1	AFCS0	typ. transconductance (μA/V)
0	0	0,25*
0	1	25
1	0	50
1	1	100

* Value after reset.

A.F.C. polarity

If a positive differential input voltage is applied to the (switched on) a.f.c. amplifier, the tuning voltage V_{TUN} falls when the a.f.c. polarity bit AFCP is at logic 0 (value after reset). At AFCP = logic 1, V_{TUN} rises.

Minimum tuning voltage

Both minimum tuning voltage control bits, VTMI1 and VTMI0, are at logic 0 after reset. Further details are given in CHARACTERISTICS.

Frequency measuring window

The frequency measuring window which is programmed must correspond with the division factor of the prescaler in use (see Table 8).

Table 8 Frequency measuring window programming

FDIVM	prescaler division factor	cycle period (ms)	measuring window (ms)
0	256	6,4*	5,12*
1	64	2,56	1,28

* Values after reset.

Tuning direction

Both tuning direction bits, TDIRU (up) and TDIRD (down), are at logic 0 after reset.

Control

The instruction byte POD (port output data) is shown in Fig. 5, together with the corresponding data/control byte. Control is implemented as follows:

P13, P12, P11, P10 — Band select outputs. If a logic 1 is programmed on any of the POD bits D_3 to D_0, the relevant output goes HIGH. All outputs are LOW after reset.

P23, P22, P21, P20 — Open collector I/O ports. If a logic 0 is programmed on any of the POD bits D_7 to D_4, the relevant output is forced LOW. All outputs are at logic 1 after reset (high impedance state).

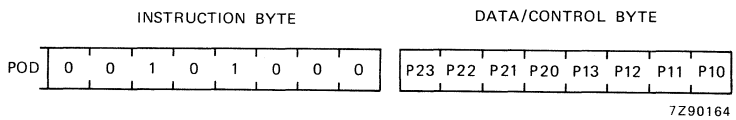


Fig. 5 Control programming.

OPERATION (continued)

Read

Information is read from CITAC when the R/$\overline{W}$ bit is set to logic 1. An acknowledge must be generated by the master after each data byte to allow transmission to continue. If no acknowledge is generated by the master the slave (CITAC) stops transmitting. The format of the information bytes is shown in Fig. 6.

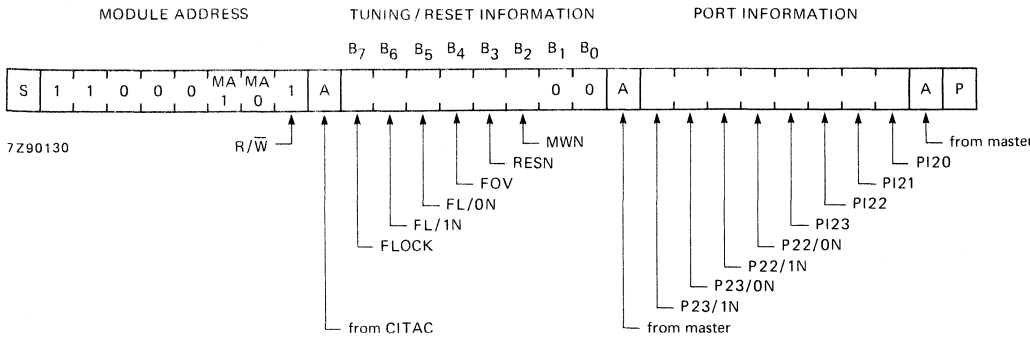


Fig. 6 Information byte format.

Tuning/reset information bits

FLOCK	Set to logic 1 when the tuning oscillator frequency is within the programmed tuning window.
FL/1N	Set to logic 0 (active LOW) when FLOCK changes from 0 to 1 and is reset to logic 1 automatically after tuning information has been read.
FL/0N	As for FL/1N but is set to logic 0 when FLOCK changes from 1 to 0.
FOV	Indicates frequency overflow. When the tuner oscillator frequency is too high with respect to the programmed frequency, FOV is at logic 1, and when too low, FOV is at logic 0. FOV is not valid when TDIRU and/or TDIRD are set to logic 1.
RESN	Set to logic 0 (active LOW) by a programmed reset or a power-down-reset. It is reset to logic 1 automatically after tuning/reset information has been read.
MWN	MWN (frequency measuring window, active LOW) is at logic 1 for a period of 1,28 ms, during which time the results of frequency measurement are processed. This time is independent of the cycle period. During the remaining time, MWN is at logic 0 and the received frequency is measured. When slightly different frequencies are programmed repeatedly and a.f.c. is switched on, the received frequency can be measured using FOV and FLOCK. To prevent the frequency counter and frequency buffer being loaded at the same time, frequency should be programmed only during the period of MWN = logic 0.

Port information bits

P23/1N, P22/1N	Set to logic 0 (active LOW) at a LOW-to-HIGH transition in the input voltage on P23 and P22 respectively. Both are reset to logic 1 after the port information has been read.
P23/0N, P22/0N	As for P23/1N and P22/1N but are set to logic 0 at a HIGH-to-LOW transition.
PI23, PI22, PI21, PI20	Indicate input voltage levels at P23, P22, P21 and P20 respectively. A logic 1 indicates a HIGH input level.

Reset

The programming to reset all registers is shown in Fig. 7. Reset is activated only at data byte HEX 06. Acknowledge is generated at every byte, provided that CITAC is not in the power-down-reset mode. After the general call address byte, transmission of more than one data byte is not allowed.

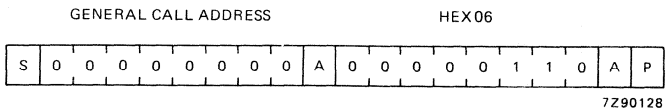


Fig. 7 Reset programming.

DEVELOPMENT DATA

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage ranges:		
(pin 5)	V_{P1}	−0,3 to + 18 V
(pin 14)	V_{P2}	−0,3 to + 18 V
(pin 9)	V_{P3}	−0,3 to + 36 V
Input/output voltage ranges:		
(pin 17)	V_{SDA}	−0,3 to + 18 V
(pin 18)	V_{SCL}	−0,3 to + 18 V
(pins 1 and 2)	$V_{P20, P21}$	−0,3 to + 18 V
(pins 3 and 4)	$V_{P22, P23, AFC}$	−0,3 to V_{P1}* V
(pin 6)	V_{TI}	−0,3 to V_{P1}* V
(pin 8)	V_{TUN}	−0,3 to V_{P3}* V
(pins 10 to 13)	V_{P1X}	−0,3 to V_{P2}** V
(pin 15)	V_{FDIV}	−0,3 to V_{P1}* V
(pin 16)	V_{OSC}	−0,3 to + 5 V
Total power dissipation	P_{tot}	max. 1000 mW
Storage temperature range	T_{stg}	−55 to + 125 °C
Operating ambient temperature	T_{amb}	−20 to + 70 °C

* Pin voltage may exceed supply voltage if current is limited to 10 mA.
** Pin voltage must not exceed 18 V but may exceed V_{P2} if current is limited to 200 mA.

CHARACTERISTICS

T_{amb} = 25 °C; V_{P1}, V_{P2}, V_{P3} at typical voltages, unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply voltages	V_{P1}	10,5	12	13,5	V
	V_{P2}	4,7	13	16	V
	V_{P3}	30	32	35	V
Supply currents (no outputs loaded)	I_{P1}	14	23	40	mA
	I_{P2}	0	–	0,1	mA
	I_{P3}	0,2	0,6	2	mA
Additional supply currents (A)	I_{P2A}	–2	–	I_{OHP1X}	mA
(note 1)	I_{P3A}	0,2	–	2	mA
Total power dissipation	P_{tot}	–	300	–	mW
Operating ambient temperature	T_{amb}	–20	–	+70	°C
I^2C bus inputs/outputs					
SDA input (pin 17); SCL input (pin 18)					
Input voltage HIGH (note 2)	V_{IH}	3	–	$V_{P1}-1$	V
Input voltage LOW	V_{IL}	–0,3	–	1,5	V
Input current HIGH (note 2)	I_{IH}	–	–	10	μA
Input current LOW (note 2)	I_{IL}	–	–	10	μA
SDA output (pin 17, open collector)					
Output voltage LOW at I_{OL} = 3 mA	V_{OL}	–	–	0,4	V
Maximum output sink current	I_{OL}	–	5	–	mA
Open collector I/O ports					
P20, P21, P22, P23 (pins 1 to 4, open collector)					
Input voltage HIGH (P20, P21)	V_{IH}	2	–	16	V
Input voltage HIGH (P22, P23) AFC switched off	V_{IH}	2	–	$V_{P1}-2$	V
Input voltage LOW	V_{IL}	–0,3	–	0,8	V
Input current HIGH	I_{IH}	–	–	25	μA
Input current LOW	$-I_{IL}$	–	–	25	μA
Output voltage LOW at I_{OL} = 2 mA	V_{OL}	–	–	0,4	V
Maximum output sink current	I_{OL}	–	4	–	mA

DEVELOPMENT DATA

parameter	symbol	min.	typ.	max.	unit
A.F.C. amplifier					
Inputs AFC+, AFC– (pins 3, 4)					
Transconductance for input voltages up to 1 V differential:					
AFCS1 AFCS2					
0 0	g_{00}	100	250	800	nA/V
0 1	g_{01}	15	25	35	μA/V
1 0	g_{10}	30	50	70	μA/V
1 1	g_{11}	60	100	140	μA/V
Tolerance of transconductance multiplying factor (2, 4 or 8) when correction-in-band is used	ΔM_g	–20	–	+20	%
Input offset voltage	V_{Ioff}	–75	–	+75	mV
Common mode input voltage	V_{com}	3	–	$V_{P1}-2,5$	V
Common mode rejection ratio	CMRR	–	50	–	dB
Power supply (V_{P1}) rejection ratio	PSRR	–	50	–	dB
Input current (P22 and P23 programmed HIGH)	I_I	–	–	500	nA
Tuning voltage amplifier					
Input TI, output TUN (pins 6, 8)					
Maximum output voltage at $I_{load} = \pm 2,5$ mA	V_{TUN}	$V_{P3}-1,6$	–	$V_{P3}-0,4$	V
Minimum output voltage at $I_{load} = \pm 2,5$ mA:					
VTMI1 VTMI0					
0 0	V_{TM00}	300	–	500	mV
1 0	V_{TM10}	450	–	650	mV
1 1	V_{TM11}	650	–	900	mV
Maximum output source current	$-I_{TUNH}$	2,5	–	8	mA
Maximum output sink current	I_{TUNL}	–	40	–	mA
Input bias current	I_{TI}	–5	–	+5	nA
Power supply (V_{P3}) rejection ratio	PSRR	–	60	–	dB

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Tuning voltage amplifier (continued)					
Minimum charge IT to tuning voltage amplifier					
TUHN1 TUHN0					
0 0	CH_{00}	0,4	1	1,7	μA μs
0 1	CH_{01}	4	8	14	μA μs
1 0	CH_{10}	15	30	48	μA μs
1 1	CH_{11}	130	250	370	μA μs
Tolerance of charge (or ΔV_{TUN}) multiplying factor when COIB and/or TUS are used	ΔCH	−20	–	+20	%
Maximum current I into tuning amplifier					
TUHN1 TUHN0					
0 0	I_{T00}	1,7	3,5	5,1	μA
0 1	I_{T01}	15	29	41	μA
1 0	I_{T10}	65	110	160	μA
1 1	I_{T11}	530	875	1220	μA
Correction-in-band					
Tolerance of correction-in-band levels 12 V, 18 V and 24 V	ΔV_{CIB}	−15	–	+15	%
Band-select output ports					
P10, P11, P12, P13 (pins 10 to 13)					
Output voltage HIGH at $-I_{OH}$ = 50 mA (note 3)	V_{OH}	V_{P2}−0,6	–	–	V
Output voltage LOW at I_{OL} = 2 mA	V_{OL}	–	–	0,4	V
Maximum output source current (note 3)	$-I_{OH}$	–	130	200	mA
Maximum output sink current	I_{OL}	–	5	–	mA
FDIV input (pin 15)					
Input voltage (peak-to-peak value) (t_{rise} and $t_{fall} \leqslant 40$ ns)	$V_{FDIV(p-p)}$	0,1	–	2	V
Duty cycle	–	40	–	60	%
Maximum input frequency	f_{max}	16	–	–	MHz
Input impedance	Z_i	–	8	–	kΩ
Input capacitance	C_i	–	5	–	pF

parameter	symbol	min.	typ.	max.	unit
OSC input (pin 24)					
Crystal resistance at resonance (4 MHz)	R_X	–	–	150	Ω
Power-down-reset					
Maximum supply voltage V_{P1} at which power-down-reset is active	V_{PD}	7,5	–	9,5	V
V_{P1} rise-time during power-up (up to V_{PD})	t_r	5	–	–	μs
Voltage level for valid module address					
Voltage level at P20 (pin 1) for valid module address as a function of MA1, MA0					
MA1 MA0					
0 0	V_{VA00}	−0,3	–	16	V
0 1	V_{VA01}	−0,3	–	0,8	V
1 0	V_{VA10}	2,5	–	$V_{P1}-2$	V
1 1	V_{VA11}	$V_{P1}-0,3$	–	V_{P1}	V

DEVELOPMENT DATA

Notes to the characteristics

1. For each band-select output which is programmed at logic 1, sourcing a current I_{OHP1X}, the additional supply currents (A) shown must be added to I_{P2} and I_{P3} respectively.
2. If $V_{P1} < 1$ V, the input current is limited to 10 μA at input voltages up to 16 V.
3. At continuous operation the output current should not exceed 50 mA. When the output is short-circuited to ground for several seconds the device may be damaged.
4. Values are proportional to V_{P1}.

I²C BUS TIMING (Fig. 8)

I²C bus load conditions are as follows:
4 kΩ pull-up resistor to +5 V; 200 pF capacitor to GND.

All values are referred to V_{IH} = 3 V and V_{IL} = 1,5 V.

parameter	symbol	min.	typ.	max.	unit
Bus free before start	t_{BUF}	4	–	–	μs
Start condition set-up time	$t_{SU,STA}$	4	–	–	μs
Start condition hold time	$t_{HD,STA}$	4	–	–	μs
SCL, SDA LOW period	t_{LOW}	4	–	–	μs
SCL HIGH period	t_{HIGH}	4	–	–	μs
SCL, SDA rise time	t_R	–	–	1	μs
SCL, SDA fall time	t_F	–	–	0,3	μs
Data set-up time (write)	$t_{SU,DAT}$	1	–	–	μs
Data hold time (write)	$t_{HD,DAT}$	1	–	–	μs
Acknowledge (from CITAC) set-up time	$t_{SU,CAC}$	–	–	2	μs
Acknowledge (from CITAC) hold time	$t_{HD,CAC}$	0	–	–	μs
Stop condition set-up time	$t_{SU,STO}$	4	–	–	μs
Data set-up time (read)	$t_{SU,RDA}$	–	–	2	μs
Data hold time (read)	$t_{HD,RDA}$	0	–	–	μs
Acknowledge (from master) set-up time	$t_{SU,MAC}$	1	–	–	μs
Acknowledge (from master) hold time	$t_{HD,MAC}$	2	–	–	μs

Note

Timings $t_{SU,DAT}$ and $t_{HD,DAT}$ deviate from the I²C bus specification .
After reset has been activated, transmission may only be started after a 50 μs delay.

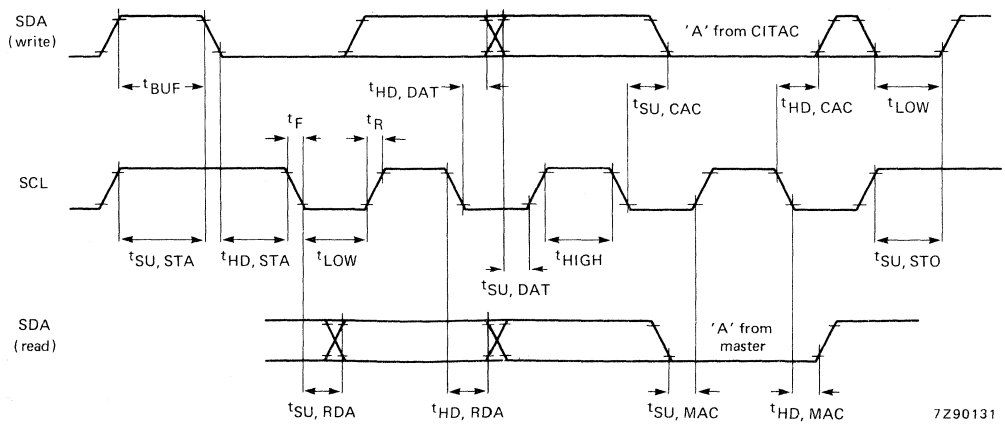


Fig. 8 I²C bus timing SAB3036.

COMPUTER INTERFACE FOR TUNING AND CONTROL (CITAC)

GENERAL DESCRIPTION

The SAB3037 provides closed-loop digital tuning of TV receivers, with or without a.f.c., as required. It also controls up to 4 analogue functions, 4 general purpose I/O ports and 4 high-current outputs for tuner band selection.

The IC is used in conjunction with a microcomputer from the MAB8400 family and is controlled via a two-wire, bidirectional I^2C bus.

Features

- Combined analogue and digital circuitry minimizes the number of additional interfacing components required
- Frequency measurement with resolution of 50 kHz
- Selectable prescaler divisor of 64 or 256
- 32 V tuning voltage amplifier
- 4 high-current outputs for direct band selection
- 4 static digital to analogue converters (DACs) for control of analogue functions
- Four general purpose input/output (I/O) ports
- Tuning with control of speed and direction
- Tuning with or without a.f.c.
- Single-pin, 4 MHz on-chip oscillator
- I^2C bus slave transceiver

QUICK REFERENCE DATA

Supply voltages			
(pin 13)	V_{P1}	typ.	12 V
(pin 19)	V_{P2}	typ.	13 V
(pin 14)	V_{P3}	typ.	32 V
Supply currents (no outputs loaded)			
(pin 13)	I_{P1}	typ.	30 mA
(pin 19)	I_{P2}	typ.	0,1 mA
(pin 14)	I_{P3}	typ.	0,6 mA
Total power dissipation	P_{tot}	typ.	380 mW
Operating ambient temperature range	T_{amb}	−20 to +70	°C

PACKAGE OUTLINE

24-lead DIL; plastic (SOT-101A).

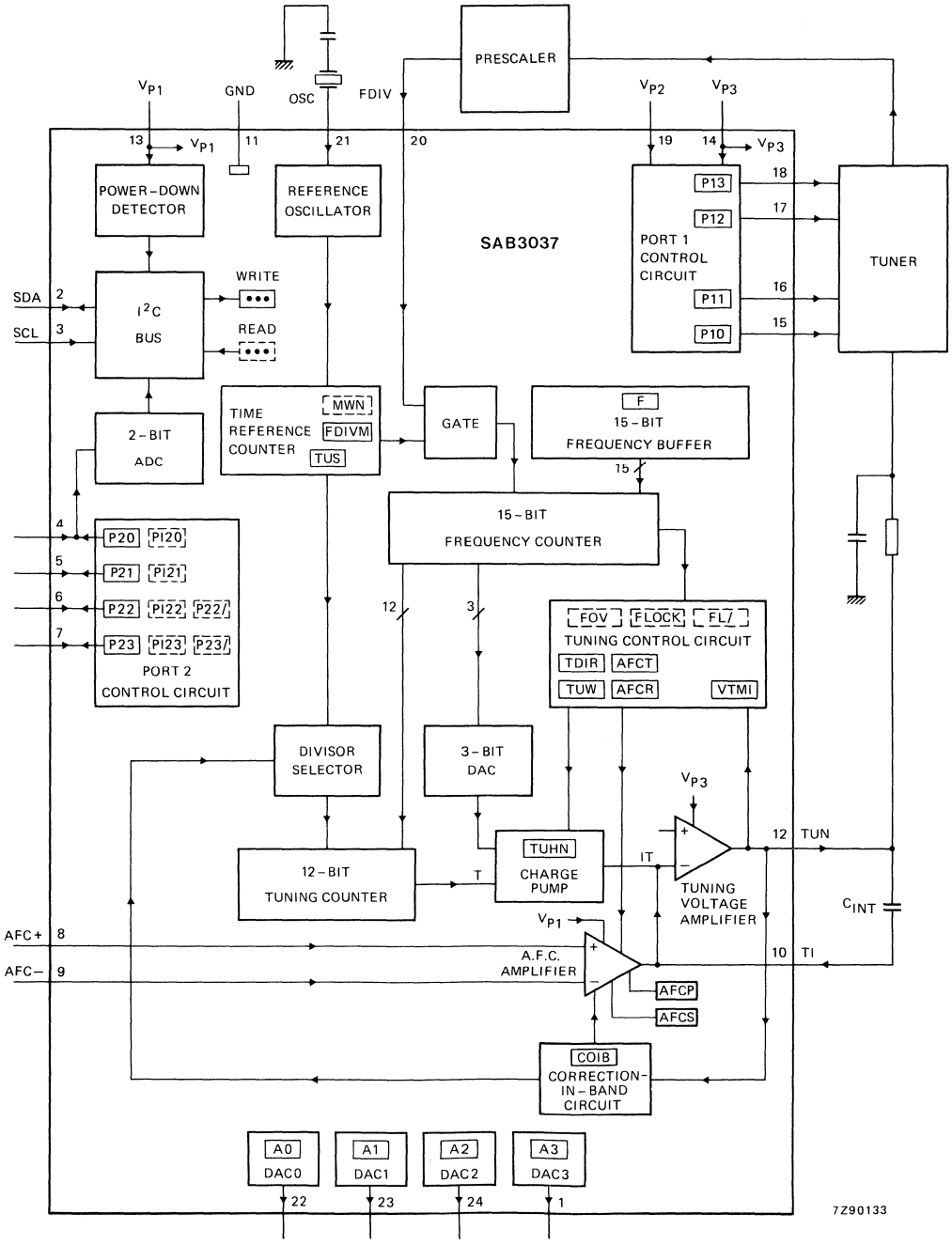


Fig. 1 Block diagram.

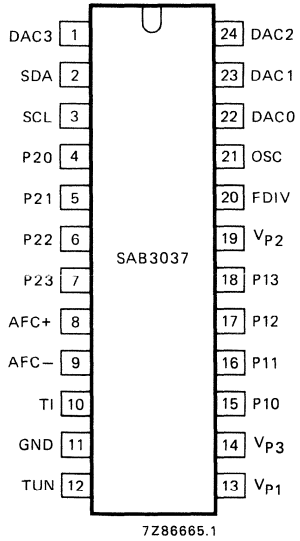


Fig. 2 Pinning diagram.

PINNING

1	DAC3	output of static DAC
2	SDA	serial data line (I²C bus)
3	SCL	serial clock line (I²C bus)
4	P20	general purpose input/output ports
5	P21	general purpose input/output ports
6	P22	general purpose input/output ports
7	P23	general purpose input/output ports
8	AFC+	a.f.c. inputs
9	AFC−	a.f.c. inputs
10	TI	tuning voltage amplifier inverting input
11	GND	ground
12	TUN	tuning voltage amplifier output
13	V_{P1}	+ 12 V supply voltage
14	V_{P3}	+ 32 V supply for tuning voltage amplifier
15	P10	high-current band-selection output ports
16	P11	high-current band-selection output ports
17	P12	high-current band-selection output ports
18	P13	high-current band-selection output ports
19	V_{P2}	positive supply for high-current band-selection output circuits
20	FDIV	input from prescaler
21	OSC	crystal oscillator input
22	DAC0	outputs of static DACs
23	DAC1	outputs of static DACs
24	DAC2	outputs of static DACs

DEVELOPMENT DATA

FUNCTIONAL DESCRIPTION

The SAB3037 is a monolithic computer interface which provides tuning and control functions and operates in conjunction with a microcomputer via an I^2C bus.

Tuning

This is performed using frequency-locked loop digital control. Data corresponding to the required tuner frequency is stored in a 15-bit frequency buffer. The actual tuner frequency, divided by a factor of 256 (or by 64) by a prescaler, is applied via a gate to a 15-bit frequency counter. This input (FDIV) is measured over a period controlled by a time reference counter and is compared with the contents of the frequency buffer. The result of the comparison is used to control the tuning voltage so that the tuner frequency equals the contents of the frequency buffer multiplied by 50 kHz within a programmable tuning window (TUW).

The system cycles over a period of 6,4 ms (or 2,56 ms), controlled by the time reference counter which is clocked by an on-chip 4 MHz reference oscillator. Regulation of the tuning voltage is performed by a charge pump frequency-locked loop system. The charge IT flowing into the tuning voltage amplifier is controlled by the tuning counter, 3-bit DAC and the charge pump circuit. The charge IT is linear with the frequency deviation Δf in steps of 50 kHz. For loop gain control, the relationship $\Delta IT/\Delta f$ is programmable. In the normal mode (when control bits TUHN0 and TUHN1 are both at logic 1, see OPERATION), the minimum charge IT at Δf = 50 kHz equals 250 μA μs (typical).

By programming the tuning sensitivity bits (TUS), the charge IT can be doubled up to 6 times. If correction-in-band (COIB) is programmed, the charge can be further doubled up to three times in relation to the tuning voltage level. From this, the maximum charge IT at Δf = 50 kHz equals $2^6 \times 2^3 \times 250$ μA μs (typical).

The maximum tuning current I is 875 μA (typical). In the tuning-hold (TUHN) mode (TUHN is active LOW), the tuning current I is reduced and as a consequence the charge into the tuning amplifier is also reduced.

An in-lock situation can be detected by reading FLOCK. When the tuner oscillator frequency is within the programmable tuning window (TUW), FLOCK is set to logic 1. If the frequency is also within the programmable a.f.c. hold range (AFCR), which always occurs if AFCR is wider than TUW, control bit AFCT can be set to logic 1. When set, digital tuning will be switched off, a.f.c. will be switched on and FLOCK will stay at logic 1 as long as the oscillator frequency is within AFCR. If the frequency of the tuning oscillator does not remain within AFCR, AFCT is cleared automatically and the system reverts to digital tuning. To be able to detect this situation, the occurrence of positive and negative transitions in the FLOCK signal can be read (FL/1N and FL/0N). AFCT can also be cleared by programming the AFCT bit to logic 0.

The a.f.c. has programmable polarity and transconductance; the latter can be doubled up to 3 times, depending on the tuning voltage level if correction-in-band is used.

The direction of tuning is programmable by using control bits TDIRD (tuning direction down) and TDIRU (tuning direction up). If a tuner enters a region in which oscillation stops, then, providing the prescaler remains stable, no FDIV signal is supplied to CITAC. In this situation the system will tune up, moving away from frequency lock-in. This situation is avoided by setting TDIRD which causes the system to tune down. In normal operation TDIRD must be cleared.

If a tuner stops oscillating and the prescaler becomes unstable by going into self-oscillation at a very high frequency, the system will react by tuning down, moving away from frequency lock-in. To overcome this, the system can be forced to tune up at the lowest sensitivity (TUS) value, by setting TDIRU.

Setting both TDIRD and TDIRU causes the digital tuning to be interrupted and a.f.c. to be switched on.

The minimum tuning voltage which can be generated during digital tuning is programmable by VTMI to prevent the tuner being driven into an unspecified low tuning voltage region.

Control

For tuner band selection there are four outputs P10 to P13 which are capable of sourcing up to 50 mA at a voltage drop of less than 600 mV with respect to the separate power supply input V_{P2}.

For additional digital control, four open collector I/O ports P20 to P23 are provided. Ports P22 and P23 are capable of detecting positive and negative transitions in their input signals. With the aid of port P20, up to three independent module addresses can be programmed.

Four 6-bit digital-to-analogue converters DAC0 to DAC3 are provided for analogue control.

Reset

CITAC goes into the power-down-reset mode when V_{P1} is below 8,5 V (typical). In this mode all registers are set to a defined state. Reset can also be programmed.

OPERATION

Write

CITAC is controlled via a bidirectional two-wire I^2C bus; the I^2C bus is specified in our data handbook "ICs for digital systems in radio, audio, and video equipment". For programming, a module address, R/$\overline{W}$ bit (logic 0), an instruction byte and a data/control byte are written into CITAC in the format shown in Fig. 3.

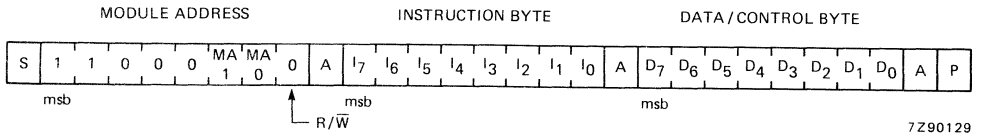


Fig. 3 I^2C bus write format.

The module address bits MA1, MA0 are used to give a 2-bit module address as a function of the voltage at port P20 as shown in Table 1.

Acknowledge (A) is generated by CITAC only when a valid address is received and the device is not in the power-down-reset mode ($V_{P1} > 8,5$ V (typical)).

Table 1 Valid module addresses

MA1	MA0	P20
0	0	don't care
0	1	GND
1	0	½V_{P1}
1	1	V_{P1}

OPERATION (continued)

Tuning

Tuning is controlled by the instruction and data/control bytes as shown in Fig. 4.

	INSTRUCTION BYTE								DATA/CONTROL BYTE							
	I_7	I_6	I_5	I_4	I_3	I_2	I_1	I_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
freq.	1	F14	F13	F12	F11	F10	F9	F8	F7	F6	F5	F4	F3	F2	F1	F0
TCD0	0	0	1	0	1	0	0	1	AFCT	VTMI0	AFCR1	AFCR0	TUHN1	TUHN0	TUW1	TUW0
TCD1	0	0	1	0	1	0	1	0	VTMI1	COIB1	COIB0	AFCS1	AFCS0	TUS2	TUS1	TUS0
TCD2	0	0	1	0	1	0	1	1	0	0	0	0	AFCP	FDIVM	TDIRD	TDIRU

7Z90125

Fig. 4 Tuning control format.

Frequency

Frequency is set when bit I_7 of the instruction byte is set to logic 1; the remainder of this byte together with the data/control byte are loaded into the frequency buffer. The frequency to which the tuner oscillator is regulated equals the decimal representation of the 15-bit word multiplied by 50 kHz. All frequency bits are set to logic 1 at reset.

Tuning hold

The TUHN bits are used to decrease the maximum tuning current and, as a consequence, the minimum charge IT (at Δf = 50 kHz) into the tuning amplifier.

Table 2 Tuning current control

TUHN1	TUHN0	typ. I_{max} μA	typ. IT_{min} $\mu A\ \mu s$	typ. ΔV_{TUNmin} at C_{INT} = 1 μF μV
0	0	3,5*	1*	1*
0	1	29	8	8
1	0	110	30	30
1	1	875	250	250

* Values after reset.

During tuning but before lock-in, the highest current value should be selected.
After lock-in the current may be reduced to decrease the tuning voltage ripple.

The lowest current value should not be used for tuning due to the input bias current of the tuning voltage amplifier (max. 5 nA). However it is good practice to program the lowest current value during tuner band switching.

Tuning sensitivity

To be able to program an optimum loop gain, the charge IT can be programmed by changing T using tuning sensitivity (TUS). Table 3 shows the minimum charge IT obtained by programming the TUS bits at Δf = 50 kHz; TUHN0 and TUHN1 = logic 1.

Table 3 Minimum charge IT as a function of TUS

Δf = 50 kHz; TUHN0 = logic 1; TUHN1 = logic 1

TUS2	TUS1	TUS0	typ. IT_{min} mA μs	typ. ΔV_{TUNmin} at C_{INT} = 1 μF mV
0	0	0	0,25*	0,25*
0	0	1	0,5	0,5
0	1	0	1	1
0	1	1	2	2
1	0	0	4	4
1	0	1	8	8
1	1	0	16	16

* Values after reset.

Correction-in-band

This control is used to correct the loop gain of the tuning system to reduce in-band variations due to a non-linear voltage/frequency characteristic of the tuner. Correction-in-band (COIB) controls the time T of the charge equation IT and takes into account the tuning voltage V_{TUN} to give charge multiplying factors as shown in Table 4.

DEVELOPMENT DATA

Table 4 Programming correction-in-band

COIB1	COIB0	charge multiplying factors at typical values of V_{TUN} at:			
		< 12 V	12 to 18 V	18 to 24 V	> 24 V
0	0	1*	1*	1*	1*
0	1	1	1	1	2
1	0	1	1	2	4
1	1	1	2	4	8

* Values after reset.

The transconductance multiplying factor of the a.f.c. amplifier is similar when COIB is used, except for the lowest transconductance which is not affected.

Tuning window

Digital tuning is interrupted and FLOCK is set to logic 1 (in-lock) when the absolute deviation $|\Delta f|$ between the tuner oscillator frequency and the programmed frequency is smaller than the programmed TUW value (see Table 5). If $|\Delta f|$ is up to 50 kHz above the values listed in Table 5, it is possible for the system to be locked depending on the phase relationship between FDIV and the reference counter.

Table 5 Tuning window programming

TUW1	TUW0	$\|\Delta f\|$ (kHz)	tuning window (kHz)
0	0	0*	0*
0	1	50	100
1	0	150	300

* Values after reset.

OPERATION (continued)

A.F.C.

When AFCT is set to logic 1 it will not be cleared and the a.f.c. will remain on as long as $|\Delta f|$ is less than the value programmed for the a.f.c. hold range AFCR (see Table 6). It is possible for the a.f.c. to remain on for values of up to 50 kHz more than the programmed value depending on the phase relationship between FDIV and the reference counter.

Table 6 A.F.C. hold range programming

AFCR1	AFCR0	$\|\Delta f\|$ (kHz)	a.f.c. hold range (kHz)
0	0	0*	0*
0	1	350	700
1	0	750	1500

* Values after reset.

Transconductance

The transconductance (g) of the a.f.c. amplifier is programmed via the a.f.c. sensitivity bits AFCS as shown in Table 7.

Table 7 Transconductance programming

AFCS1	AFCS0	typ. transconductance (μA/V)
0	0	0,25*
0	1	25
1	0	50
1	1	100

* Value after reset.

A.F.C. polarity

If a positive differential input voltage is applied to the (switched on) a.f.c. amplifier, the tuning voltage V_{TUN} falls when the a.f.c. polarity bit AFCP is at logic 0 (value after reset). At AFCP = logic 1, V_{TUN} rises.

Minimum tuning voltage

Both minimum tuning voltage control bits, VTMI1 and VTMI0, are at logic 0 after reset. Further details are given in CHARACTERISTICS.

Frequency measuring window

The frequency measuring window which is programmed must correspond with the division factor of the prescaler in use (see Table 8).

Table 8 Frequency measuring window programming

FDIVM	prescaler division factor	cycle period (ms)	measuring window (ms)
0	256	6,4*	5,12*
1	64	2,56	1,28

* Values after reset.

Tuning direction

Both tuning direction bits, TDIRU (up) and TDIRD (down), are at logic 0 after reset.

Control

The instruction bytes POD (port output data) and DACX (digital-to-analogue converter control) are shown in Fig. 5, together with the corresponding data/control bytes. Control is implemented as follows:

P13, P12, P11, P10 — Band select outputs. If a logic 1 is programmed on any of the POD bits D_3 to D_0, the relevant output goes HIGH. All outputs are LOW after reset.

P23, P22, P21, P20 — Open collector I/O ports. If a logic 0 is programmed on any of the POD bits D_7 to D_4, the relevant output is forced LOW. All outputs are at logic 1 after reset (high impedance state).

DACX — Digital-to-analogue converters. The digital-to-analogue converter selected corresponds to the decimal equivalent of the DACX bits X1, X0. The output voltage of the selected DAC is set by programming the bits AX5 to AX0; the lowest output voltage is programmed with all data AX5 to AX0 at logic 0, or after reset has been activated.

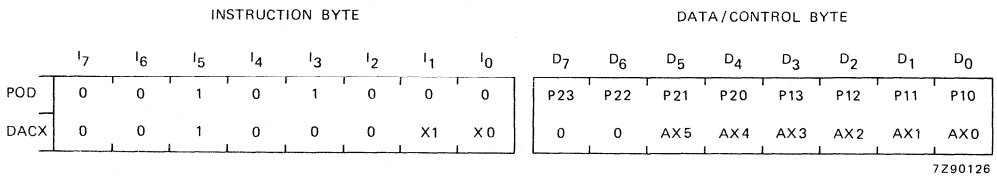


Fig. 5 Control programming.

Read

Information is read from CITAC when the R/$\overline{W}$ bit is set to logic 1. An acknowledge must be generated by the master after each data byte to allow transmission to continue. If no acknowledge is generated by the master the slave (CITAC) stops transmitting. The format of the information bytes is shown in Fig. 6.

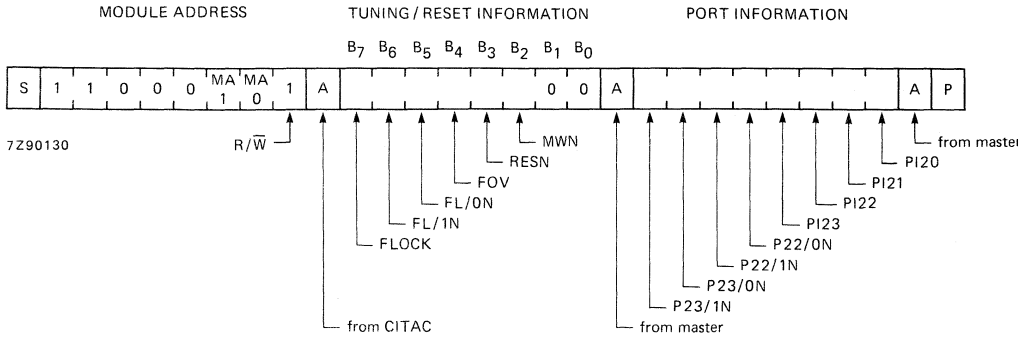


Fig. 6 Information byte format.

OPERATION (continued)

Tuning/reset information bits

FLOCK	Set to logic 1 when the tuning oscillator frequency is within the programmed tuning window.
FL/1N	Set to logic 0 (active LOW) when FLOCK changes from 0 to 1 and is reset to logic 1 automatically after tuning information has been read.
FL/0N	As for FL/1N but is set to logic 0 when FLOCK changes from 1 to 0.
FOV	Indicates frequency overflow. When the tuner oscillator frequency is too high with respect to the programmed frequency, FOV is at logic 1, and when too low, FOV is at logic 0. FOV is not valid when TDIRU and/or TDIRD are set to logic 1.
RESN	Set to logic 0 (active LOW) by a programmed reset or a power-down-reset. It is reset to logic 1 automatically after tuning/reset information has been read.
MWN	MWN (frequency measuring window, active LOW) is at logic 1 for a period of 1,28 ms, during which time the results of frequency measurement are processed. This time is independent of the cycle period. During the remaining time, MWN is at logic 0 and the received frequency is measured. When slightly different frequencies are programmed repeatedly and a.f.c. is switched on, the received frequency can be measured using FOV and FLOCK. To prevent the frequency counter and frequency buffer being loaded at the same time, frequency should be programmed only during the period of MWN = logic 0.

Port information bits

P23/1N, P22/1N	Set to logic 0 (active LOW) at a LOW-to-HIGH transition in the input voltage on P23 and P22 respectively. Both are reset to logic 1 after the port information has been read.
P23/0N, P22/0N	As for P23/1N and P22/1N but are set to logic 0 at a HIGH-to-LOW transition.
PI23, PI22, PI21, PI20	Indicate input voltage levels at P23, P22, P21 and P20 respectively. A logic 1 indicates a HIGH input level.

Reset

The programming to reset all registers is shown in Fig. 7. Reset is activated only at data byte HEX 06. Acknowledge is generated at every byte, provided that CITAC is not in the power-down-reset mode. After the general call address byte, transmission of more than one data byte is not allowed.

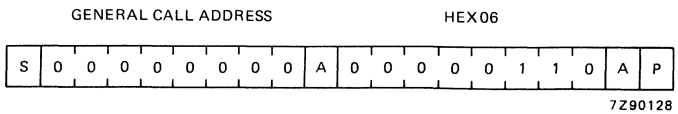


Fig. 7 Reset programming.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage ranges:			
(pin 13)	V_{P1}	−0,3 to +18	V
(pin 19)	V_{P2}	−0,3 to +18	V
(pin 14)	V_{P3}	−0,3 to +36	V
Input/output voltage ranges:			
(pin 2)	V_{SDA}	−0,3 to +18	V
(pin 3)	V_{SCL}	−0,3 to +18	V
(pins 4 to 7)	V_{P2X}	−0,3 to +18	V
(pins 8 and 9)	$V_{AFC+,AFC-}$	−0,3 to V_{P1}*	V
(pin 10)	V_{TI}	−0,3 to V_{P1}*	V
(pin 12)	V_{TUN}	−0,3 to V_{P3}*	V
(pins 15 to 18)	V_{P1X}	−0,3 to V_{P2}**	V
(pin 20)	V_{FDIV}	−0,3 to V_{P1}*	V
(pin 21)	V_{OSC}	−0,3 to +5	V
(pins 1 and 22 to 24)	V_{DACX}	−0,3 to V_{P1}*	V
Total power dissipation	P_{tot}	max. 1000	mW
Storage temperature range	T_{stg}	−55 to +125	°C
Operating ambient temperature range	T_{amb}	−20 to +70	°C

DEVELOPMENT DATA

* Pin voltage may exceed supply voltage if current is limited to 10 mA.

** Pin voltage must not exceed 18 V but may exceed V_{P2} if current is limited to 200 mA.

CHARACTERISTICS

T_{amb} = 25 °C; V_{P1}, V_{P2}, V_{P3} at typical voltages, unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply voltages	V_{P1}	10,5	12	13,5	V
	V_{P2}	4,7	13	16	V
	V_{P3}	30	32	35	V
Supply currents (no outputs loaded)	I_{P1}	18	30	45	mA
	I_{P2}	0	–	0,1	mA
	I_{P3}	0,2	0,6	2	mA
Additional supply currents (A)	I_{P2A}	−2	–	I_{OHP1X}	mA
(note 1)	I_{P3A}	0,2	–	2	mA
Total power dissipation	P_{tot}	–	380	–	mW
Operating ambient temperature	T_{amb}	−20	–	+70	°C
I²C bus inputs/outputs					
SDA input (pin 2); SCL input (pin 3)					
Input voltage HIGH (note 2)	V_{IH}	3	–	$V_{P1}-1$	V
Input voltage LOW	V_{IL}	−0,3	–	1,5	V
Input current HIGH (note 2)	I_{IH}	–	–	10	μA
Input current LOW (note 2)	I_{IL}	–	–	10	μA
SDA output (pin 2, open collector)					
Output voltage LOW at I_{OL} = 3 mA	V_{OL}	–	–	0,4	V
Maximum output sink current	I_{OL}	–	5	–	mA
Open collector I/O ports					
P20, P21, P22, P23 (pins 4 to 7, open collector)					
Input voltage HIGH	V_{IH}	2	–	16	V
Input voltage LOW	V_{IL}	−0,3	–	0,8	V
Input current HIGH	I_{IH}	–	–	25	μA
Input current LOW	$-I_{IL}$	–	–	25	μA
Output voltage LOW at I_{OL} = 2 mA	V_{OL}	–	–	0,4	V
Maximum output sink current	I_{OL}	–	4	–	mA

DEVELOPMENT DATA

parameter	symbol	min.	typ.	max.	unit
A.F.C. amplifier					
Inputs AFC+, AFC– (pins 8, 9)					
Transconductance for input voltages up to 1 V differential:					
AFCS1 AFCS2					
0 0	g_{00}	100	250	800	nA/V
0 1	g_{01}	15	25	35	μA/V
1 0	g_{10}	30	50	70	μA/V
1 1	g_{11}	60	100	140	μA/V
Tolerance of transconductance multiplying factor (2, 4 or 8) when correction-in-band is used	ΔM_g	–20	–	+20	%
Input offset voltage	V_{Ioff}	–75	–	+75	mV
Common mode input voltage	V_{com}	3	–	$V_{P1}-2,5$	V
Common mode rejection ratio	CMRR	–	50	–	dB
Power supply (V_{P1}) rejection ratio	PSRR	–	50	–	dB
Input current	I_I	–	–	500	nA
Tuning voltage amplifier					
Input TI, output TUN (pins 10, 12)					
Maximum output voltage at $I_{load} = \pm 2,5$ mA	V_{TUN}	$V_{P3}-1,6$	–	$V_{P3}-0,4$	V
Minimum output voltage at $I_{load} = \pm 2,5$ mA:					
VTMI1 VTMI0					
0 0	V_{TM00}	300	–	500	mV
1 0	V_{TM10}	450	–	650	mV
1 1	V_{TM11}	650	–	900	mV
Maximum output source current	$-I_{TUNH}$	2,5	–	8	mA
Maximum output sink current	I_{TUNL}	–	40	–	mA
Input bias current	I_{TI}	–5	–	+5	nA
Power supply (V_{P3}) rejection ratio	PSRR	–	60	–	dB

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Tuning voltage amplifier (continued)					
Minimum charge IT to tuning voltage amplifier					
TUHN1 TUHN0					
0 0	CH_{00}	0,4	1	1,7	μA μs
0 1	CH_{01}	4	8	14	μA μs
1 0	CH_{10}	15	30	48	μA μs
1 1	CH_{11}	130	250	370	μA μs
Tolerance of charge (or ΔV_{TUN}) multiplying factor when COIB and/or TUS are used	ΔCH	−20	–	+20	%
Maximum current i into tuning amplifier					
TUHN1 TUHN0					
0 0	I_{T00}	1,7	3,5	5,1	μA
0 1	I_{T01}	15	29	41	μA
1 0	I_{T10}	65	110	160	μA
1 1	I_{T11}	530	875	1220	μA
Correction-in-band					
Tolerance of correction-in-band levels 12 V, 18 V and 24 V	ΔV_{CIB}	−15	–	+15	%
Band-select output ports					
P10, P11, P12, P13 (pins 15 to 18)					
Output voltage HIGH at $-I_{OH}$ = 50 mA (note 3)	V_{OH}	V_{P2}−0,6	–	–	V
Output voltage LOW at I_{OL} = 2 mA	V_{OL}	–	–	0,4	V
Maximum output source current (note 3)	$-I_{OH}$	–	130	200	mA
Maximum output sink current	I_{OL}	–	5	–	mA
FDIV input (pin 20)					
Input voltage (peak-to-peak value) (t_{rise} and $t_{fall} \leqslant 40$ ns)	$V_{FDIV(p-p)}$	0,1	–	2	V
Duty cycle	–	40	–	60	%
Maximum input frequency	f_{max}	14,5	–	–	MHz
Input impedance	Z_i	–	8	–	kΩ
Input capacitance	C_i	–	5	–	pF

parameter	symbol	min.	typ.	max.	unit
OSC input (pin 21)					
Crystal resistance at resonance (4 MHz)	R_X	–	–	150	Ω
DAC outputs 0 to 3 (pins 22 to 24 and pin 1)					
Maximum output voltage (no load) at V_{P1} = 12 V (note 4)	V_{DH}	10	–	11,5	V
Minimum output voltage (no load) at V_{P1} = 12 V (note 4)	V_{DL}	0,1	–	1	V
Positive value of smallest step (1 least-significant bit)	ΔV_D	0	–	350	mV
Deviation from linearity	–	–	–	0,5	V
Output impedance at I_{load} = ± 2 mA	Z_o	–	–	70	Ω
Maximum output source current	$-I_{DH}$	–	–	6	mA
Maximum output sink current	I_{DL}	–	8	–	mA
Power-down-reset					
Maximum supply voltage V_{P1} at which power-down-reset is active	V_{PD}	7,5	–	9,5	V
V_{P1} rise-time during power-up (up to V_{PD})	t_r	5	–	–	μs
Voltage level for valid module address					
Voltage level at P20 (pin 4) for valid module address as a function of MA1, MA0					
MA1 MA0					
0 0	V_{VA00}	−0,3	–	16	V
0 1	V_{VA01}	−0,3	–	0,8	V
1 0	V_{VA10}	2,5	–	$V_{P1}-2$	V
1 1	V_{VA11}	$V_{P1}-0,3$	–	V_{P1}	V

DEVELOPMENT DATA

Notes to the characteristics

1. For each band-select output which is programmed at logic 1, sourcing a current I_{OHP1X}, the additional supply currents (A) shown must be added to I_{P2} and I_{P3} respectively.
2. If $V_{P1} < 1$ V, the input current is limited to 10 μA at input voltages up to 16 V.
3. At continuous operation the output current should not exceed 50 mA. When the output is short-circuited to ground for several seconds the device may be damaged.
4. Values are proportional to V_{P1}.

I²C BUS TIMING (Fig. 8)

I²C bus load conditions are as follows:
4 kΩ pull-up resistor to +5 V; 200 pF capacitor to GND.

All values are referred to V_{IH} = 3 V and V_{IL} = 1,5 V.

parameter	symbol	min.	typ.	max.	unit
Bus free before start	t_{BUF}	4	–	–	μs
Start condition set-up time	$t_{SU,STA}$	4	–	–	μs
Start condition hold time	$t_{HD,STA}$	4	–	–	μs
SCL, SDA LOW period	t_{LOW}	4	–	–	μs
SCL HIGH period	t_{HIGH}	4	–	–	μs
SCL, SDA rise time	t_R	–	–	1	μs
SCL, SDA fall time	t_F	–	–	0,3	μs
Data set-up time (write)	$t_{SU,DAT}$	1	–	–	μs
Data hold time (write)	$t_{HD,DAT}$	1	–	–	μs
Acknowledge (from CITAC) set-up time	$t_{SU,CAC}$	–	–	2	μs
Acknowledge (from CITAC) hold time	$t_{HD,CAC}$	0	–	–	μs
Stop condition set-up time	$t_{SU,STO}$	4	–	–	μs
Data set-up time (read)	$t_{SU,RDA}$	–	–	2	μs
Data hold time (read)	$t_{HD,RDA}$	0	–	–	μs
Acknowledge (from master) set-up time	$t_{SU,MAC}$	1	–	–	μs
Acknowledge (from master) hold time	$t_{HD,MAC}$	2	–	–	μs

Note

Timings $t_{SU,DAT}$ and $t_{HD,DAT}$ deviate from the I²C bus specification .
After reset has been activated, transmission may only be started after a 50 μs delay.

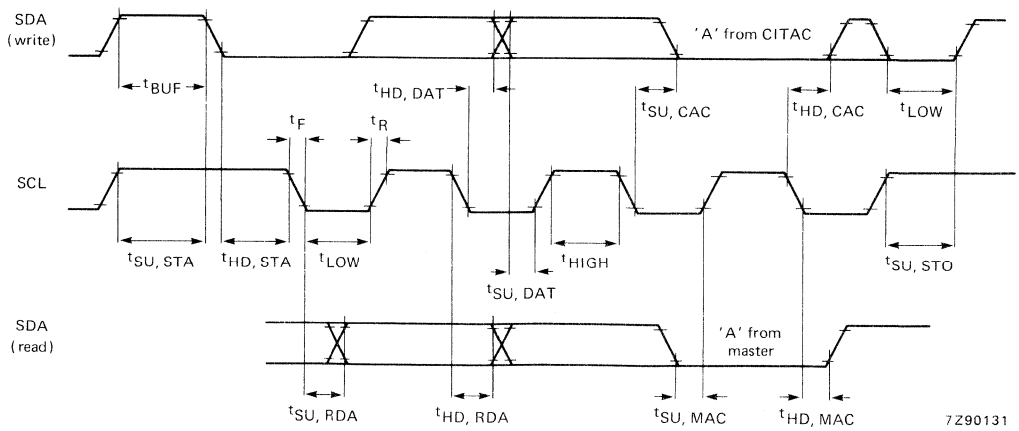


Fig. 8 I²C bus timing SAB3037.

DATA LINE DECODER

GENERAL DESCRIPTION

The SAF1135 is a data line decoder, designed in CMOS technology, which operates in conjunction with the data line processor (SAA5235) to form a data line receiver system.

This system receives and decodes binary data that is transmitted in line 16 of every first field of a standard television signal. The decoded information is accessed via the built-in I^2C bus interface. This information can be used to program a video tape recorder to start and stop the recording of a television program at the correct time, regardless of a delay or extension in the transmission time of the required television program.

Valid Video Programming System (VPS) data is transmitted in line 16 only. There is no VPS information in line 329.

The data transmission is biphase modulated and the bit transfer rate is 2,5 Mbit/s.

Features

- Field selection
- Line 16 decoding
- Start code check
- Biphase check
- Storage of data line information
- Generation of data reset pulse
- I^2C bus transmitter

QUICK REFERENCE DATA

parameter	symbol	min.	typ.	max.	unit
Supply voltage (pin 14)	V_{DD}	4,5	5,0	5,5	V
Supply current (pin 14)	I_{DD}	–	1	–	mA
Bit transfer rate at input DLD (pin 8)	BR_{DLD}	–	2,5	–	Mbits/s
Clock frequency at input DLCL (pin 11)	f_{DLCL}	–	5	–	MHz
Storage temperature range	T_{stg}	−65	–	+150	°C
Operating ambient temperature range	T_{amb}	0	–	70	°C

PACKAGE OUTLINES

14-lead DIL; plastic (SOT-27).

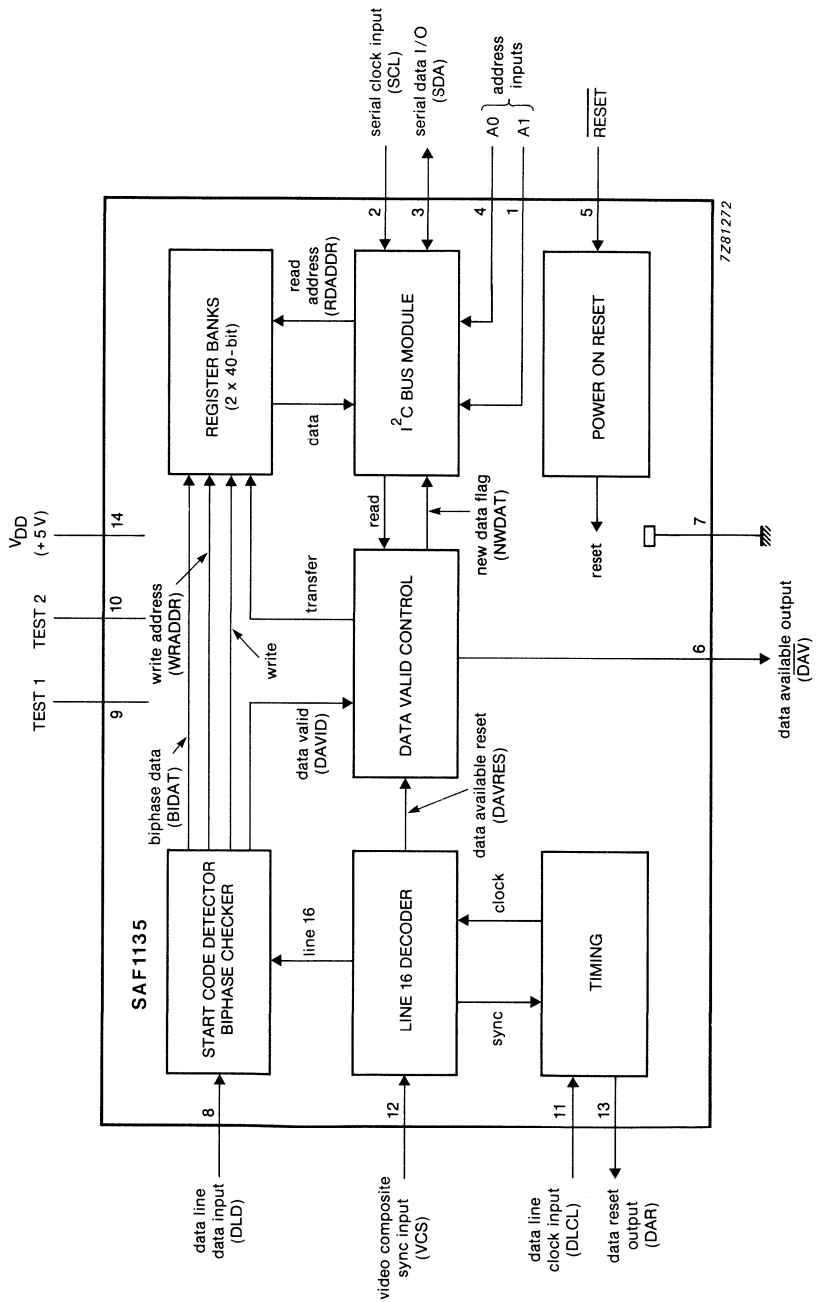


Fig. 1 Block diagram.

FUNCTIONAL DESCRIPTION

The SAF1135 is designed to receive and decode Video Tape Recorder (VTR) control information which is transmitted in line 16 of every first field of a standard television signal. The following description refers to the block diagram Fig. 1 unless otherwise stated.

Data line 16

The total information of data line 16 consists of fifteen 8-bit words. The contents of the information is shown in Fig. 2, a timing diagram of the data line in Fig. 3 and a survey of VTR control labels in Fig. 4.

From the total fifteen 8-bit words, the SAF1135 extracts words 5, 11, 12, 13 and 14. The contents of these words can be requested via the built-in I^2C bus interface (see Fig. 9). The circuit is fully transparent, thus each bit is transferred without modification. Only the sequence of the words is changed; words 11 to 14 being transmitted first followed by word 5.

By evaluation of the Video Composite Sync (VCS) signal at pin 12 the SAF1135 identifies the beginning of line 16 in the first field. The line 16 decoder stage releases the start code detector. When a correct start code is detected (for timing of start code detection, see Fig. 5) words 5 and 11 to 14 are decoded, checked for biphase errors and stored in register bank R (Receive). If no biphase error has occurred, the contents of register bank R are transferred to register bank T (Transmit) by the data valid control signal (DAVID). If the system has been addressed, this transfer is delayed until the next start or stop condition of the I^2C bus has been received.

The last correct data line information remains available until it is read via the I^2C bus. After it is read once the stored information is no longer considered to be valid, the internal new data flag (NWDAT) is reset and if the circuit is addressed, the only VPS data sent back is "FFF...F". The same conditions apply after power-up. Then no data can be read out.

New data is available after reception of another error-free line 16.

Power-on Reset

Reset pulses applied externally to pin 5 ($\overline{\text{RESET}}$; active LOW) are latched internally by the power-on reset circuit.

$\overline{\text{RESET}}$ = LOW influences:

- I^2C bus logic to no acknowledge
- NWDAT flag and internal timing to reset
- Data available output ($\overline{\text{DAV}}$; active LOW) at pin 6 forced to LOW
- Data reset output (DAR) at pin 13 forced to HIGH
- Serial data (SDA) input/output at pin 3 released

When $\overline{\text{RESET}}$ changes to HIGH the reset period is terminated with the next negative-going transition of the data line clock (DLCL) input at pin 11. Then, the data available ($\overline{\text{DAV}}$) output at pin 6 will go HIGH.

When an external reset is not used pin 5 is connected to V_{DD}. If an external reset is required, the rise time (t_r) of $\overline{\text{RESET}}$ voltage must be greater than 50 μs. An external 10 kΩ resistor connected between pin 5 and V_{DD} and an external 2,7 nF capacitor connected to V_{SS} will result in $t_r \geqslant 50$ μs.

DEVELOPMENT DATA

FUNCTIONAL DESCRIPTION (continued)

Word	Content
1	Run in
2	Start code
3	Program source identification (binary coded)
4	Program source identification (ASCII sequential)
5	Sound and VTR control information
6	Program/Test picture identification
7	Internal information exchange
8	Address assignment of signal distribution
9	
10	Messages/Commands
11	VTR Control Information
12	
13	
14	
15	Reserve

Fig. 2 Total information of data line 16.

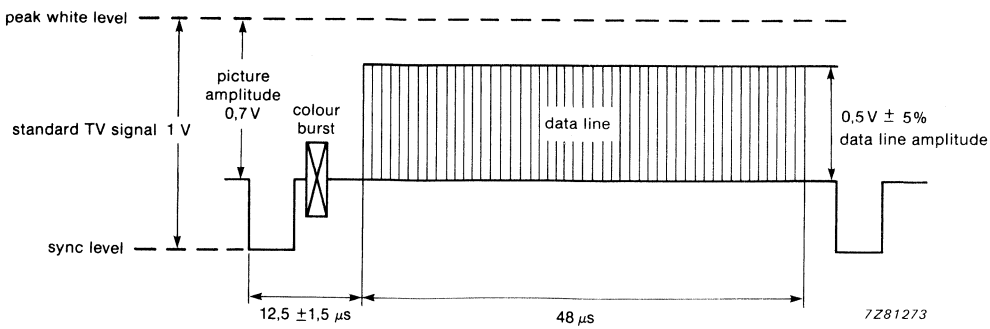


Fig. 3 Timing diagram of data line 16; modulation depth 71,4%.

VTR Control Information

Word-no.	5								11								12								13								14							
Bit-no.	1	2	3	4	5	6	7	8	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
Label binary	Bit 1	Bit 2	Status						Address range	Day							Month				Hour				Minute								Nation							Program Source	
	0	0	2-Channel						Special System Code																															
	0	1	Mono																																					
	1	0	Stereo																																					
	1	1	2-Channel																																					
System Status Code									1	X	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	NC	. .	NC	PC	. . . .	PC		
	Bit 3	Bit 4																																					
Pause Code	1	0	not for children						1	X	0	0	0	0	0	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	NC	. .	NC	PC	. . . .	PC		
Interrupt Code	0	1	free						1	X	0	0	0	0	0	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	NC	. .	NC	PC	. . . .	PC		

Where:

X = 0 or 1 (bit)
NC is the Nation Code
PC is the Program Source Code

Fig. 4 VTR control information of data line 16.

DEVELOPMENT DATA

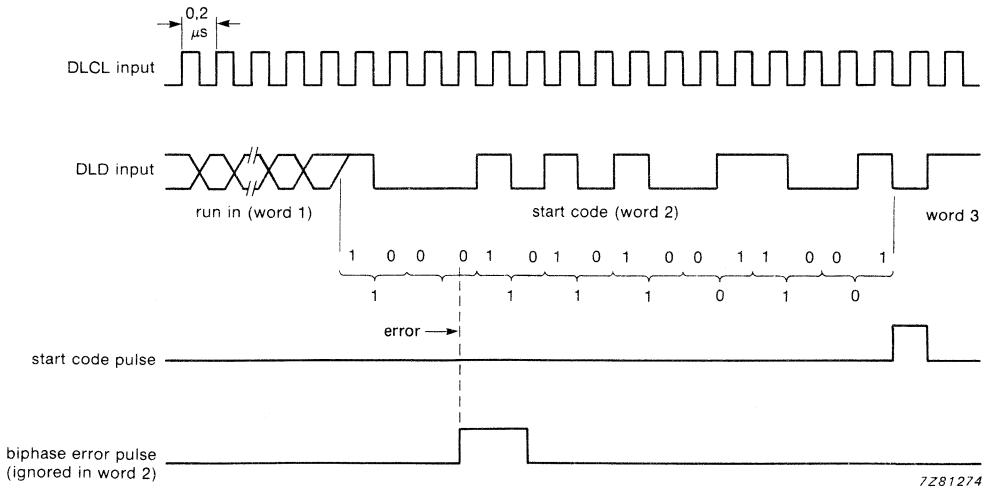


Fig. 5 Timing diagram of start code detection.

FUNCTIONAL DESCRIPTION (continued)

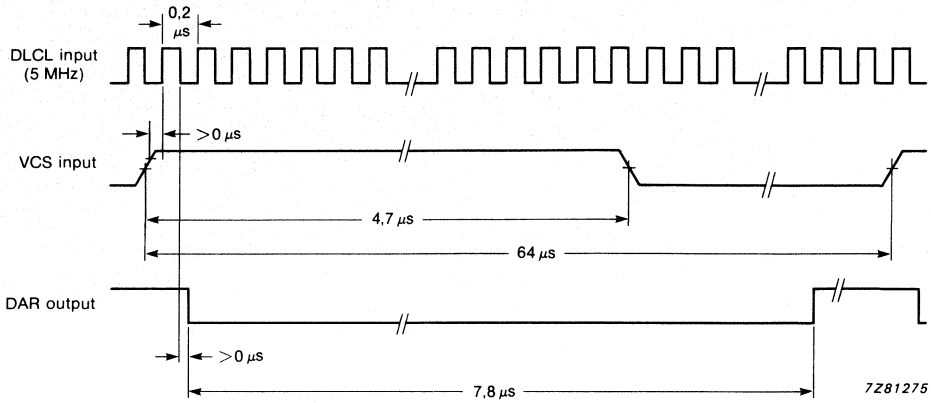


Fig. 6 Timing diagram of the data reset pulse generation.

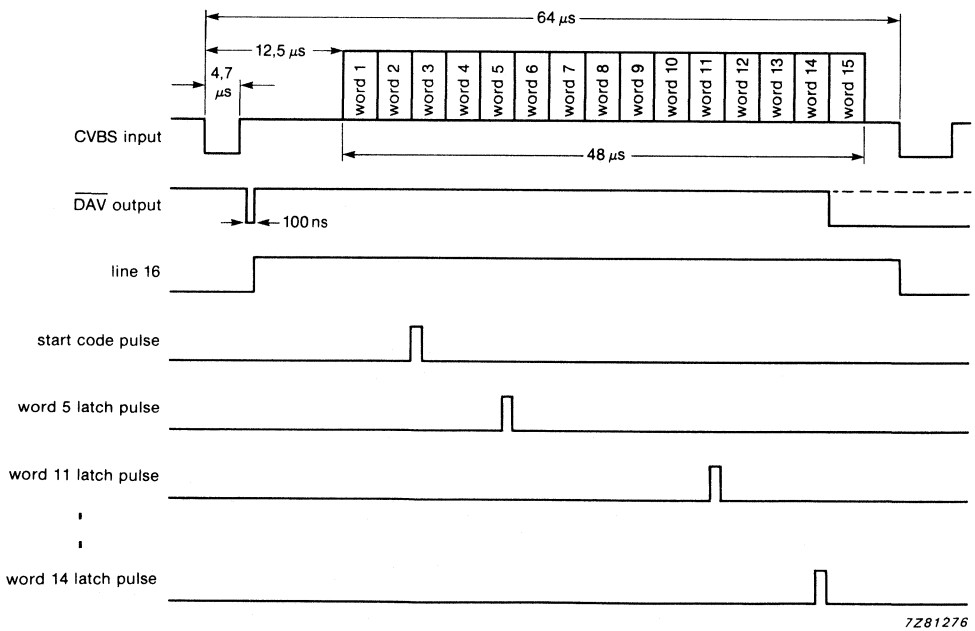


Fig. 7 Timing diagram of the data available output and word latch pulses.

Data line data and clock inputs (DLD; DLCL)

The data line data and clock signals from the SAA5235 are input at pins 8 and 11 respectively. The data transmission is biphase modulated, the bit transfer rate is 2,5 Mbit/s and the clock frequency is 5 MHz.

Input DLD incorporates an internal active clamping circuit. DLCL is internally a.c. coupled.

Video composite sync input (VCS)

The VCS input pulse at pin 12 is used for:

- Generation of the data reset pulse (DAR)
- Identification of the first field
- Selection of line 16

The timing of the data reset pulse generation is shown in Fig. 6.

I^2C bus address inputs (A0; A1)

The two I^2C address inputs at pins 4 and 1 respectively, provide the four different addresses 20H, 22H, 24H and 26H.

Data reset output (DAR)

The DAR output at pin 13 is a line frequency pulse with a 0,88 duty factor derived from the VCS pulse. The DAR pulse is fed to the SAA5235 to reset the data slicer circuit and the clock phase detector circuit.

Data available output ($\overline{DAV}$)

The $\overline{DAV}$ active LOW output at pin 6 is set to LOW after reception of one error-free data line 16. $\overline{DAV}$ returns to HIGH after at the beginning of the next first field.

If no valid data is available $\overline{DAV}$ remains HIGH. However, a short duration (100 ns) pulse inserted at the beginning of line 16 ensures that a HIGH-to-LOW transition occurs, which can be used for triggering.

The timing of $\overline{DAV}$ output and word latch pulses is shown in Fig. 7.

I^2C bus

The internally latched data from words 5 and 11 to 14 can be clocked out via the I^2C interface by a bus master. The lines are the serial clock input (SCL) at pin 2 and the serial data input/output (SDA) at pin 3.

The SAF1135 can operate only as a slave transmitter on the bus.
Data format is shown in Fig. 8.

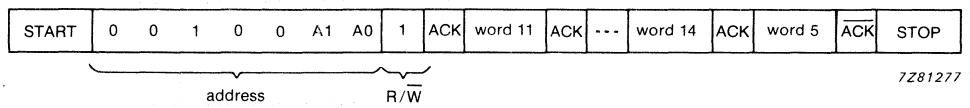


Fig. 8 I^2C bus data format.

- The MSB of each word is transmitted first.
- There is no restriction on the number of words to be transmitted, but if more than five words are requested, word 5 will be repeated.
- Noise pulses less than 200 ns duration are ignored on the bus lines.

DEVELOPMENT DATA

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range (pin 14)	V_{DD}		−0,5 to +7,0	V
Supply current (pin 14)	I_{DD}	max.	20	mA
Supply current (pin 7)	I_{SS}	max.	20	mA
Input voltage (pins 8 and 11)	V_I		−0,5 to +12	V
Input voltage on all other pins	V_I		−0,5 to V_{DD} +0,5*	V
Input current	$\pm I_I$	max.	10	mA
Output current	$\pm I_O$	max.	10	mA
Power dissipation per package**	P_{tot}	max.	400	mW
Power dissipation per output	P	max.	100	mW
Storage temperature range	T_{stg}		−65 to +150	°C
Operating ambient temperature range	T_{amb}		0 to +70	°C

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see 'Handling MOS devices').

* V_{DD} +0,5 not to exceed 7,0 V.
** Above +60 °C: derate linearly with 8 mW/K.

DEVELOPMENT DATA

D.C. CHARACTERISTICS

V_{DD} = 5 V ± 10%; T_{amb} = 0 to 70 °C; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply (pin 14)						
Supply voltage	–	V_{DD}	4,5	5	5,5	V
Supply current	Quiescent at 25 °C All inputs at V_{DD} or V_{SS} $\overline{RESET}$ at V_{SS} TEST 1 and TEST 2 at V_{DD} I_O = 0 mA	I_{DD}	–	–	10	μA
	During normal operation (without LED at $\overline{DAV}$, V_{DD} = 5 V)	I_{DD}	–	1	–	mA
Inputs						
A0, A1, TEST 1, TEST 2, SCL						
Input voltage LOW		V_{IL}	–	–	0,2V_{DD}	V
Input voltage HIGH		V_{IH}	0,7V_{DD}	–	–	V
Leakage current		I_{LI}	–	–	1	μA
DLCL						
Input voltage	Clock internally a.c. coupled	V_I	–	–	12	V
Leakage current	V_I = 0 to 10 V	I_{LI}	–	–	10	μA
$\overline{RESET}$	During normal operation pin 5 connected to V_{DD}					
Input voltage LOW		V_{IL}	–	–	0,3V_{DD}	V
Input voltage HIGH		V_{IH}	0,9V_{DD}	–	–	V
Input current HIGH		I_{IH}	–	–	15	μA
Leakage current		I_{LI}	–	–	10	μA
VCS						
Input voltage LOW		V_{IL}	–	–	0,8	V
Input voltage HIGH		V_{IH}	2,0	–	–	V
Leakage current		I_{LI}	–	–	1	μA

D.C. CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Inputs/Outputs						
DLD	Internal active clamping circuit, open drain output					
Input voltage LOW		V_{IL}	–	–	0,9	V
Input voltage HIGH		V_{IH}	2,0	–	12	V
Leakage current		I_{LI}	–	–	1	μA
Output voltage LOW	I_{OL} = 4 mA	V_{OL}	–	–	0,4	V
SDA	open drain output					
Input voltage LOW		V_{IL}	–	–	0,9	V
Input voltage HIGH		V_{IH}	3,15	–	–	V
Leakage current	V_{DD} = 6 V; V_I = 0 or V_{DD}	I_{LI}	–	–	6	μA
Output voltage LOW	I_{OL} = 4 mA	V_{OL}	–	–	0,4	V
Outputs						
DAR						
Output voltage LOW	I_{OL} = 1 mA	V_{OL}	–	–	0,4	V
Output voltage HIGH	$-I_{OH}$ = 400 μA	V_{OH}	V_{DD}–0,5 V	–	–	V
$\overline{DAV}$						
Output voltage LOW	I_{OL} = 10 mA	V_{OL}	–	–	1,0	V
Output voltage HIGH	$-I_{OH}$ = 400 μA	V_{OH}	V_{DD}–0,5 V	–	–	V

DEVELOPMENT DATA

A.C. CHARACTERISTICS

V_{DD} = 5 V ± 10%; T_{amb} = 0 to 70 °C; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Inputs						
Input capacitance		C_I	–	–	10	pF
A0, A1, TEST 1, TEST 2, SCL						
Rise time	$V_{IL(max)}$ to $V_{IH(min)}$	t_r	50	–	–	µs
DLCL						
Clock frequency	sinusoidal input signal	f_{DLCL}	–	5	–	MHz
Input voltage	peak-to-peak value	$V_{I(p-p)}$	1	–	–	V
DLD						
Coupling capacitor		C_{EXT}	—	1	4,7	nF
Set-up time	relative to rising edge of DLCL	t_{SU}	40	–	–	ns
Hold-up time	relative to rising edge of DLCL	t_{HD}	40	–	–	ns
Outputs						
DAR, $\overline{DAV}$						
Rise and fall times	C_L = 50 pF	t_r, t_f	–	–	50	ns
DAR-time LOW		$t_{DAR,L}$	–	7,8	–	µs
SDA						
Fall time	C_L = 400 pF	t_f	–	–	300	ns
I^2C bus - Input/Output						
	For both SDA and SCL valid					
Input current HIGH	0,9 V_{DD}, including I_{LI} of possible output stage	I_{IH}	–	–	10	µA
Input capacitance		C_I	–	–	10	pF
Rise time		t_r	–	–	1	µs
Fall time		t_f	–	–	0,3	µs
Clock frequency		f_{CL}	–	–	100	kHz
Pulse duration LOW		t_{LOW}	4,7	–	–	µs
Pulse duration HIGH		t_{HIGH}	4,0	–	–	µs

APPLICATION INFORMATION

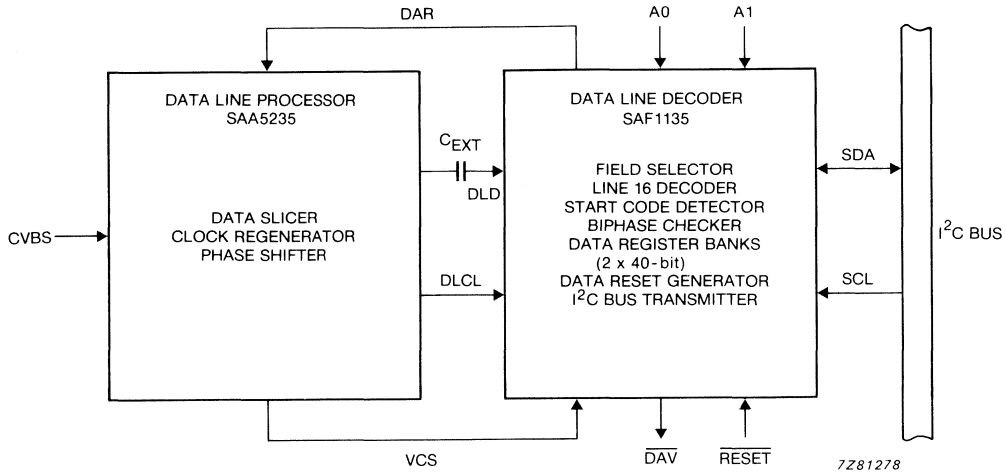


Fig. 9 Data line receiver.

COMPUTER INTERFACED PRESCALER-SYNTHESIZER

GENERAL DESCRIPTION

The TDA8400 provides closed-loop digital tuning of TV receivers, with or without a.f.c., as required. It comprises a 1,1 GHz prescaler, with the divide-by-64 ratio, which drives a tuning interface providing a tuning voltage of 33 V (max.) via an external output transistor. The TDA8400 can also drive external p-n-p transistors to provide 4 high-current outputs for tuner band selection.

The IC is used in conjunction with a microcomputer from the MAB8400 family and is controlled via a two-wire, bidirectional I^2C bus.

Features

- Combined analogue and digital circuitry minimizes the number of additional interfacing components required
- Frequency measurement with resolution of 50 kHz
- On-chip prescaler divisor of 64
- 33 V tuning voltage amplifier
- 4 high-current outputs for direct band selection
- Tuning with control of speed
- Tuning with or without a.f.c.
- Single-pin, 4 MHz on-chip oscillator
- I^2C bus slave transceiver

QUICK REFERENCE DATA

Supply voltages			
(pin 10)	V_{CCS}	typ.	5 V
(pin 15)	V_{CCP}	typ.	5 V
Supply currents			
(pin 10)	I_{CCS}	typ.	12 mA
(pin 15)	I_{CCP}	typ.	43 mA
Power dissipation	P_{tot}	typ.	275 mW
Operating ambient temperature range	T_{amb}		0 to + 70 °C

PACKAGE OUTLINE

18-lead DIL; plastic (SOT-102H).

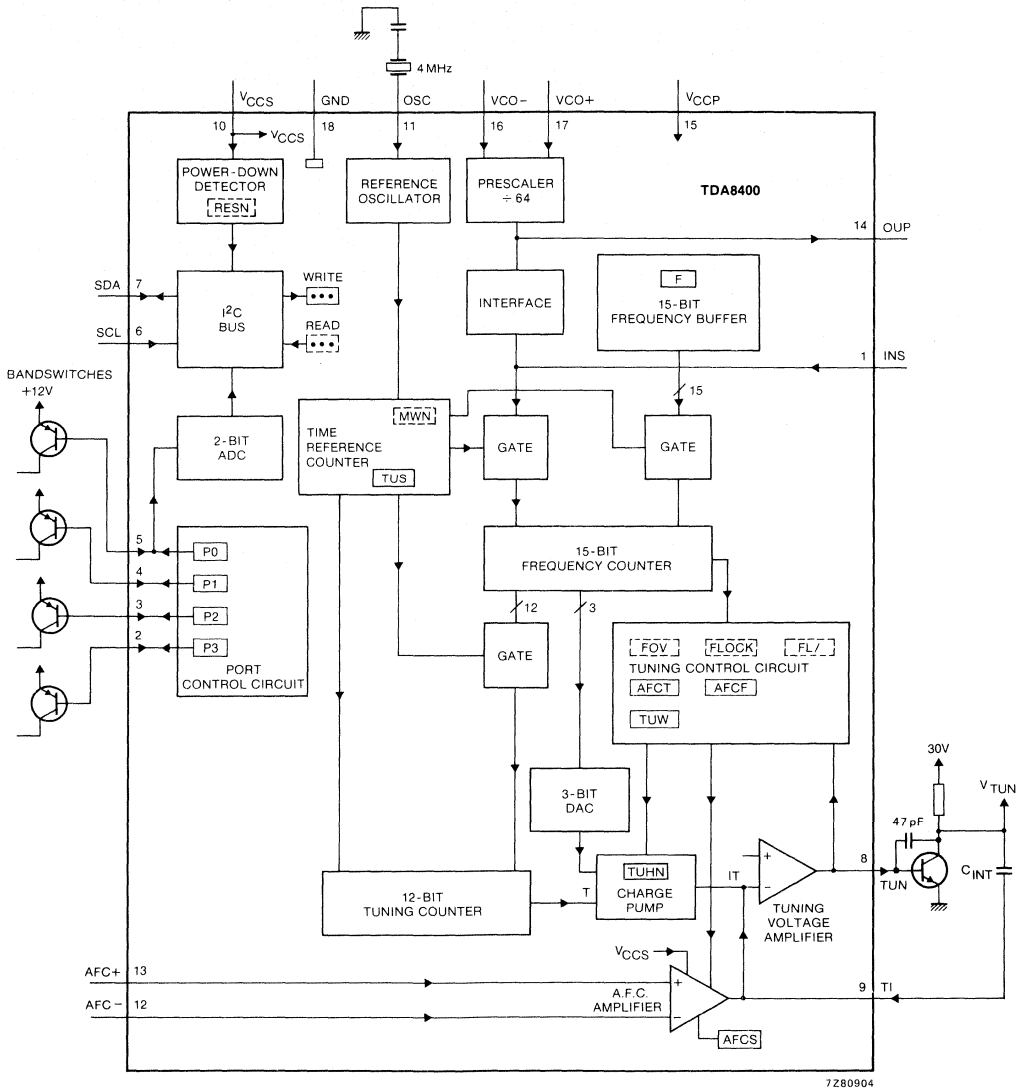


Fig. 1 Block diagram.

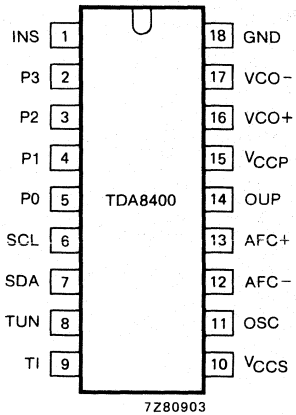


Fig. 2 Pinning diagram.

PINNING

1	INS	input synthesizer (test) *
2	P3	high-current band-selection output ports
3	P2	
4	P1	
5	P0	
6	SCL	serial clock line (I²C bus)
7	SDA	serial data line (I²C bus)
8	TUN	tuning voltage amplifier output
9	TI	tuning voltage amplifier inverting input
10	V_{CCS}	+ 5 V supply voltage (synthesizer)
11	OSC	crystal oscillator input
12	AFC−	a.f.c. amplifier inputs
13	AFC+	
14	OUP	output from prescaler (test)
15	V_{CCP}	+ 5 V supply voltage (prescaler) **
16	VCO+	inputs to prescaler
17	VCO−	
18	GND	ground

DEVELOPMENT DATA

* Connected to ground for application.
** Left open-circuit for application.

FUNCTIONAL DESCRIPTION

Prescaler

The integrated prescaler has a divide-by-64 ratio with a maximum input frequency of 1,1 GHz. It will oscillate in the absence of an input signal within the frequency range of 800 MHz to 1,1 GHz.

Tuning

This is performed using frequency-locked loop digital control. Data corresponding to the required tuner frequency is stored in the 15-bit frequency buffer. The actual tuner frequency (1,1 GHz max.) is applied to the circuit on the two complementary inputs VCO+ and VCO– which drive the integrated prescaler. The resulting frequency (FDIV) is measured over a period controlled by a time reference counter and fed via a gate to a 15-bit frequency counter where it is compared to the contents of the frequency buffer. The result of the comparison is used to control the tuning voltage so that the tuner frequency equals the contents of the frequency buffer multiplied by 50 kHz within a programmable tuning window (TUW).

The system cycles over a period of 2,56 ms, controlled by the time reference counter which is clocked by an on-chip 4 MHz reference oscillator. Regulation of the tuning voltage is performed by a charge pump frequency-locked loop system. The charge IT flowing into the tuning voltage amplifier (external capacitance C_{INT} = 0,5 μF) is controlled by the tuning counter, 3-bit DAC and the charge pump circuit. The charge IT is linear with the frequency deviation Δf in steps of 50 kHz. For loop gain control, the relationship $\Delta IT/\Delta f$ is programmable. In the normal mode (control bit TUHN = logic 1; see Table 2) the minimum charge IT at Δf = 50 kHz equals 125 $\mu A \cdot \mu s$ (typ.).

By programming the tuning sensitivity bits (TUS; see Table 3) the charge IT can be doubled up to 6 times. From this, the maximum charge IT at Δf = 50 kHz equals 2^6 x 125 $\mu A \cdot \mu s$ (typ.). The maximum tuning current I is 440 μA, while T is limited to the duration of the tuning cycle (2,56 ms).

In the tuning-hold mode (TUHN = logic 0) the tuning current I is reduced and as a consequence the charge into the tuning amplifier is also reduced. An in-lock situation can be detected by reading FLOCK. The TDA8400 can be programmed to tune in the digital mode or the AFC mode by setting AFCF. In the digital mode (AFCF = logic 0), the tuning window is programmable through the TUW flag. When the tuner oscillator frequency is within the programmable tuning window (TUW), FLOCK is set to logic 1.

In the AFC mode, FLOCK will remain at logic 1 provided the tuner frequency is within a ± 800 kHz hold range. Switching from digital mode to AFC mode is determined by the microcontroller (AFCF flag). Switching from AFC mode to digital mode can be determined by the microcontroller, but if the frequency of the tuning oscillator does not remain within the hold range, the system automatically reverts to digital tuning. Switching back to the AFC mode will then have to be effected externally again. The tuning mode can be checked by reading the AFCT flag.

The occurance of positive and negative transitions in the FLOCK signal can be read by FL/1N and FL/0N. The AFC amplifier has programmable transconductance to 2 pre-defined values.

Control

For tuner band selection there are four output ports P0 to P3 which are capable of driving external p-n-p transistors (open collector) as current sources. Output port P0 can also be used as valid address input with an active level determined by module address bits MA0 and MA1.

Reset

The TDA8400 goes into the power-down-reset mode when V_{P1} is below 3 V (typ.). In this mode all registers are set to a defined state.

OPERATION

Write

The TDA8400 is controlled via a bidirectional two-wire I²C bus; additional information on the I²C bus is available on request.

For programming, a module address, R/$\overline{W}$ bit (logic 0), an instruction byte and a data/control byte are written into the device in the format shown in Fig. 3.

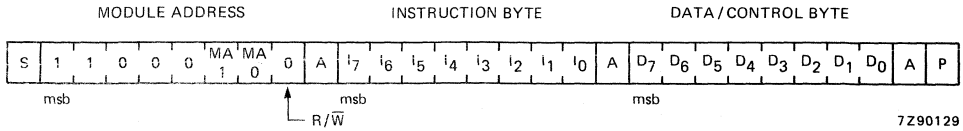


Fig. 3 I²C bus write format.

The module address bits MA1, MA0 are used to give a 2-bit module address as a function of the voltage at port input P0 as shown in Table 1.

Acknowledge (A) is generated by the TDA8400 only when a valid address is received and the device is not in the power-down-reset mode.

DEVELOPMENT DATA

Table 1 Valid module addresses

P0	MA1	MA0
don't care	0	0
GND	0	1
½V_{CCS}	1	0
V_{CCS}	1	1

Tuning

Tuning is controlled by the instruction and data/control bytes as shown in Fig. 4.

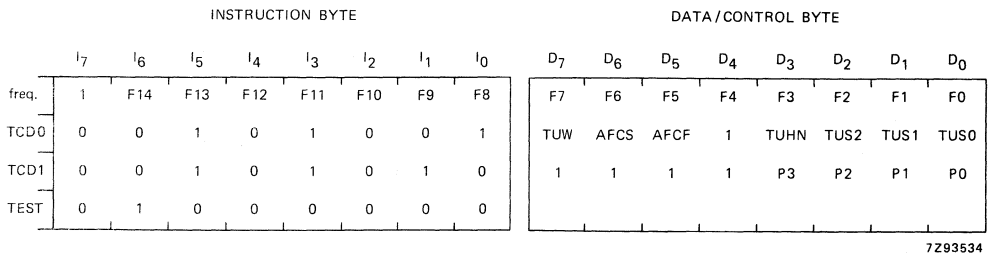


Fig. 4 Tuning control format.

Frequency

Frequency is set when bit I_7 of the instruction byte is set to logic 1; the remaining bits of this byte are processed as being data. Instruction bytes are fully decoded. All frequency bits are set to logic 1 and control bits to logic 0 at reset. The test instruction byte cannot be used for any other purpose.

OPERATION (continued)

Tuning hold

The TUHN bit is used to decrease the maximum tuning current (I) and, as a consequence, the minimum charge IT (at $\Delta f = 50$ kHz) into the tuning amplifier.

Table 2 Tuning current control

TUHN	typ. I_{max} (μA)	typ. IT_{min} ($\mu A \cdot \mu s$)
0	18*	5*
1	440	125

Tuning sensitivity

To be able to program an optimum loop gain, the charge IT can be programmed by changing T using tuning sensitivity (TUS). Table 3 shows the minimum charge IT obtained by programming the TUS bits at $\Delta f = 50$ kHz; TUHN = logic 1.

Table 3 Minimum charge IT as a function of TUS

TUS2	TUS1	TUS0	typ. IT_{min} ($\mu A \cdot \mu s$)
0	0	0	0,125
0	0	1	0,25
0	1	0	0,5
0	1	1	1
1	0	0	2
1	0	1	4
1	1	0	8

The minimum tuning pulse is 2 μs.

Tuning mode

AFCF determines whether the TDA8400 has to tune in the digital mode or the AFC mode as shown in Table 4.

Table 4 Selection of tuning mode as a function of AFCF

AFCF	tuning mode
0	digital
1	AFC

If the tuner oscillator frequency comes out of the hold range when in the AFC mode, the device will automatically switch to digital tuning and AFCF is reset to logic 0.

* Values after reset.

Tuning window

In the digital tuning mode TUW determines the tuning window (see Table 5) and the device is said to be in the "in-lock" situation.

Table 5 Tuning window programming

TUW	tuning window (kHz)
0	0
1	± 200

Transconductance

The transconductance (g) of the AFC amplifier is programmed via the AFC sensitivity bit AFCS as shown in Table 6.

Table 6 Transconductance programming

AFCS	typ. transconductance (μA/V)
1	10
0	50

Band-selection control ports (PX)

For band-selection control there are four output ports P0 to P3 which are capable of driving external p-n-p transistors (open collector) as current sources. If a logic 1 is programmed on any of the PX bits P0 to P3, the p-n-p transistor will conduct and the relevant output goes LOW. All outputs are HIGH after reset.

Read

Information is read from the TDA8400 when the R/$\overline{W}$ bit is set to logic 1. Only one information byte is sent from the device. No acknowledge is required from the master after transmitting. The format of the information byte is shown in Fig. 5.

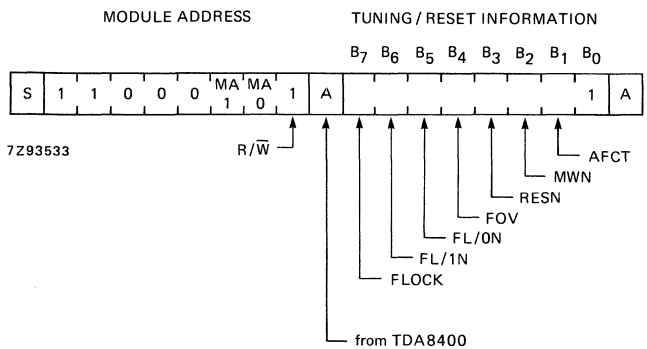


Fig. 5 Information byte format.

OPERATION (continued)

Tuning/reset information bits

FLOCK	Set to logic 1 when the tuning oscillator frequency is within the programmed tuning window (TUW) in the digital tuning mode or within the ± 800 kHz AFC hold range in the AFC mode.
FL/1N	Set to logic 0 (active LOW) when FLOCK changes from 0 to 1 and is reset to logic 1 automatically after tuning information has been read.
FL/0N	As for FL/IN buts is set to logic 0 when FLOCK changes from 1 to 0.
FOV	Indicates frequency overflow. When the tuner oscillator frequency is too high with respect to the programmed frequency, FOV is at logic 1, and when too low, FOV is at logic 0.
RESN	Set to logic 0 (active LOW) by a power-down-reset. It is reset to logic 1 automatically after tuning/reset information has been read.
MWN	MWN (frequency measuring window, active LOW) is at logic 1 for a period of 1,28 ms, during which time the results of frequency measurement are processed. During the remaining time, MWN is at logic 0 and the received frequency is measured.
AFCT	AFCT (tuning mode flag) is set to logic 1 when the TDA8400 is in AFC mode and reset to logic 0 when in the digital mode.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage:			
(pin 10)	V_{CCS}	max.	6 V
(pin 15)	V_{CCP}	max.	6 V
Input/output voltage (each pin)	V_n	max.	6 V
Total power dissipation	P_{tot}	max.	350 mW
Storage temperature range	T_{stg}	−25 to + 150	°C
Operating ambient temperature	T_{amb}	−10 to + 80	°C

DEVELOPMENT DATA

CHARACTERISTICS

T_{amb} = 25 °C; V_{P1}, V_{P2} at typical voltages, unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply voltage					
synthesizer (pin 10)	V_{CCS}	4,5	5	5,5	V
prescaler (pin 15)	V_{CCP}	4,5	5	5,5	V
Supply current					
synthesizer (pin 10)	I_{CCS}	–	12	–	mA
prescaler (pin 15)	I_{CCP}	–	43	–	mA
Total power dissipation	P_{tot}	–	275	–	mW
Operating ambient temperature range	T_{amb}	0	–	+ 70	°C
Operating storage temperature range	T_{stg}	−10	–	+ 85	°C
I²C bus inputs/outputs					
Inputs: SDA (pin 7); SCL (pin 6)					
Input voltage HIGH	V_{IH}	3,1	–	5,5	V
Input voltage LOW	V_{IL}	−0,3	–	1,6	V
Input current HIGH	I_{IH}	–	–	10	μA
Input current LOW	I_{IL}	–	–	10	μA
SDA output (pin 7, open collector)					
Output voltage LOW at I_{OL} = 3 mA	V_{OL}	–	–	0,4	V
Output sink current	I_{OL}	–	–	5	mA
Tuning voltage amplifier					
Input TI, output TUN (pins 9, 8)					
Input bias current	I_{TI}	−5	–	+ 5	nA
Output current LOW at V_{TUN} = 0,4 V	$-I_{TUNL}$	20	–	–	μA
Minimum charge IT to tuning amplifier					
TUHN = 0	CH_0	–	5	–	μA·μs
TUHN = 1	CH_1	–	125	–	μA·μs
Maximum current I into tuning amplifier					
TUHN = 0	I_{T0}	–	18	–	μA
TUHN = 1	I_{T1}	–	440	–	μA
AFC amplifier (Inputs AFC+, AFC− pins 13, 12)					
Differential input voltage	V_{DIF}	–	–	1	V
Transconductance at AFCS = 1	g_1	5	10	15	μA/V
Transconductance at AFCS = 0	g_0	30	50	70	μA/V
Common mode input voltage	V_{CM}	2,5	–	V_{P1}−1	V
Common mode rejection ratio	CMRR	–	50	–	dB
Power supply (V_{P1}) rejection ratio	PSRR	–	50	–	dB
Input current	I_I	–	–	1	μA

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Main band-selection output ports					
P0, P1, P2, P3 (pins 5 to 2, open collector)					
Output sink current					
LOW impedance	I_{BSL1}	0,8	1	1,2	mA
HIGH impedance	I_{BSH1}	–	–	10	μA
Prescaler inputs (VCO+ pin 16; VCO– pin 17)					
Input differential voltage (r.m.s. value)					
at f = 70 MHz	$V_{I(rms)}$	17,5	–	200	mV
at f = 150 MHz	$V_{I(rms)}$	10	–	200	mV
at f = 300 MHz	$V_{I(rms)}$	10	–	200	mV
at f = 500 MHz	$V_{I(rms)}$	10	–	200	mV
at f = 900 MHz	$V_{I(rms)}$	10	–	200	mV
at f = 1,1 GHz	$V_{I(rms)}$	25	–	200	mV
Input frequency	f_i	0,07	–	1,1	GHz
OSC input (pin 11)					
Crystal resistance at resonance (4 MHz)	R_{XTAL}	–	–	150	Ω
Power-down-reset					
Maximum supply voltage V_{P1} at which power-down reset is active	V_{PD}	3	–	4	V
Voltage level for valid module address					
Voltage level P0 (pin 5) for valid module address as a function of MA1, MA0					
MA1 MA0					
0 0		pin used as an output			
0 1	V_{VA01}	–0,3	–	0,8	V
1 0	V_{VA10}	2,4	–	V_{CCS}–1,6	V
1 1	V_{VA11}	V_{CCS}–0,3	–	V_{CCS}	V

TV AND VTR STEREO/DUAL SOUND PROCESSOR WITH I²C BUS CONTROL

GENERAL DATA

The TDA8405 integrated circuit is a processor for stereo/dual-language signals for stereo-sound television receivers and VTR. The modulated signals at the TDA8405 inputs need to be "(L+R)/2" or "language A" on one channel and "R" or "language B" on the second channel (where L = left and R = right). The second channel is also modulated with the pilot carrier. The IC is controlled via the two-line, bidirectional I²C bus.

Features

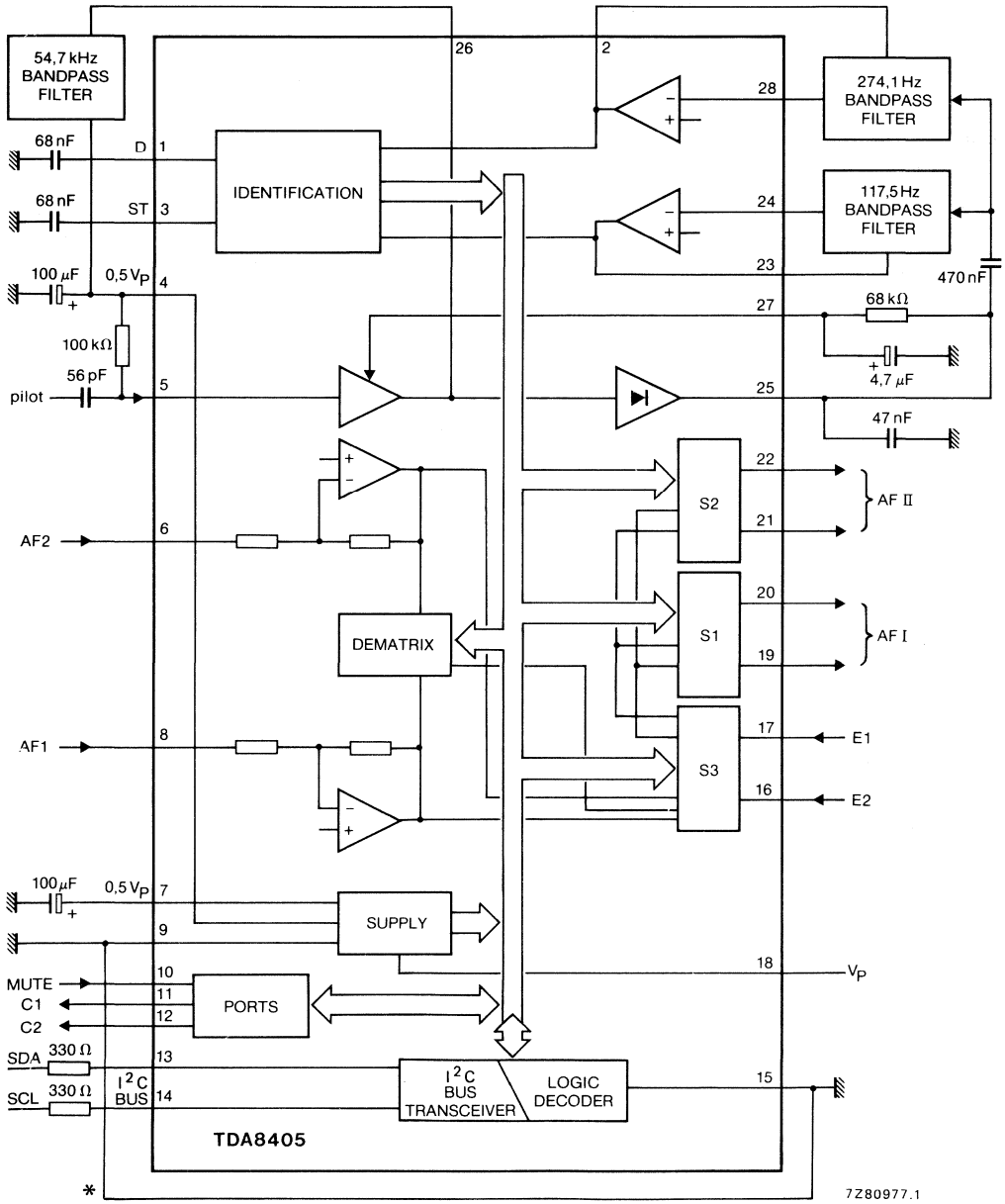
- Amplification of the two a.f. input signals by integrated operational amplifiers.
- Low distortion stereo dematrix
- All operational amplifiers are offset compensated
- I²C bus transceiver for system control (port control, mute, mode select, identification, etc.)
- Input port for fast muting
- Two general purpose output ports (three-state, bus-controlled)

QUICK REFERENCE DATA

Supply voltage	$V_P = V_{18\text{-}9\text{-}15}$	typ.	12 V
Supply current	$I_P = I_{18}$	typ.	25 mA
A.F. input signal	$V_{i(rms)} = V_{6\text{-}9}, V_{8\text{-}9}$	typ.	1 V
Weighted signal-to-noise ratio of the a.f. output-signals (CCIR 468/2)	(S+N)/N	≥	70 dB
Crosstalk attenuation: stereo mode at f = 1 kHz	α_S	>	40 dB
dual sound mode at f = 40 to 12 500 Hz	α_{DS}	>	70 dB
Pilot signal input sensitivity	$V_i = V_{5\text{-}9(rms)}$	typ.	5 mV
Pilot signal amplifier gain control range	ΔG_V	>	40 dB

PACKAGE OUTLINE

28-lead DIL; plastic (SOT-117).



* Direct connection between pins 9 and 15 is needed.

Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 18)*	$V_P = V_{18-9, 15}$	max.	13,2 V
Output current (pins 19, 20, 21, 22)	I_n	max.	5 mA
Output current (pins 2, 23)	I_n	max.	1 mA
Output current (pins 11, 12)	I_n	max.	3 mA
Voltage range at any pin	V_n		0 to V_P V
Total power dissipation	P_{tot}	max.	1 W
Storage temperature range	T_{stg}		−40 to + 150 °C
Operating ambient temperature range	T_{amb}		0 to + 70 °C

DEVELOPMENT DATA

* Supply voltage may be applied only when pins 9 and 15 are connected to ground.

CHARACTERISTICS

T_{amb} = 25 °C; V_P = 12 V; $V_{i(af)rms}$ = 1 V; f = 1 kHz; dematrix aligned; $V_{i\ pilot(rms)}$ = 16 mV; test circuit Fig. 2; unless otherwise specified.

parameter	symbol	min.	typ.	max.	unit
Supply voltage	$V_P = V_{18\text{-}9,\ 15}$	10,8	12	13,2	V
Supply current at V_P = 12 V	$I_P = I_{18}$	–	25	–	mA
Reference voltage	$V_{ref} = V_{4\text{-}9,\ 15}$	–	$V_P/2$	–	V
DC levels (pins 5, 6, 7, 8, 16 17, 19, 20, 21, 22, 24, 28)	$V_{n\text{-}9,\ 15}$	–	$V_P/2$	–	V
BUS TRANSCEIVER (pins 13, 14) (note 1)					
Clock SCL					
Voltage level LOW	$V_{14\text{-}15}$	−0,3	–	1,5	V
Voltage level HIGH	$V_{14\text{-}15}$	3,0	–	–	V
Timing LOW period	t_{PL}	4,7	–	–	μs
Timing HIGH period	t_{PH}	4,0	–	–	μs
Rise time	t_r	–	–	1	μs
Fall time	t_f	–	–	0,3	μs
Input current HIGH	I_{IH}	–	–	10	μA
Input current LOW	$-I_{IL}$	–	–	10	μA
Data					
Voltage level LOW	$V_{13\text{-}15}$	−0,3	–	1,5	V
Voltage level HIGH	$V_{13\text{-}15}$	3,0	–	–	V
Rise time	t_r	–	–	1,0	μs
Fall time	t_f	–	–	0,3	μs
Set-up time data	t_{SU}	0,25	–	–	μs
Input current HIGH	I_{13}	–	–	10	μA
Input current LOW	$-I_{13}$	–	–	10	μA
Output current LOW	$+I_{13}$	3,0	–	–	mA
MUTE PORT (pin 10) note 2					
Input voltage LOW	$V_{10\text{-}15}$	–	–	1,5	V
Input voltage HIGH	$V_{10\text{-}15}$	8	–	–	V

DEVELOPMENT DATA

parameter	symbol	min.	typ.	max.	unit
CONTROL PORTS (pins 11, 12)					
3-state HIGH, LOW, high ohmic					
Output resistance in open state	$R_{11, 12\text{-}15}$	50	–	–	kΩ
Output voltage LOW	$V_{11, 12\text{-}15}$	–	–	0,8	V
Output voltage HIGH	$V_{11, 12\text{-}15}$	V_{P}-1	–	–	V
Output current LOW	$I_{11, 12}$	500	–	–	μA
Output current HIGH	$-I_{11, 12}$	80	–	–	μA
IDENTIFICATION (See Fig. 3)					
Input amplifier and demodulator					
Input voltage	$V_{5\text{-}9(p\text{-}p)}$	–	–	2,0	V
Min. input voltage	$V_{5\text{-}9(rms)}$	5,0	–	–	mV
Input resistance	$R_{5\text{-}9}$	500	–	–	kΩ
Gain	$G_{25\text{-}9}$	–	42	–	dB
Gain control range	ΔG	40	–	–	dB
Output voltage (gain-controlled)	$V_{25\text{-}9(p\text{-}p)}$	–	1,5	–	V
Operational amplifiers					
Input current	$I_{24, 28}$	–	70	–	nA
Gain at f = 200 Hz	$G_{23\text{-}24}$, $G_{2\text{-}28}$	78	–	–	dB
Output current	$I_{2, 23}$	1,5	–	–	mA
Output resistance	$R_{2, 23\text{-}9}$	–	2	–	kΩ
Output load capacitance	$C_{2, 23\text{-}9}$	–	–	30	pF
Schmitt trigger					
A.C. input signal	$V_{2, 23\text{-}9(rms)}$	–	1	–	V
Internal discharge resistors	$R_{1, 3\text{-}9}$	–	3	–	kΩ
A.F. STAGES					
Input resistance (pins 6, 8, 16 and 17)	$R_{n\text{-}9}$	10	–	–	kΩ
Gain ($V_{19, 20, 21, 22\text{-}9}/V_{6, 8\text{-}9}$)	G1	–	6	–	dB
Gain ($V_{19, 20, 21, 22\text{-}9}/V_{16, 17\text{-}9}$)	G2	–	0	–	dB
Input voltage	$V_{6, 8\text{-}9(rms)}$	–	1	–	V
Crosstalk attenuation (notes 3, 4 and 9)					
dual sound	α_{DS}	70	–	–	dB
stereo f = 250 Hz to 6,3 kHz	α_{S}	40	–	–	dB
stereo f = 40 Hz to 250 Hz; 6,3 kHz to 12,5 kHz	α_{S}	30	–	–	dB

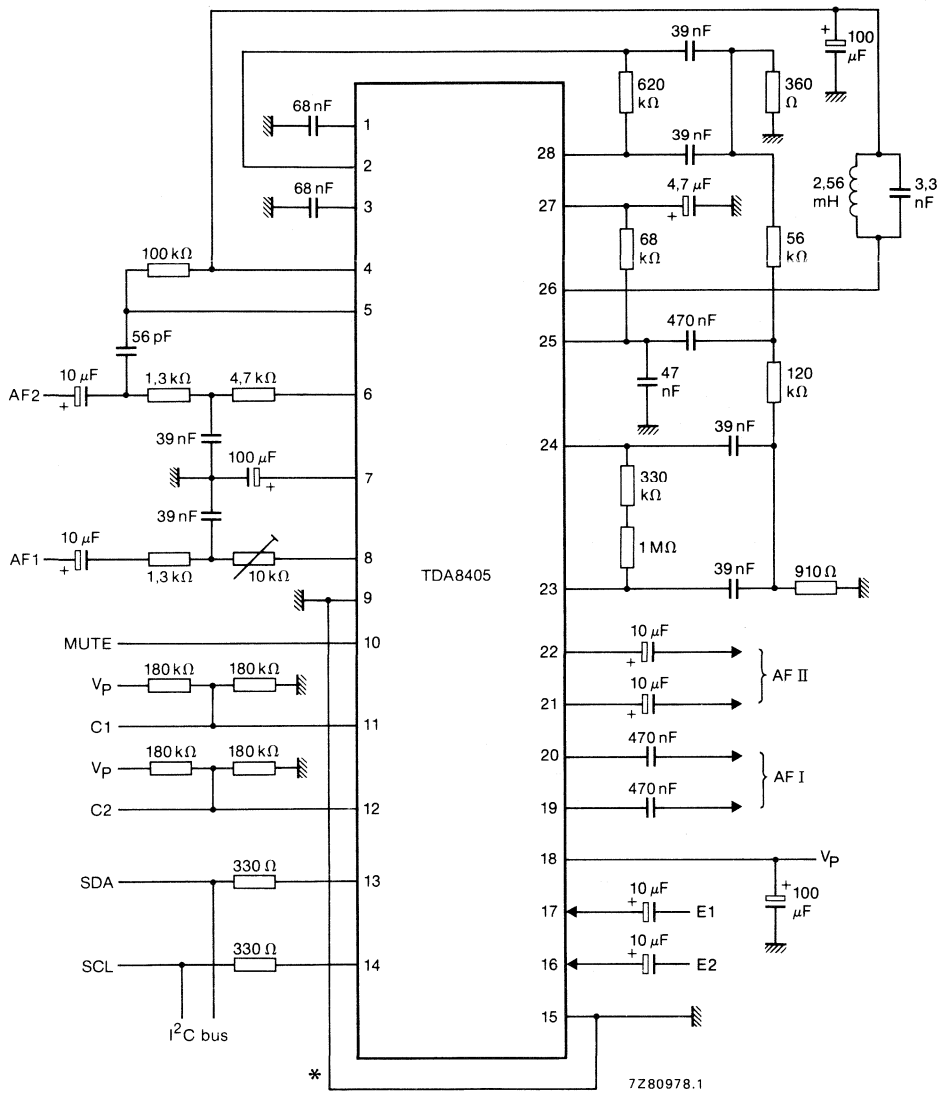
CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
A.F. STAGES (continued)					
Output resistance	$R_{19,20,21,22}$	–	200	300	Ω
Output load capacitance (pins 19, 20, 21 and 22)	$C_{n\text{-}9}$	–	–	1,5	nF
D.C. offsets (note 8) at pins 19,20,21 and 22	Δ_V	–	–	30	mV
Total harmonic distortion (notes 4 and 5)	THD	–	0,1	0,5	%
Output signal (r.m.s. value) (pins 19, 20, 21 and 22)	$V_{n\text{-}9(rms)}$	–	–	2,0	V
Ripple rejection (note 6)	RR	30	35	–	dB
Noise rejection (note 7) (noise from I^2C bus)	NR	80	–	–	dB
Signal-to-noise ratio (note 7)	(S+N)/N	70	–	–	dB
Ident signal suppression		70	–	–	dB
Signal suppression during mute (notes 4 and 7)		70	–	–	dB

Notes to the characteristics

1. Full specification of the I^2C bus will be supplied on request.
2. Programmable mute state. If the SC3 bit in the I^2C bus is LOW then the mute input is active LOW; if the mute bit is set to HIGH then the mute input is active HIGH.
3. Crosstalk attenuation definition: 20 log (unwanted output signal/input signal).
4. Frequency range: 40 Hz $<$ f $<$ 12,5 kHz.
5. In dual sound mode.
6. Test circuit as in Fig. 4: ripple rejection = output modulation due to hum on the supply line.
7. Related to 2 V (r.m.s.) output signal at pin 19, 20, 21 or 22; noise weighted according to CCIR 468/2.
8. Caused by any change of the switch position.
9. α_S measured without de-emphasis network.

DEVELOPMENT DATA



* Direct connection between pins 9 and 15 is needed.

Fig. 2 Test circuit.

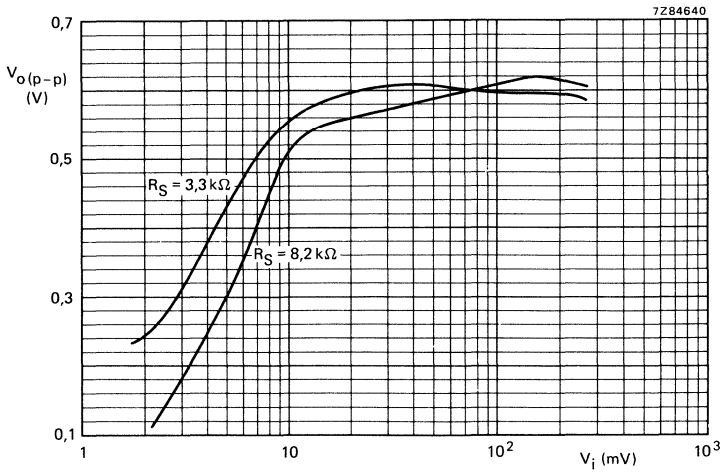


Fig. 3 Controlled output voltage as a function of the input signal (Q = 80); pilot frequency f_o = 54 kHz; R_S = source resistance.

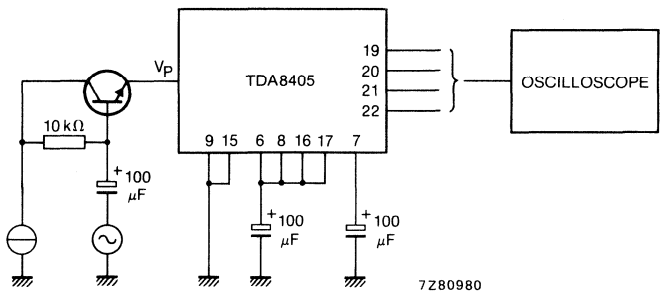
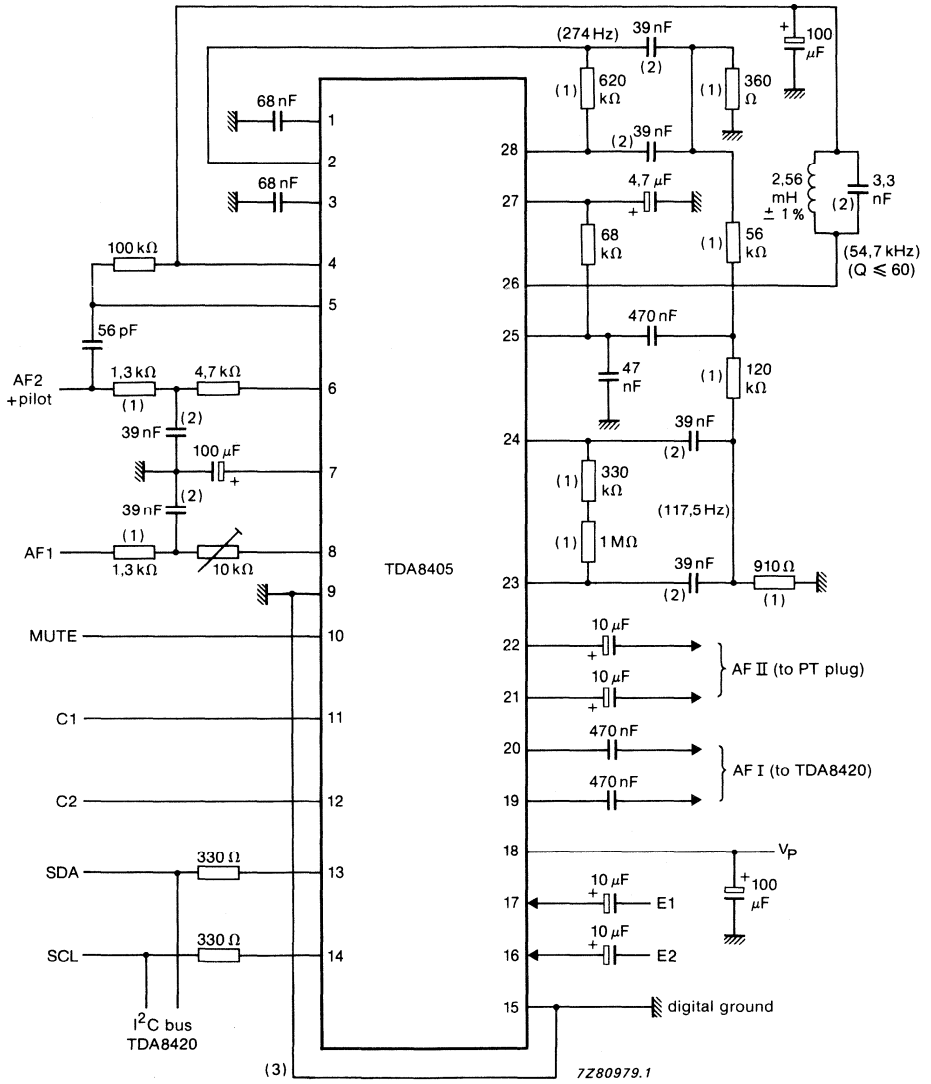


Fig. 4 Test circuit for ripple rejection: supply (d.c.) + pulse (r.m.s.) voltage at 100 Hz = 12 V + 50 mV.

DEVELOPMENT DATA



(1) ± 1 % tolerance

(2) polystyrene film/foil capacitors (KS) : ± 1 % tolerance

metallized polyethyleneterephthalate film capacitors (MKT) : ± 10 % tolerance

(3) Direct connection is needed between pins 9 and 15

Fig. 5 Application diagram.

HI-FI STEREO AUDIO PROCESSOR; I²C BUS

GENERAL DESCRIPTION

The TDA8420 is a monolithic bipolar integrated stereo sound circuit with a loudspeaker channel (CH1) and a headphone channel (CH2), digital controlled via the I²C bus, for application in hi-fi audio and television sound.

Features

- Input selector
- Mode selector
- Loudspeaker channel (CH1) } with volume control, balance control and mute
- Headphone channel (CH2) }
- Pseudo stereo and spatial function
- Bass and treble control

QUICK REFERENCE DATA

parameter	symbol	min.	typ.	max.	unit
Supply voltage (pin 4)	V_{CC}	7,5	12	14	V
Input signal handling	V_I	2	–	–	V
Input sensitivity full power at the output stage	V_i	–	200	–	mV
Signal plus noise-to-noise ratio	(S+N)/N	–	90	–	dB
Total harmonic distortion	THD	–	0,05	–	%
Channel separation	α	–	75	–	dB
Volume control range CH1	G	–46	–	16	dB
Treble control range	G	–12	–	12	dB
Bass control range	G	–12	–	15	dB
Volume control range CH2	G	–62	–	0	dB

PACKAGE OUTLINE

28-lead dual in-line; plastic (SOT-117).

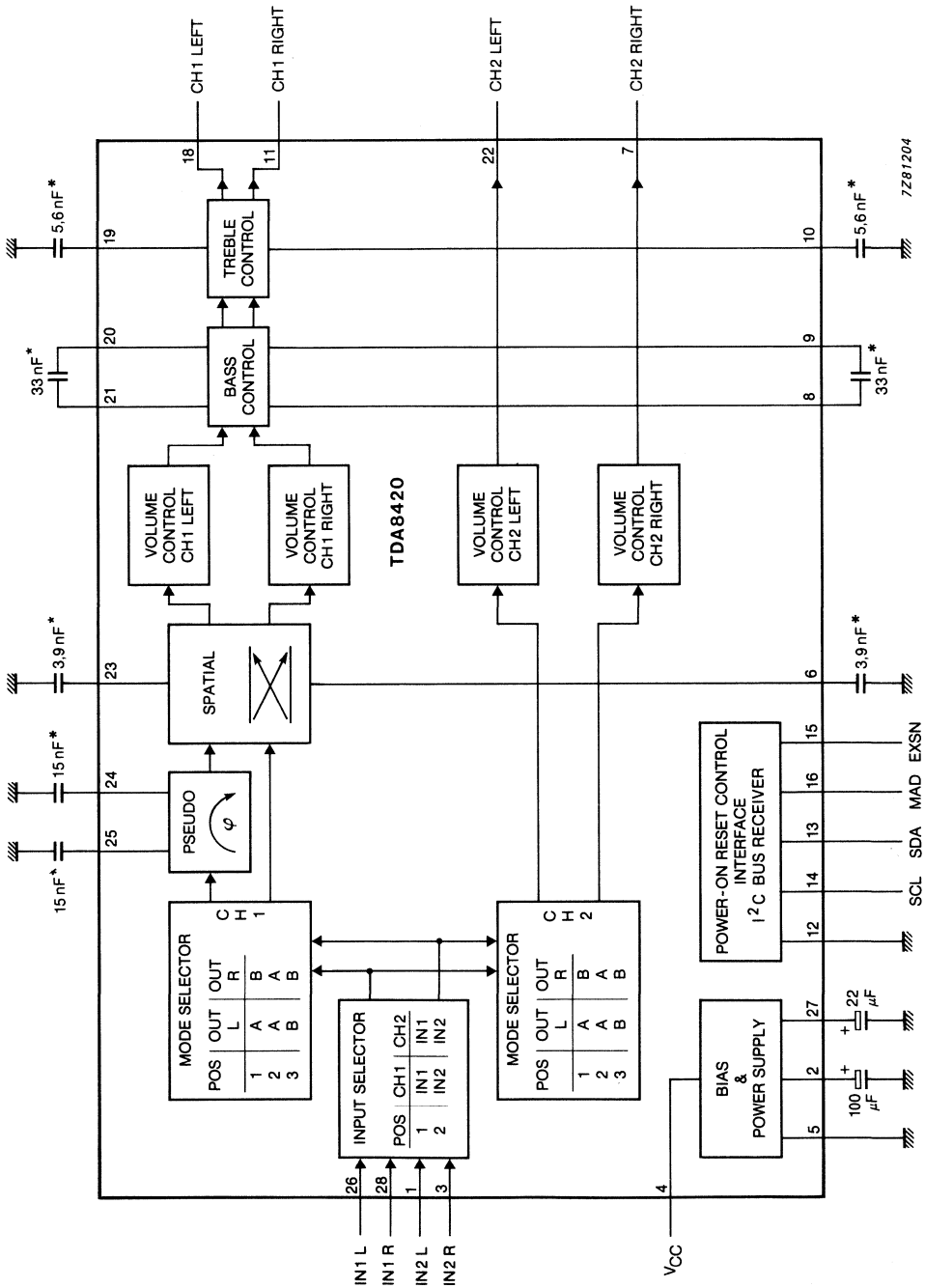


Fig. 1 Block diagram.

* These values are dependent on the required frequency response and effect.

PINNING

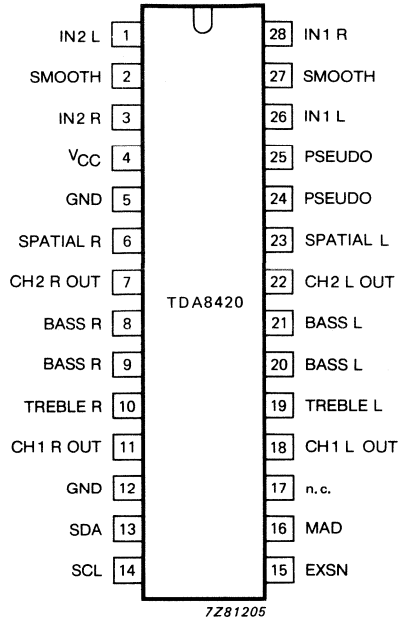


Fig. 2 Pinning diagram.

FUNCTIONAL DESCRIPTION

Input selector

The input to channel 1 (CH1) and channel 2 (CH2) is determined by the input selector. The selection is made from the following AF input signals:

- IN1 L (pin 26); IN1 R (pin 28)
  or
- IN2 L (pin 1); IN2 R (pin 3)

Where IN1 is an internal input signal and IN2 an external input signal.

Mode selector

For each channel (CH1 and CH2) there is a mode selector which selects between stereo, sound A and sound B in the event of bilingual transmission. Both mode selectors can be controlled independently.

Headphone channel (CH2)

Volume control and balance

The stages for volume control for CH2 consist of two parts for left and right. In each part the gain can be adjusted between 0 and −62 dB in steps of 2 dB. An additional step allows an attenuation of $\geqslant$ 90 dB. Both parts can be controlled independently over the whole range, which allows the balance to be varied by controlling the volume of left and right.

Loudspeaker channel (CH1)

Volume control and balance

The loudspeaker channel (CH1) also consists of two parts for volume control (left and right). In each part the gain can be adjusted between + 16 dB and −62 dB in steps of 2 dB. An additional step allows an attenuation of $\geqslant$ 90 dB. Both parts can be controlled independently over the whole range, which allows the balance to be varied by controlling the volume of left and right.

Stereo/pseudo stereo/spatial stereo mode

It is possible to select three modes. Stereo, pseudo or spatial stereo. The pseudo stereo mode receives mono transmissions and the stereo and spatial stereo mode receives stereo transmissions.

Bass control

The bass control stage can be switched from an emphasis of 15 dB to an attenuation of 12 dB for low frequencies in steps of 3 dB.

Treble control

The treble control stage can be switched from + 12 dB to −12 dB in steps of 3 dB.

Bias and power supply

The TDA8420 includes a bias and power supply stage, which generates a voltage of ½ V_{CC} with a low output impedance and injector currents for the logic part.

Power-on reset

The on-chip power-on reset circuit sets the mute bit to active, which mutes both the loudspeaker channel (CH1) and the headphone channel (CH2). The muting can be switched by transmission of the mute bit.

I^2C bus receiver and data handling

Bus specification

The TDA8420 is controlled via the 2-wire I^2C bus by a microcomputer. The two wires (SDA – serial data, SCL – serial clock) carry information between the devices connected to the bus. Both SDA and SCL are bidirectional lines, connected to a positive supply voltage via a pull up resistor.
When the bus is free both lines are HIGH. The data on the SDA line must be stable during the HIGH period of the clock. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW. The set up and hold times are specified in AC CHARACTERISTICS.

A HIGH-to-LOW transition of the SDA line while SCL is HIGH is defined as a start condition.
A LOW-to-HIGH transition of the SDA line while SCL is HIGH is defined as a stop condition.
The bus receiver will be reset by the reception of a start condition. The bus is considered to be busy after the start condition. The bus is considered to be free again after a stop condition.

Module address

Data transmission to the TDA8420 starts with the module address MAD.

MSB								LSB
1	0	0	0	0	0	MAD	R/W	ACK

Fig. 3 TDA8420 module address.

The module address is determined by pin 16. When connected to ground MAD = 0; when connected to V_{CC} MAD = 1. Thus two TDA8420s can be selected within a system.

Subaddress

After the module address byte a second byte is used to select the functions for both channels:

- CH1 – Volume left, volume right, bass, treble and switch functions
- CH2 – Volume left, volume right and switch functions

The subaddress SAD is stored within the TDA8420. Table 1 defines the coding of the second byte after the module address MAD.

Table 1 Second byte after module address MAD

		128	64	32	16	8	4	2	1
	function	MSB 7	6	5	4	3	2	1	LSB 0
CH1	volume left	0	0	0	0	0	0	0	0
	volume right	0	0	0	0	0	0	0	1
	bass	0	0	0	0	0	0	1	0
	treble	0	0	0	0	0	0	1	1
	switch functions	0	0	0	0	1	0	0	0
CH2	volume left	0	0	0	0	0	1	0	0
	volume right	0	0	0	0	0	1	0	1
	switch functions	0	0	0	0	1	1	0	0
						subaddress SAD			

Definition of 3rd byte

A third byte is used to transmit data to the TDA8420. Table 2 defines the coding of the third byte after module address MAD and subaddress SAD.

Table 2 Third byte after module address MAD and subaddress SAD

	function		MSB 7	6	5	4	3	2	1	LSB 0
	volume left	VL1	1	1	V05	V04	V03	V02	V01	V00
	volume right	VR1	1	1	V15	V14	V13	V12	V11	V10
CH1	bass	BA	1	1	1	1	BA3	BA2	BA1	BA0
	treble	TR	1	1	1	1	TR3	TR2	TR1	TR0
	switch functions	S1	1	1	MU	EFL	STL	ML1	ML0	IS
	volume left	VL2	1	1	V25	V24	V23	V22	V21	V20
CH2	volume right	VR2	1	1	V35	V34	V33	V32	V31	V30
	switch functions	S2	1	1	1	1	EXS	MH1	MH0	1

Truth tables

Truth tables for the switch functions

Table 3 Input selector

function	IS
IN1	0
IN2	1

Table 4 Mode selectors

	CH1		CH2	
mode	ML0	ML1	MH0	MH1
stereo	1	1	1	1
sound A	1	0	1	0
sound B	0	1	0	1
----------	0	0	0	0

Table 5 Stereo/pseudo stereo/spatial stereo

choice	STL	EFL
spatial	1	1
stereo	1	0
pseudo	0	1
----------	0	0

Table 6 Mute

mute	MU
active; automatic after POR*	1
not active	0

Table 7 Output for external switch

EXSN	EXS
ground	1
open collector	0

Where: POR = Power-On Reset.

Truth tables for the volume base and treble controls.

Table 8 Volume control

CH1	CH2	Vx5	Vx4	Vx3	Vx2	Vx1	Vx0
16	0	1	1	1	1	1	1
–46	–62	1	0	0	0	0	0
$\leqslant$ –90	$\leqslant$ –90	0	1	1	1	1	1
$\leqslant$ –90	$\leqslant$ –90	0	0	0	0	0	0

Where: The values of CH1 and CH2 are in 2 dB/step measured in dBs.

* Attenuation $\geqslant$ 90 dB.

Table 9 Bass control

3dB/step (dB)	BA3	BA2	BA1	BA0
15	1	1	1	1
---	---	---	---	---
---	---	---	---	---
---	---	---	---	---
15	1	0	1	1
12	1	0	1	0
---	---	---	---	---
---	---	---	---	---
---	---	---	---	---
0	0	1	1	0
---	---	---	---	---
---	---	---	---	---
---	---	---	---	---
−12	0	0	1	0
---	---	---	---	---
---	---	---	---	---
---	---	---	---	---
−12	0	0	0	0

Table 10 Treble control

3dB/step (dB)	TR3	TR2	TR1	TR0
12	1	1	1	1
---	---	---	---	---
---	---	---	---	---
---	---	---	---	---
12	1	0	1	0
---	---	---	---	---
---	---	---	---	---
---	---	---	---	---
0	0	1	1	0
---	---	---	---	---
---	---	---	---	---
---	---	---	---	---
−12	0	0	1	0
---	---	---	---	---
---	---	---	---	---
---	---	---	---	---
−12	0	0	0	0

Sequence of data transmission

After a power-on reset all eight functions have to be adjusted with eight data transmissions. It is recommended that data information for switch functions in CH1 are transmitted last because all functions have to be adjusted when the muting is switched off. The sequence of transmission of other data information is not critical.

The order of data transmission is shown in Figures 4 and 5. The number of data transmissions is unrestricted but before each data byte the module address MAD and the correct subaddress SAD is required.

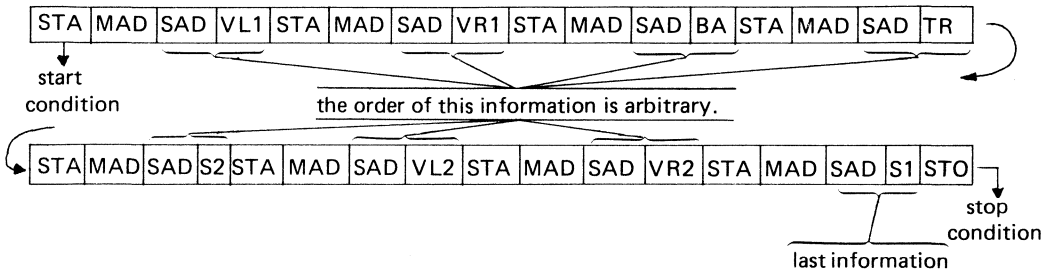


Fig. 4 Data transmission after a power-on reset.

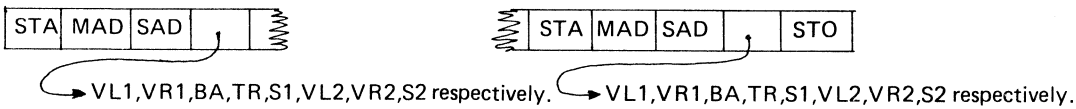


Fig. 5 Data transmission except after power-on reset.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage	V_{CC}	0	16	V
Voltage range for external capacitors				
pins 2, 6, 8 to 10, 19 to 21, 23 to 25, 27	V_{cap}	0	V_{CC}	V
pin 13	V_{SDA}	0	V_{CC}	V
pin 14	V_{SCL}	0	V_{CC}	V
pin 15	V_{EXSN}	0	V_{CC}	V
pin 16	V_{MAD}	0	V_{CC}	V
Input voltage range				
at pins 1, 3, 7, 11, 18, 22, 26, 28	V_I	0	V_{CC}	V
Output voltage range				
at pins 1, 3, 7, 11, 18, 22, 26, 28	V_O	0	V_{CC}	V
Output current at pins 7, 11, 18, 22	I_O	–	45	mA
Total power dissipation				
at $T_{amb} < 70\ ^oC$	P_{tot}	–	1350	mW
Operating ambient temperature range	T_{amb}	0	70	^oC
Storage temperature range	T_{stg}	−25	150	^oC

DC CHARACTERISTICS

V_{CC} = 12 V; T_{amb} = 25 °C; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply voltage (pin 4)	V_{CC}	7,5	12	14	V
Supply current at V_{CC} = 12 V	I_{CC}	–	42	55	mA
Input voltage IN1 L, IN1 R, IN2 L, IN2 R DC voltage internally generated; capacitive coupling recommended	V_I	5,4	6,0	6,6	V
MAD (pin 16)					
input voltage HIGH	V_{IH}	3,0	–	V_{CC}	V
input voltage LOW	V_{IL}	0	–	1,5	V
input current HIGH	I_{IH}	–	–	1,0	μA
input current LOW	I_{IL}	–	1	10	μA
SDA; SCL (pins 13 and 14)					
input voltage HIGH	V_{IH}	3,0	–	V_{CC}	V
input voltage LOW	V_{IL}	−0,3	–	1,5	V
input current HIGH	I_{IH}	–	–	1,0	μA
input current LOW	I_{IL}	–	1	10	μA
Output voltage CH1 (pins 11 and 18); CH2 (pins 7 and 22)	V_O	5,4	½ V_{CC}	6,6	V
External capacitors					
pins 6 to 10; 19 to 21; 23 to 25	$V_{cap.n}$	–	½ V_{CC}	–	V
pin 2	$V_{cap.2}$	–	V_{CC}−0,1	–	V
External switch (pin 15) at I_{EXSN} = 1 mA					
Output voltage HIGH	V_{EXSNH}	–	–	16	V
Output voltage LOW	V_{EXSNL}	–	–	0,3	V

AC CHARACTERISTICS

V_{CC} = 12 V; bass/treble in linear position; pseudo and spatial stereo off; $R_L > 10\ k\Omega$; $C_L < 100\ pF$; T_{amb} = 25 °C unless otherwise specified.

parameter	symbol	min.	typ.	max.	unit
I²C bus timing (see Fig. 6)					
SDA, SCL (pin 13 and 14)					
Clock frequency range	f_{SCL}	0	–	100	kHz
The HIGH period of the clock	t_{HIGH}	4	–	–	μs
The LOW period of the clock	t_{LOW}	4,7	–	–	μs
SCL rise time	t_r	–	–	1	μs
SCL fall time	t_f	–	–	0,3	μs
Set-up time for start condition	$t_{SU;STA}$	4,7	–	–	μs
Hold time for start condition	$t_{HD;STA}$	4	–	–	μs
Set-up time for stop condition	$t_{SU;STO}$	4,7	–	–	μs
Time bus must be free before a new transmission can start	t_{BUF}	4,7	–	–	μs
Set-up time DATA	$t_{SU;DAT}$	250	–	–	ns
Input signals					
IN1 L (pin 26) IN1 R (pin 28) IN2 L (pin 1) IN2 R (pin 3)					
Input signal handling (r.m.s. value) at V_u = −4 dB; THD ⩽ 0,5%	$V_{i(rms)}$	2	–	–	V
Input resistance	R_{n-5}	35	50	–	kΩ
Frequency response (−0,5 dB) bass and treble in linear position; stereo mode; effects off	f	20	–	20 000	Hz

AC CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
LOUDSPEAKER CHANNEL OUTPUTS					
CH1 LEFT (pin 18); CH1 RIGHT (pin 11)					
Output voltage range (r.m.s. value) at THD $\leqslant$ 0,5%	$V_{o(rms)}$	2	–	–	V
Load resistance	R_L	10	–	–	kΩ
Output impedance	Z_O	–	–	100	Ω
Noise level weighted according to CCIR468-2					
gain = 16 dB	V_n	–	90	–	μV
gain = 0 dB	V_n	–	20	40	μV
gain = $\leqslant$ –90 dB	V_n	–	15	–	μV
Total harmonic distortion (f = 20 Hz to 12,5 kHz)					
for $V_{i(rms)}$ = 0,5 V; gain = + 16 dB to –30 dB	THD	–	0,05	0,2	%
for $V_{i(rms)}$ = 1,0 V; gain = + 2 dB to –30 dB	THD	–	0,07	0,2	%
for $V_{i(rms)}$ = 2,0 V; gain = –4 dB to –30 dB	THD	–	0,1	–	%
Channel separation at 10 kHz gain = 0 dB	α_{cr}	–	75	–	dB
Ripple rejection (gain = 0 dB; bass and treble in linear position) f_{ripple} = 100 Hz	RR_{100}	–	50	–	dB
Crosstalk attenuation from logic inputs to AF outputs (gain = 0 dB; bass and treble in linear position)	α_L	–	110	–	dB
VOLUME CONTROL					
For truth table see Table 8					

parameter	symbol	min.	typ.	max.	unit
Loudspeaker channel (CH1)					
Control range at f = 1 kHz					
maximum voltage gain (16 dB step)	G_{max}	15	–	–	dB
minimum voltage gain (–46 dB step)	G_{min}	–43	–	–	dB
last position	G_{off}	–80	–85	–	dB
mute position	G_{mute}	–85	–90	–	dB
Resolution	G_{step}	–	2	–	dB/step
Gain difference between left and right AF channel (note 1)					
gain from 16 dB to –30 dB	ΔG	–	–	0,5	dB
gain from –30 dB to –46 dB	ΔG	–	–	1	dB
TREBLE CONTROL (CH1)					
For truth table see Table 10					
Control range for C_{10-5}; C_{19-5} = 5,6 nF					
Maximum emphasis at 15 kHz with respect to linear position	G	11	12	13	dB
Maximum attenuation at 15 kHz with respect to linear position	G	11	12	13	dB
Resolution	G_{step}	–	3	–	dB/step
BASS CONTROL					
For truth table see Table 9					
Control range for C_{8-9}; C_{20-21} = 33 nF					
Maximum emphasis at 40 kHz with respect to linear position	G	14	15	16	dB
Maximum attenuation at 40 kHz with respect to linear position	G	11	12	13	dB
Resolution	G_{step}	–	3	–	dB/step
SPATIAL AND PSEUDO FUNCTION					
Spatial:					
Antiphase crosstalk	α	–	50	–	%
Pseudo:					
Phase shift			(see Fig. 15)		

AC CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
HEADPHONE CHANNEL OUTPUTS					
CH2 LEFT (pin 22); CH2 RIGHT (pin 7)					
Output voltage range (r.m.s. value) at THD $\leqslant$ 0,5%	$V_{o(rms)}$	2	–	–	V
Load resistance	R_L	10	–	–	kΩ
Output impedance	Z_O	–	–	100	Ω
Noise level (weighted according to CCIR468-2)					
gain = 0 dB	V_n	–	15	–	μV
gain = 16 dB	V_n	–	12	25	μV
gain = $\leqslant$ –90 dB	V_n	–	10	–	μV
Total harmonic distortion (f = 20 Hz to 12,5 kHz)					
for $V_{i(rms)}$ = 0,2 V; gain = 0 dB to –30 dB	THD	–	0,01	0,2	%
for $V_{i(rms)}$ = 1,0 V; gain = 0 dB to –30 dB	THD	–	0,1	–	%
for $V_{i(rms)}$ = 2,0 V gain = –4 dB to –30 dB	THD	–	0,3	–	%
Channel separation at 10 kHz gain = 0 dB	α_{cr}	–	75	–	dB
Ripple rejection (gain = 0 dB; bass and treble in linear position) f_{ripple} = 100 Hz	RR_{100}	–	50	–	dB
Crosstalk attenuation from logic inputs to AF outputs (gain = 0 dB; bass and treble in linear position)	α_L	–	110	–	dB
Crosstalk between any input/output f = 100 Hz to 12,5 kHz	α	65	70	–	dB
Crosstalk IN1/IN2 gain = 0 dB; R_G = 0	α	95	100	–	dB

parameter	symbol	min.	typ.	max.	unit
Headphone channel (CH2)					
Control range					
maximum voltage gain (0 dB step)	G_{max}	−1	–	–	dB
minimum voltage gain (−62 dB step)	G_{min}	−57	–	–	dB
last position	G_{off}	−80	−85	–	dB
mute position	G_{mute}	−85	−90	–	dB
Resolution	G_{step}	–	2	–	dB/step
Gain difference between left and right AF channel (note 1)					
gain from 0 dB to −40 dB	ΔG	–	–	0,5	dB
gain from −40 dB to −62 dB	ΔG	–	–	2	dB

Note to the AC characteristics

1. Balance is realized via software by different volume settings in both channels.

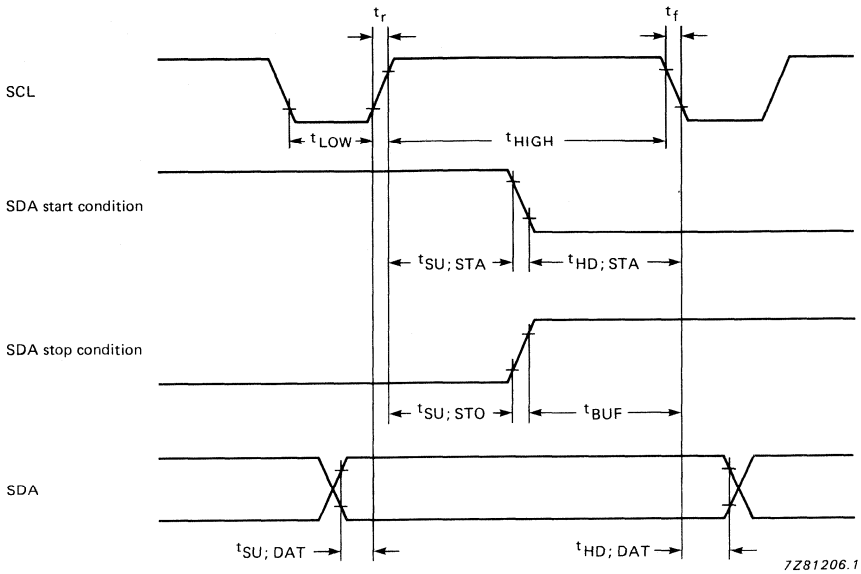


Fig. 6 Timing requirements for I²C bus.

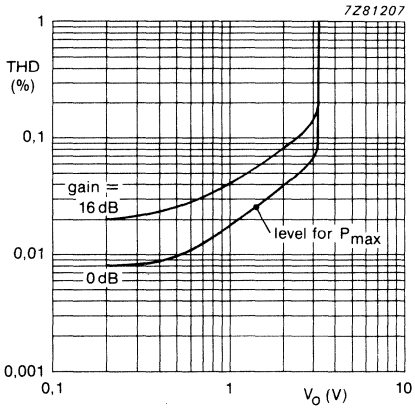


Fig. 7 Distortion loudspeaker channel CH1 as a function of the output voltage with gain as parameter.

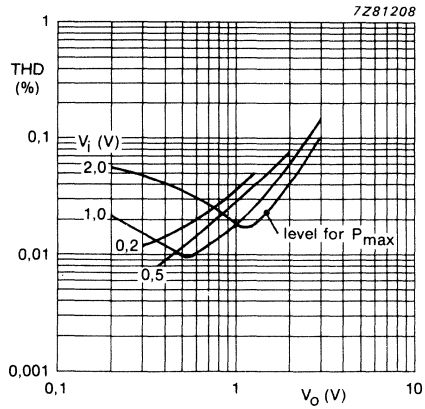


Fig. 8 Distortion loudspeaker channel CH1 as a function of the output voltage with input voltage as parameter.

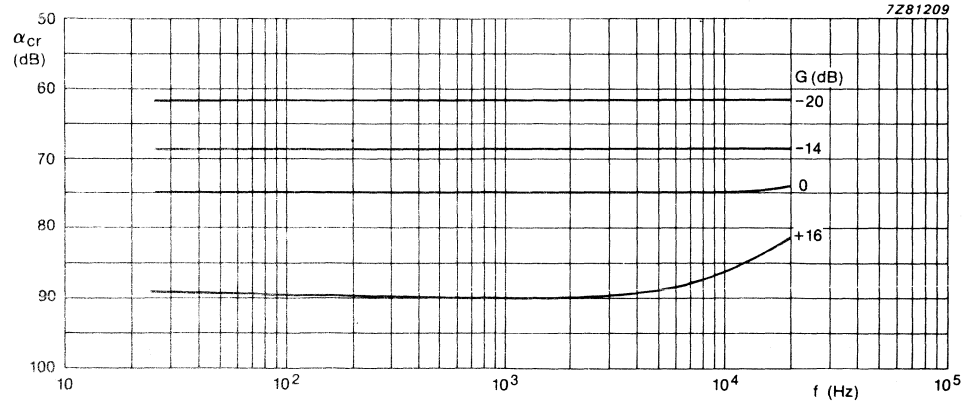


Fig. 9 Channel separation loudspeaker channel CH1 as a function of frequency.

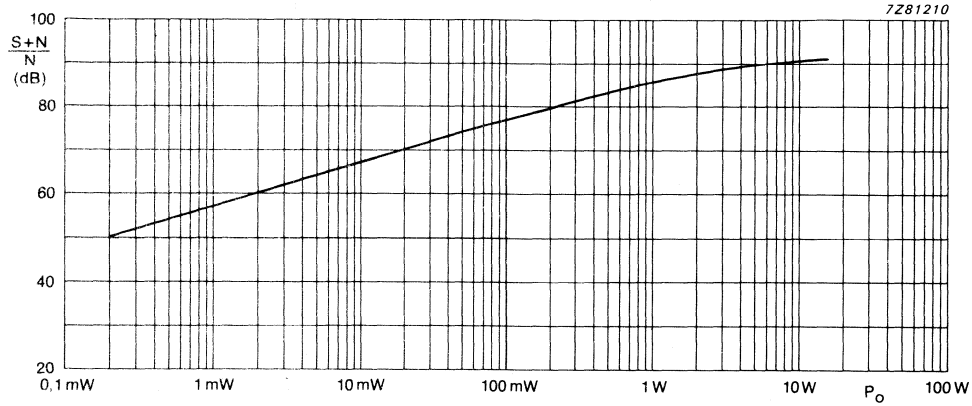


Fig. 10 Signal-to-noise ratio as a function of output power.
Input voltage V_i = 0,5 V; according to CCIR; quasi peak; P_o = 15 W.

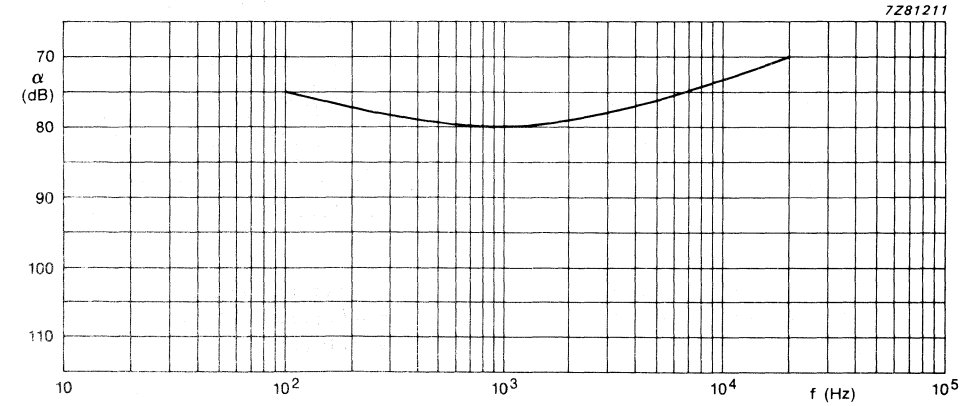


Fig. 11 Crosstalk 2-tone mode as a function of frequency.
CH1: mode AA, Gain + 16 dB; CH2: mode BB, Gain 0 dB. Signal input RIGHT; input LEFT to ground, measured at output CH1.

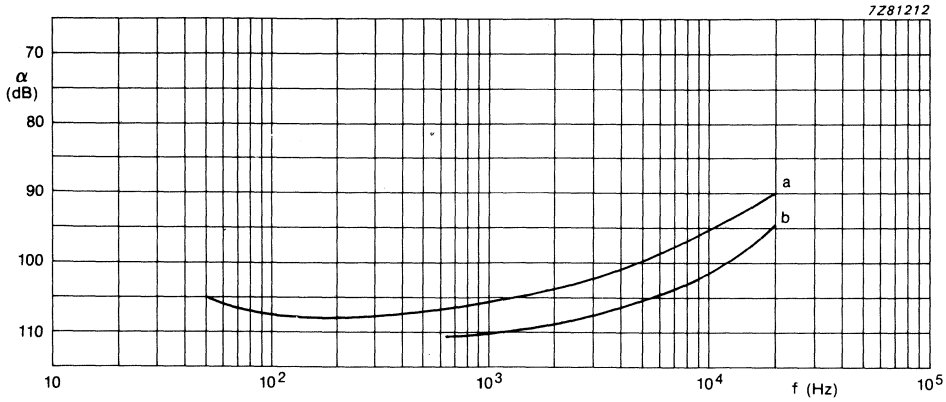


Fig. 12 Crosstalk between IN1 and IN2 as a function of frequency; measured at output CH1, $R_G = 0$.
a) Gain = + 16 dB; V_i = 200 mV. b) Gain = 0 dB; V_i = 1 V.

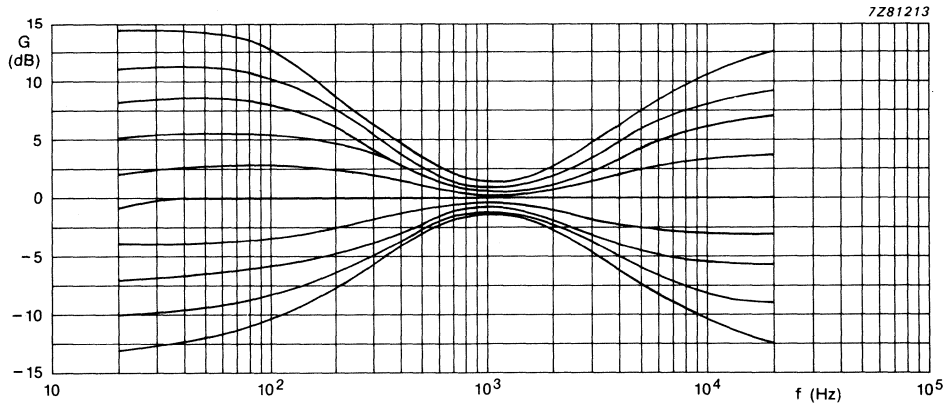


Fig. 13 Bass and treble tone control. C_{bass} = 33 nF, C_{treble} = 5,6 nF.

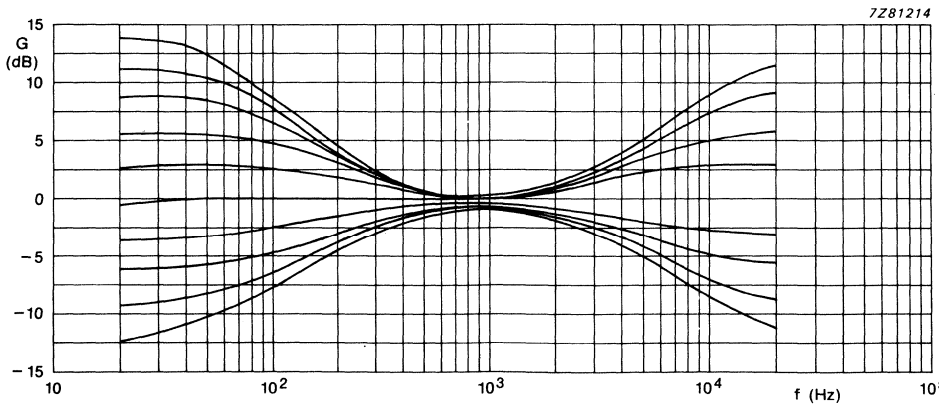
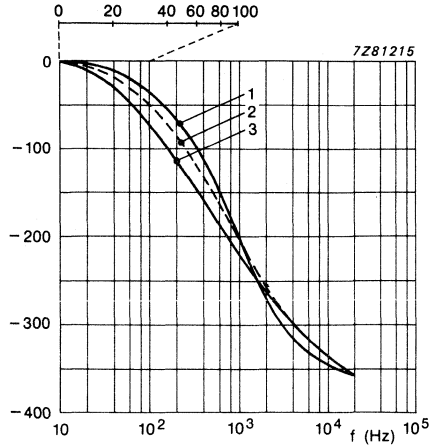


Fig. 14 Bass and treble tone control. C_{bass} = 68 nF, C_{treble} = 3,9 nF.



curve	C_{24} (nF)	C_{25} (nF)	effect
1	15	15	normal
2	5,6	47	intensified
3	5,6	68	more intensified

Fig. 15 Pseudo (phase) as a function of frequency CH1 left.

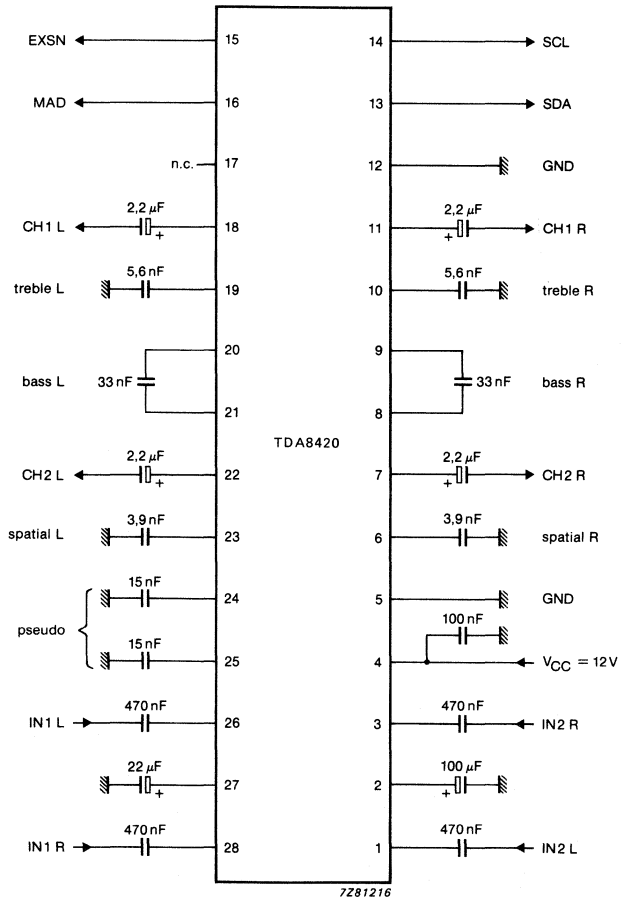
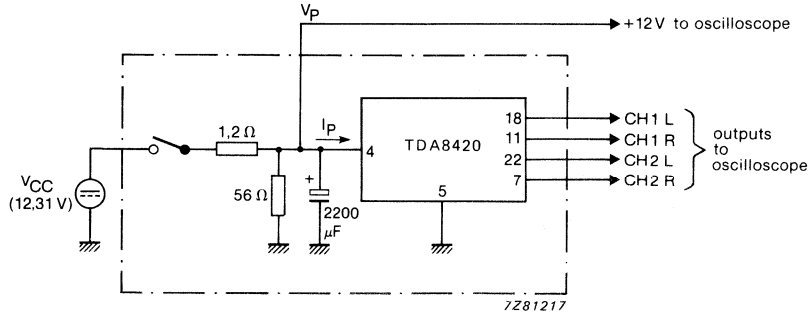


Fig. 16 Test and application circuit diagram.



I_{CC} = 45 mA;
I_{load} = 259 mA;
t_{on} = 2,64 ms;
t_{off} = 102 ms.

Fig. 17 Turn-on/off power supply circuit diagram.

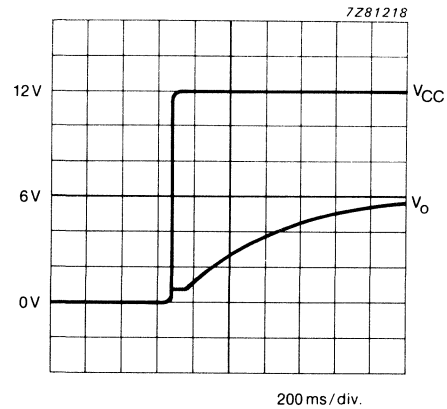


Fig. 18 Turn-on behaviour;
C = 2,2 μF; R_L = 10 kΩ.

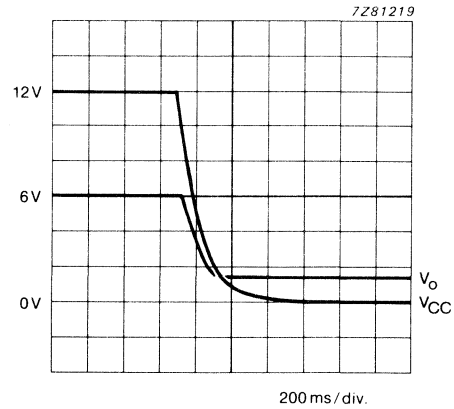


Fig. 19 Turn-off behaviour;
without modulation.

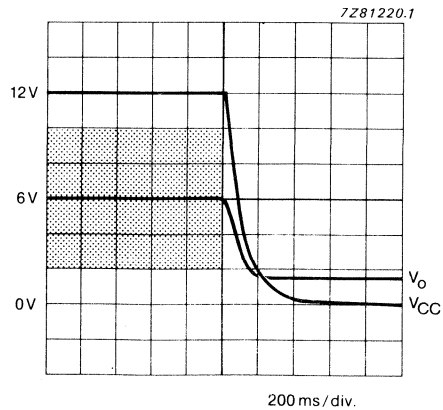


Fig. 20 Turn-off behaviour; with modulation (shaded area).

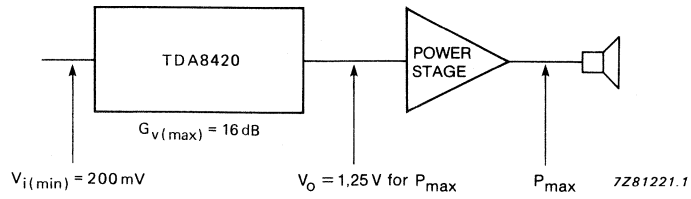


Fig. 21 Level diagram loudspeaker channel CH1 with $V_{i(min)}$ = 200 mV; V_o = 1,25 for P_{max}.

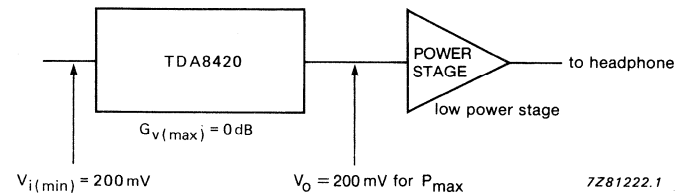


Fig. 22 Level diagram headphone channel CH2 with V_i = 200 mV; V_o = 200 mV for P_{max}.

HI-FI STEREO AUDIO PROCESSOR; I²C BUS

GENERAL DESCRIPTION

The TDA8421 is a monolithic bipolar integrated stereo sound circuit with a loudspeaker channel (CH1) and a headphone channel (CH2), digital controlled via the I²C bus, for application in hi-fi audio and television sound.

Features

- Input selector
- Mode selector
- Loudspeaker channel (CH1) } with volume control, balance control and mute
- Headphone channel (CH2) }
- Pseudo stereo and spatial function
- Bass and treble control
- Electrostatic discharge protection diodes

QUICK REFERENCE DATA

parameter	symbol	min.	typ.	max.	unit
Supply voltage (pin 4)	V_{CC}	7,5	12	14	V
Input signal handling	V_I	2	–	–	V
Input sensitivity full power at the output stage	V_i	–	200	–	mV
Signal plus noise-to-noise ratio	(S+N)/N	–	90	–	dB
Total harmonic distortion	THD	–	0,05	–	%
Channel separation	α	–	75	–	dB
Volume control range CH1	G	–46	–	16	dB
Treble control range	G	–12	–	12	dB
Bass control range	G	–12	–	15	dB
Volume control range CH2	G	–62	–	0	dB

PACKAGE OUTLINE

28-lead dual in-line; plastic (SOT-117).

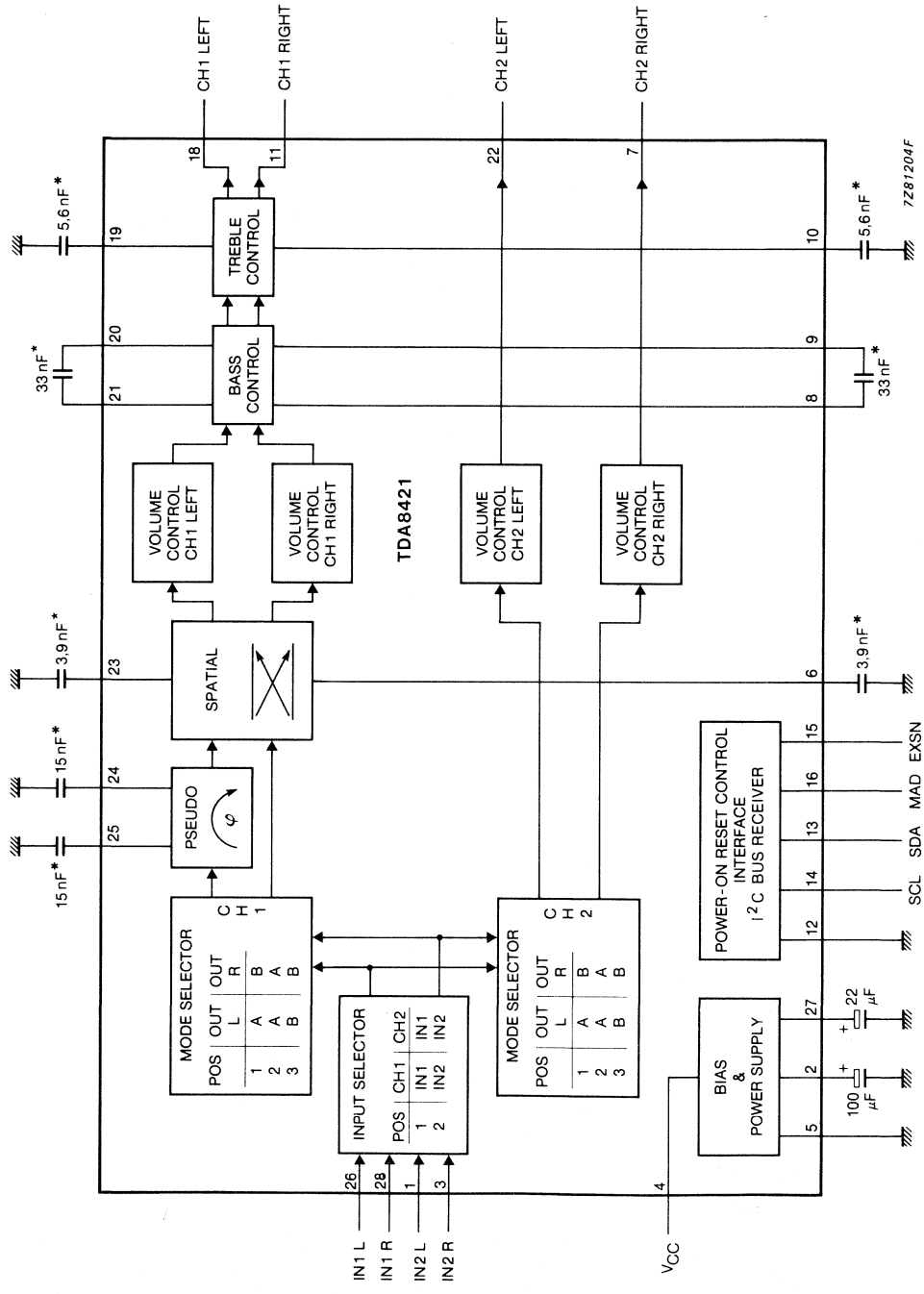


Fig. 1 Block diagram.

* These values are dependent on the required frequency response and effect.

PINNING

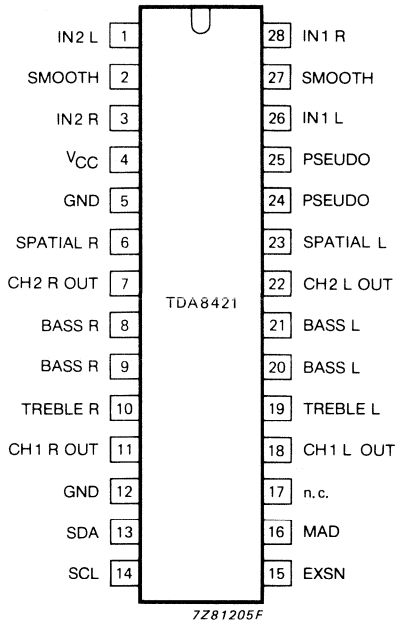


Fig. 2 Pinning diagram.

FUNCTIONAL DESCRIPTION

Input selector

The input to channel 1 (CH1) and channel 2 (CH2) is determined by the input selector. The selection is made from the following AF input signals:

- IN1 L (pin 26); IN1 R (pin 28)
  or
- IN2 L (pin 1); IN2 R (pin 3)

Where IN1 is an internal input signal and IN2 an external input signal.

Mode selector

For each channel (CH1 and CH2) there is a mode selector which selects between stereo, sound A and sound B in the event of bilingual transmission. Both mode selectors can be controlled independently.

Headphone channel (CH2)

Volume control and balance

The stages for volume control for CH2 consist of two parts for left and right. In each part the gain can be adjusted between 0 and −62 dB in steps of 2 dB. An additional step allows an attenuation of $\geqslant$ 90 dB. Both parts can be controlled independently over the whole range, which allows the balance to be varied by controlling the volume of left and right.

Loudspeaker channel (CH1)

Volume control and balance

The loudspeaker channel (CH1) also consists of two parts for volume control (left and right). In each part the gain can be adjusted between + 16 dB and −62 dB in steps of 2 dB. An additional step allows an attenuation of $\geqslant$ 90 dB. Both parts can be controlled independently over the whole range, which allows the balance to be varied by controlling the volume of left and right.

Stereo/pseudo stereo/spatial stereo mode

It is possible to select three modes. Stereo, pseudo or spatial stereo. The pseudo stereo mode receives mono transmissions and the stereo and spatial stereo mode receives stereo transmissions.

Bass control

The bass control stage can be switched from an emphasis of 15 dB to an attenuation of 12 dB for low frequencies in steps of 3 dB.

Treble control

The treble control stage can be switched from + 12 dB to −12 dB in steps of 3 dB.

Bias and power supply

The TDA8421 includes a bias and power supply stage, which generates a voltage of ½ V_{CC} with a low output impedance and injector currents for the logic part.

Power-on reset

The on-chip power-on reset circuit sets the mute bit to active, which mutes both the loudspeaker channel (CH1) and the headphone channel (CH2). The muting can be switched by transmission of the mute bit.

I^2C bus receiver and data handling

Bus specification

The TDA8421 is controlled via the 2-wire I^2C bus by a microcomputer. The two wires (SDA – serial data, SCL – serial clock) carry information between the devices connected to the bus. Both SDA and SCL are bidirectional lines, connected to a positive supply voltage via a pull up resistor.
When the bus is free both lines are HIGH. The data on the SDA line must be stable during the HIGH period of the clock. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW. The set up and hold times are specified in AC CHARACTERISTICS.

A HIGH-to-LOW transition of the SDA line while SCL is HIGH is defined as a start condition.
A LOW-to-HIGH transition of the SDA line while SCL is HIGH is defined as a stop condition.
The bus receiver will be reset by the reception of a start condition. The bus is considered to be busy after the start condition. The bus is considered to be free again after a stop condition.

Module address

Data transmission to the TDA8421 starts with the module address MAD.

MSB								LSB
1	0	0	0	0	0	MAD	R/W	ACK

Fig. 3 TDA8421 module address.

The module address is determined by pin 16. When connected to ground MAD = 0; when connected to V_{CC} MAD = 1. Thus two TDA8421s can be selected within a system.

Subaddress

After the module address byte a second byte is used to select the functions for both channels:

- CH1 – Volume left, volume right, bass, treble and switch functions
- CH2 – Volume left, volume right and switch functions

The subaddress SAD is stored within the TDA8421. Table 1 defines the coding of the second byte after the module address MAD.

Table 1 Second byte after module address MAD

		128	64	32	16	8	4	2	1
	function	MSB 7	6	5	4	3	2	1	LSB 0
CH1	volume left	0	0	0	0	0	0	0	0
	volume right	0	0	0	0	0	0	0	1
	bass	0	0	0	0	0	0	1	0
	treble	0	0	0	0	0	0	1	1
	switch functions	0	0	0	0	1	0	0	0
CH2	volume left	0	0	0	0	0	1	0	0
	volume right	0	0	0	0	0	1	0	1
	switch functions	0	0	0	0	1	1	0	0
						subaddress SAD			

Definition of 3rd byte

A third byte is used to transmit data to the TDA8421. Table 2 defines the coding of the third byte after module address MAD and subaddress SAD.

Table 2 Third byte after module address MAD and subaddress SAD

	function		MSB 7	6	5	4	3	2	1	LSB 0
	volume left	VL1	1	1	V05	V04	V03	V02	V01	V00
	volume right	VR1	1	1	V15	V14	V13	V12	V11	V10
CH1	bass	BA	1	1	1	1	BA3	BA2	BA1	BA0
	treble	TR	1	1	1	1	TR3	TR2	TR1	TR0
	switch functions	S1	1	1	MU	EFL	STL	ML1	ML0	IS
	volume left	VL2	1	1	V25	V24	V23	V22	V21	V20
CH2	volume right	VR2	1	1	V35	V34	V33	V32	V31	V30
	switch functions	S2	1	1	1	1	EXS	MH1	MH0	1

Truth tables

Truth tables for the switch functions

Table 3 Input selector

function	IS
IN1	0
IN2	1

Table 4 Mode selectors

	CH1		CH2	
mode	ML0	ML1	MH0	MH1
stereo	1	1	1	1
sound A	1	0	1	0
sound B	0	1	0	1
----------	0	0	0	0

Table 5 Stereo/pseudo stereo/spatial stereo

choice	STL	EFL
spatial	1	1
stereo	1	0
pseudo	0	1
----------	0	0

Table 6 Mute

mute	MU
active; automatic after POR*	1
not active	0

Table 7 Output for external switch

EXSN	EXS
ground	1
open collector	0

Where: POR = Power-On Reset.

Truth tables for the volume base and treble controls.

Table 8 Volume control

CH1	CH2	V x 5	V x 4	V x 3	V x 2	V x 1	V x 0
16	0	1	1	1	1	1	1
14	−2	.	.	.	.	.	.
.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.
−46	−62	1	0	0	0	0	0
−48	⩽−90	0	1	1	1	1	1
.	.	.	.	.	.	.	.
−62	⩽−90	0	1	1	0	0	0
⩽−90	⩽−90	0	1	0	1	1	1
.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.
⩽−90	⩽−90	0	0	0	0	0	0

Where: The values of CH1 and CH2 are in 2 dB/step measured in dBs.

* Attenuation ⩾ 90 dB

Table 9 Bass control

3dB/step (dB)	BA3	BA2	BA1	BA0
15	1	1	1	1
---	---	---	---	---
---	---	---	---	---
---	---	---	---	---
15	1	0	1	1
12	1	0	1	0
---	---	---	---	---
---	---	---	---	---
---	---	---	---	---
0	0	1	1	0
---	---	---	---	---
---	---	---	---	---
---	---	---	---	---
−12	0	0	1	0
---	---	---	---	---
---	---	---	---	---
---	---	---	---	---
−12	0	0	0	0

Table 10 Treble control

3dB/step (dB)	TR3	TR2	TR1	TR0
12	1	1	1	1
---	---	---	---	---
---	---	---	---	---
---	---	---	---	---
12	1	0	1	0
---	---	---	---	---
---	---	---	---	---
---	---	---	---	---
0	0	1	1	0
---	---	---	---	---
---	---	---	---	---
---	---	---	---	---
−12	0	0	1	0
---	---	---	---	---
---	---	---	---	---
---	---	---	---	---
−12	0	0	0	0

Sequence of data transmission

After a power-on reset all eight functions have to be adjusted with eight data transmissions. It is recommended that data information for switch functions in CH1 are transmitted last because all functions have to be adjusted when the muting is switched off. The sequence of transmission of other data information is not critical.

The order of data transmission is shown in Figures 4 and 5. The number of data transmissions is unrestricted but before each data byte the module address MAD and the correct subaddress SAD is required.

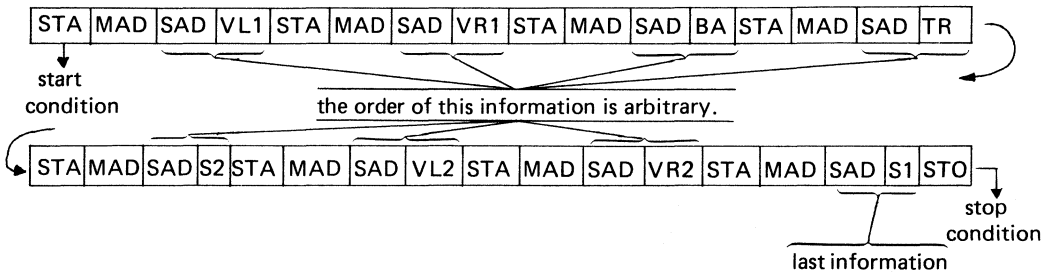


Fig. 4 Data transmission after a power-on reset.

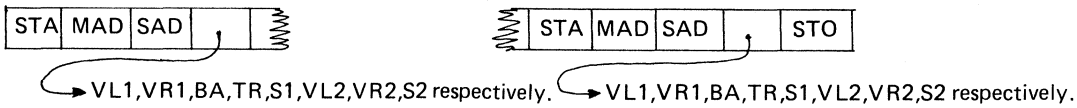


Fig. 5 Data transmission except after power-on reset.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage	V_{CC}	0	16	V
Voltage range at pins for external capacitors				
pins 2, 6, 8 to 10, 19 to 21, 23 to 25, 27	V_{cap}	0	V_{CC}	V
pin 13	V_{SDA}	0	V_{CC}	V
pin 14	V_{SCL}	0	V_{CC}	V
pin 15	V_{EXSN}	0	V_{CC}	V
pin 16	V_{MAD}	0	V_{CC}	V
Voltage range at pins 1, 3, 7, 11, 18, 22, 26, 28	V_I, V_O	0	V_{CC}	V
Output current at pins 7, 11, 18, 22	I_O	–	45	mA
Total power dissipation at $T_{amb} < 70\ ^oC$	P_{tot}	–	1350	mW
Operating ambient temperature range	T_{amb}	0	70	^oC
Storage temperature range	T_{stg}	–25	150	^oC
Electrostatic handling *	$\pm V_{ESD}$	–	2000	V

* Equivalent to discharging a 100 pF capacitor through a 1,5 kΩ resistor.

DC CHARACTERISTICS

V_{CC} = 12 V; T_{amb} = 25 °C; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply voltage (pin 4)	V_{CC}	7,5	12	14	V
Supply current at V_{CC} = 12 V	I_{CC}	–	42	55	mA
Internal input voltage IN1 L,R (pins 26,28) IN2 L,R (pins 1,3) DC voltage internally generated; capacitive coupling recommended	V_I	5,4	6,0	6,6	V
MAD (pin 16)					
input voltage HIGH	V_{IH}	3,0	–	V_{CC}	V
input voltage LOW	V_{IL}	0	–	1,5	V
input current HIGH	I_{IH}	–	–	1,0	μA
input current LOW	I_{IL}	–	1	10	μA
SDA; SCL (pins 13 and 14)					
input voltage HIGH	V_{IH}	3,0	–	V_{CC}	V
input voltage LOW	V_{IL}	−0,3	–	1,5	V
input current HIGH	I_{IH}	–	–	1,0	μA
input current LOW	I_{IL}	–	1	10	μA
Output voltage at CH1 (pins 11 and 18); CH2 (pins 7 and 22)	V_O	5,4	½ V_{CC}	6,6	V
pins with external capacitors					
pins 6 to 10; 19 to 21; 23 to 25	$V_{cap.n}$	–	½ V_{CC}	–	V
pin 2	$V_{cap.2}$	–	V_{CC}−0,1	–	V
External switch (pin 15) at I_{EXSN} = 1 mA					
Output voltage HIGH	V_{EXSNH}	–	–	16	V
Output voltage LOW	V_{EXSNL}	–	–	0,3	V

AC CHARACTERISTICS

V_{CC} = 12 V; bass/treble in linear position; pseudo and spatial stereo off; $R_L > 10\ k\Omega$; $C_L < 100\ pF$; T_{amb} = 25 °C unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
I²C bus timing (see Fig. 6)					
SDA, SCL (pin 13 and 14)					
Clock frequency range	f_{SCL}	0	–	100	kHz
The HIGH period of the clock	t_{HIGH}	4	–	–	μs
The LOW period of the clock	t_{LOW}	4,7	–	–	μs
SCL rise time	t_r	–	–	1	μs
SCL fall time	t_f	–	–	0,3	μs
Set-up time for start condition	$t_{SU;STA}$	4,7	–	–	μs
Hold time for start condition	$t_{HD;STA}$	4	–	–	μs
Set-up time for stop condition	$t_{SU;STO}$	4,7	–	–	μs
Time bus must be free before a new transmission can start	t_{BUF}	4,7	–	–	μs
Set-up time DATA	$t_{SU;DAT}$	250	–	–	ns
Input signals					
IN1 L (pin 26) IN1 R (pin 28) IN2 L (pin 1) IN2 R (pin 3)					
Input signal handling (r.m.s. value) at V_u = −4 dB; THD ⩽ 0,5%	$V_{i(rms)}$	2	–	–	V
Input resistance	R_{n-5}	35	50	–	kΩ
Frequency response (−0,5 dB) bass and treble in linear position; stereo mode; effects off	f	20	–	20 000	Hz

AC CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
LOUDSPEAKER CHANNEL OUTPUTS					
CH1 LEFT (pin 18); CH1 RIGHT (pin 11)					
Output voltage range (r.m.s. value) at THD $\leqslant$ 0,5%	$V_{o(rms)}$	2	–	–	V
Load resistance	R_L	10	–	–	kΩ
Output impedance	Z_O	–	–	100	Ω
Noise level weighted according to CCIR468-2					
gain = 16 dB	V_n	–	90	–	μV
gain = 0 dB	V_n	–	20	40	μV
gain = $\leqslant$ –90 dB	V_n	–	15	–	μV
Total harmonic distortion (f = 20 Hz to 12,5 kHz)					
for $V_{i(rms)}$ = 0,5 V; gain = + 16 dB to –30 dB	THD	–	0,05	0,2	%
for $V_{i(rms)}$ = 1,0 V; gain = + 2 dB to –30 dB	THD	–	0,07	0,2	%
for $V_{i(rms)}$ = 2,0 V; gain = –4 dB to –30 dB	THD	–	0,1	–	%
Channel separation at 10 kHz gain = 0 dB	α_{cr}	–	75	–	dB
Ripple rejection (gain = 0 dB; bass and treble in linear position) f_{ripple} = 100 Hz	RR_{100}	–	50	–	dB
Crosstalk attenuation from logic inputs to AF outputs (gain = 0 dB; bass and treble in linear position)	α_L	–	110	–	dB
VOLUME CONTROL					
For truth table see Table 8					

parameter	symbol	min.	typ.	max.	unit
Loudspeaker channel (CH1)					
Control range at f = 1 kHz					
maximum voltage gain (16 dB step)	G_{max}	15	–	–	dB
minimum voltage gain (–62 dB step)	G_{min}	–60	–	–	dB
last position	G_{off}	–80	–85	–	dB
mute position	G_{mute}	–85	–90	–	dB
Resolution	G_{step}	–	2	–	dB/step
Gain difference between left and right AF channel (note 1)					
gain from 16 dB to –30 dB	ΔG	–	–	0,5	dB
gain from –30 dB to –62 dB	ΔG	–	–	1	dB
TREBLE CONTROL (CH1)					
For truth table see Table 10					
Control range for $C_{10\text{-}5}$; $C_{19\text{-}5}$ = 5,6 nF					
Maximum emphasis at 15 kHz with respect to linear position	G	11	12	13	dB
Maximum attenuation at 15 kHz with respect to linear position	G	11	12	13	dB
Resolution	G_{step}	–	3	–	dB/step
BASS CONTROL					
For truth table see Table 9					
Control range for $C_{8\text{-}9}$; $C_{20\text{-}21}$ = 33 nF					
Maximum emphasis at 40 kHz with respect to linear position	G	14	15	16	dB
Maximum attenuation at 40 kHz with respect to linear position	G	11	12	13	dB
Resolution	G_{step}	–	3	–	dB/step
SPATIAL AND PSEUDO FUNCTION					
Spatial:					
Antiphase crosstalk	α	–	50	–	%
Pseudo:					
Phase shift (see Fig. 15)					

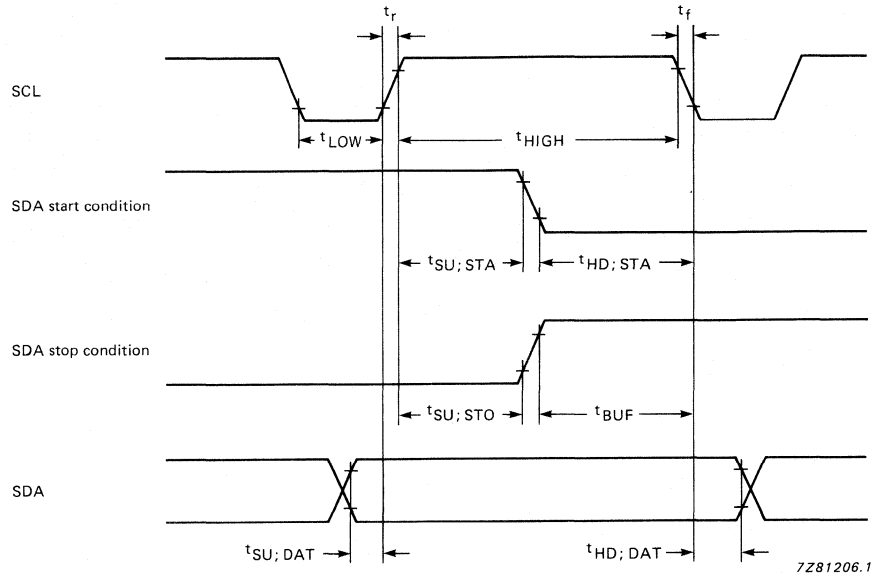
AC CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
HEADPHONE CHANNEL OUTPUTS					
CH2 LEFT (pin 22); CH2 RIGHT (pin 7)					
Output voltage range (r.m.s. value) at THD ≤ 0,5%	$V_{o(rms)}$	2	–	–	V
Load resistance	R_L	10	–	–	kΩ
Output impedance	Z_O	–	–	100	Ω
Noise level (weighted according to CCIR468-2)					
gain = 0 dB	V_n	–	15	–	μV
gain = 16 dB	V_n	–	12	25	μV
gain = ≤ −90 dB	V_n	–	10	–	μV
Total harmonic distortion (f = 20 Hz to 12,5 kHz)					
for $V_{i(rms)}$ = 0,2 V; gain = 0 dB to −30 dB	THD	–	0,01	0,2	%
for $V_{i(rms)}$ = 1,0 V; gain = 0 dB to −30 dB	THD	–	0,1	–	%
for $V_{i(rms)}$ = 2,0 V gain = −4 dB to −30 dB	THD	–	0,3	–	%
Channel separation at 10 kHz gain = 0 dB	α_{cr}	–	75	–	dB
Ripple rejection (gain = 0 dB; bass and treble in linear position) f_{ripple} = 100 Hz	RR_{100}	–	50	–	dB
Crosstalk attenuation from logic inputs to AF outputs (gain = 0 dB; bass and treble in linear position)	α_L	–	110	–	dB
Crosstalk between any input/output f = 100 Hz to 12,5 kHz	α	65	70	–	dB
Crosstalk IN1/IN2 gain = 0 dB; R_G = 0	α	95	100	–	dB

parameter	symbol	min.	typ.	max.	unit
Headphone channel (CH2)					
Control range					
maximum voltage gain (0 dB step)	G_{max}	−1	–	–	dB
minimum voltage gain (−62 dB step)	G_{min}	−57	–	–	dB
last position	G_{off}	−80	−85	–	dB
mute position	G_{mute}	−85	−90	–	dB
Resolution	G_{step}	–	2	–	dB/step
Gain difference between left and right AF channel (note 1)					
gain from 0 dB to −40 dB	ΔG	–	–	0,5	dB
gain from −40 dB to −62 dB	ΔG	–	–	2	dB

Note to the AC characteristics

1. Balance is realized via software by different volume settings in both channels.



$t_{SU;STA}$ = start code set-up time
$t_{HD;STA}$ = start code hold time
$t_{SU;STO}$ = stop code set-up time

t_{BUF} = BUS free time
$t_{SU;DAT}$ = data set-up time
$t_{HD;DAT}$ = DATA hold time

Fig. 6 Timing requirements for I²C bus.

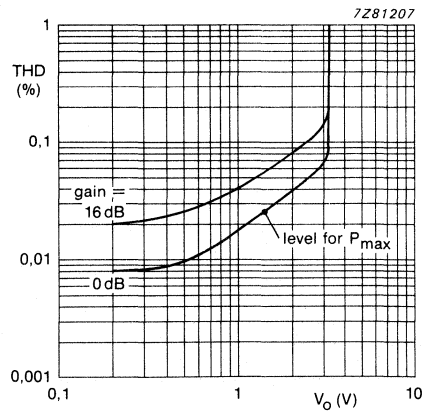


Fig. 7 Distortion loudspeaker channel CH1 as a function of the output voltage with gain as parameter.

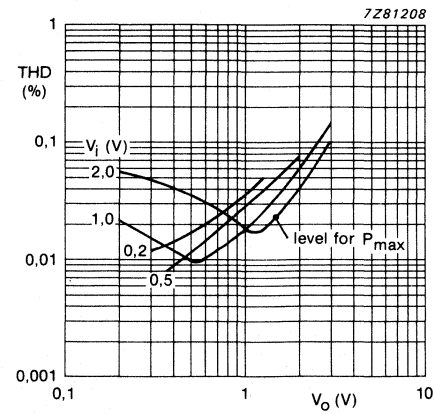


Fig. 8 Distortion loudspeaker channel CH1 as a function of the output voltage with input voltage as parameter.

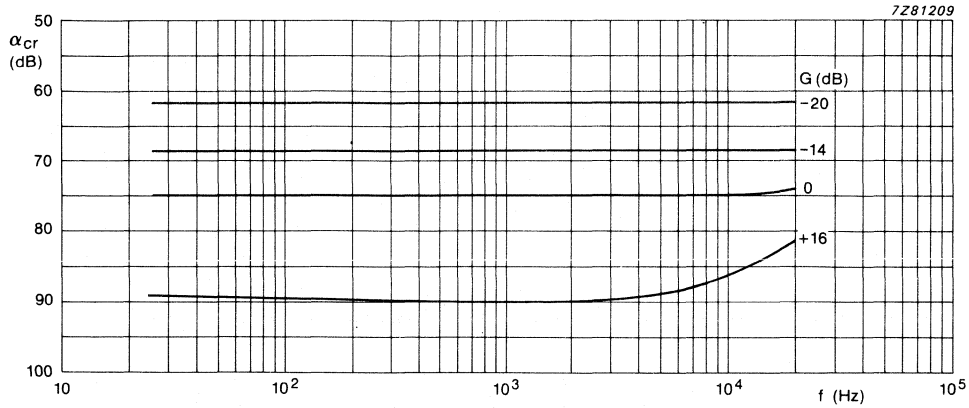


Fig. 9 Channel separation loudspeaker channel CH1 as a function of frequency.

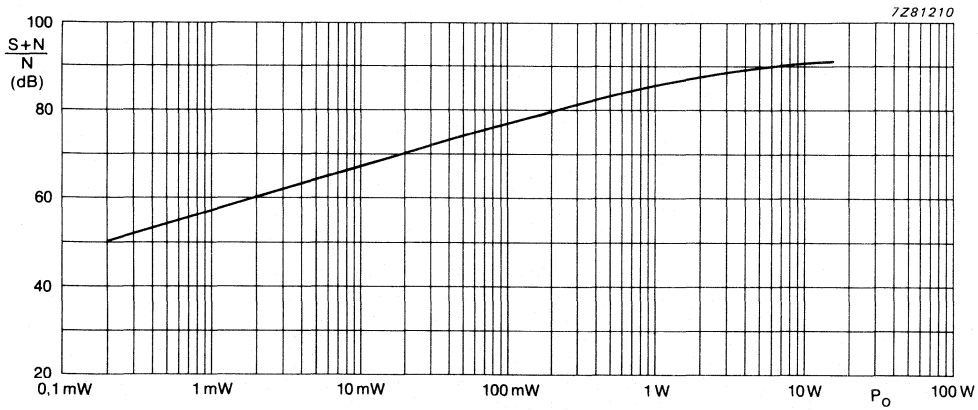


Fig. 10 Signal-to-noise ratio as a function of output power.
Input voltage V_i = 0,5 V; according to CCIR; quasi peak; P_o = 15 W.

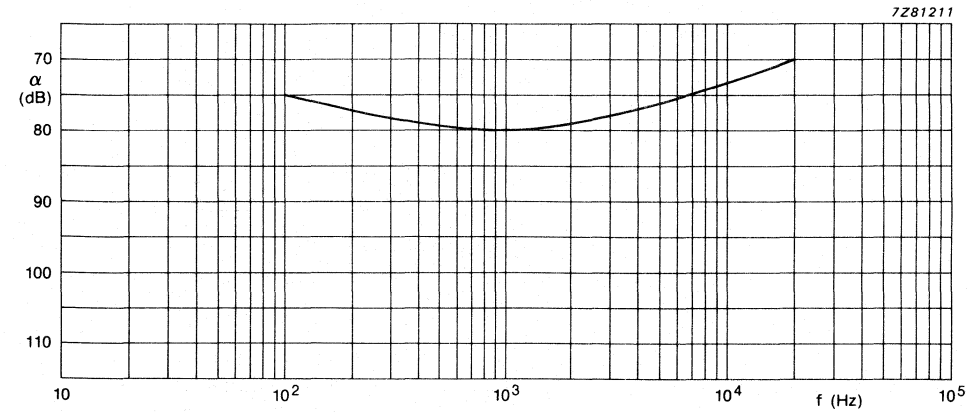


Fig. 11 Crosstalk 2-tone mode as a function of frequency.
CH1: mode AA, Gain + 16 dB; CH2: mode BB, Gain 0 dB. Signal input RIGHT; input LEFT to ground, measured at output CH1.

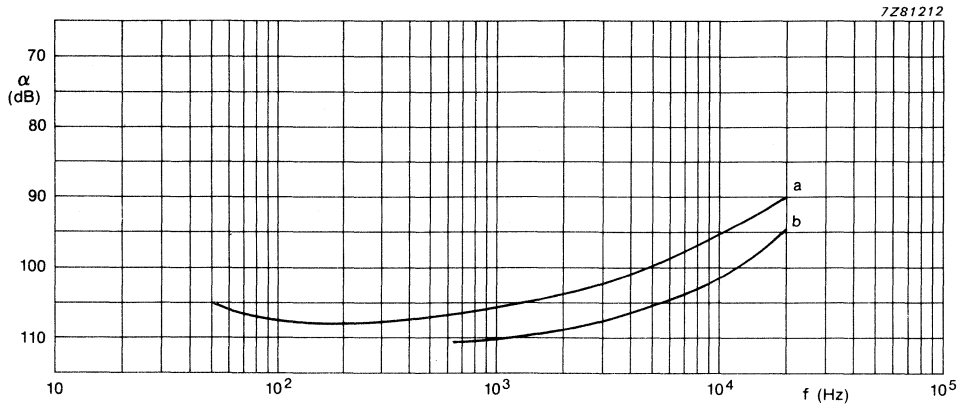


Fig. 12 Crosstalk between IN1 and IN2 as a function of frequency; measured at output CH1, $R_G = 0$.
a) Gain = + 16 dB; V_i = 200 mV. b) Gain = 0 dB; V_i = 1 V.

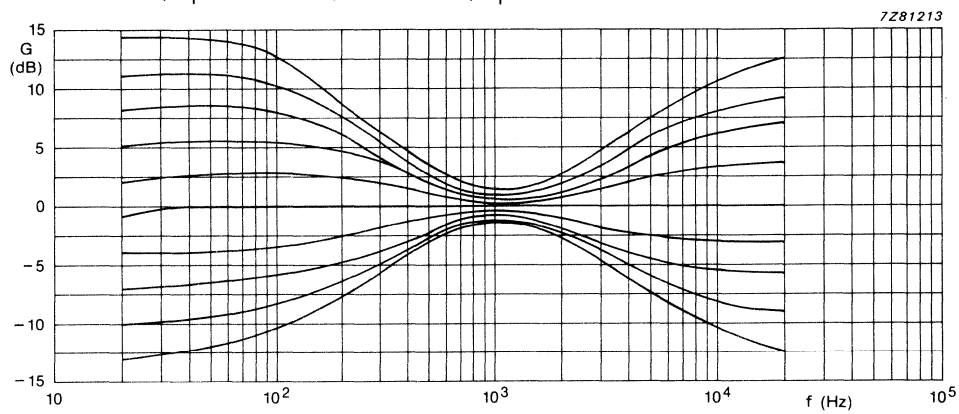


Fig. 13 Bass and treble tone control. C_{bass} = 33 nF, C_{treble} = 5,6 nF.

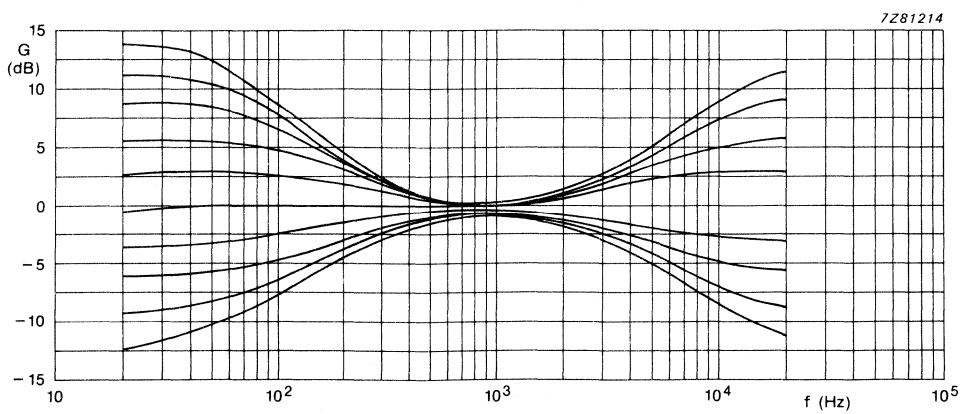
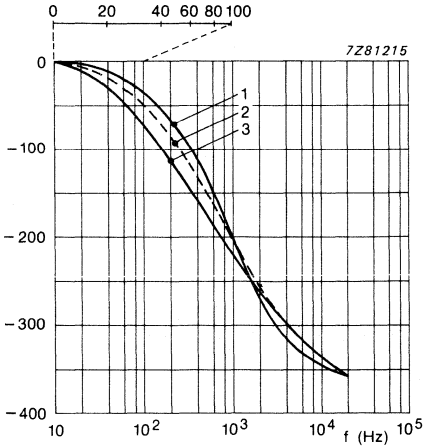


Fig. 14 Bass and treble tone control. C_{bass} = 68 nF, C_{treble} = 3,9 nF.



curve	pin 24 (nF)	pin 25 (nF)	effect
1	15	15	normal
2	5,6	47	intensified
3	5,6	68	more intensified

Fig. 15 Pseudo (phase) as a function of frequency CH1 left.

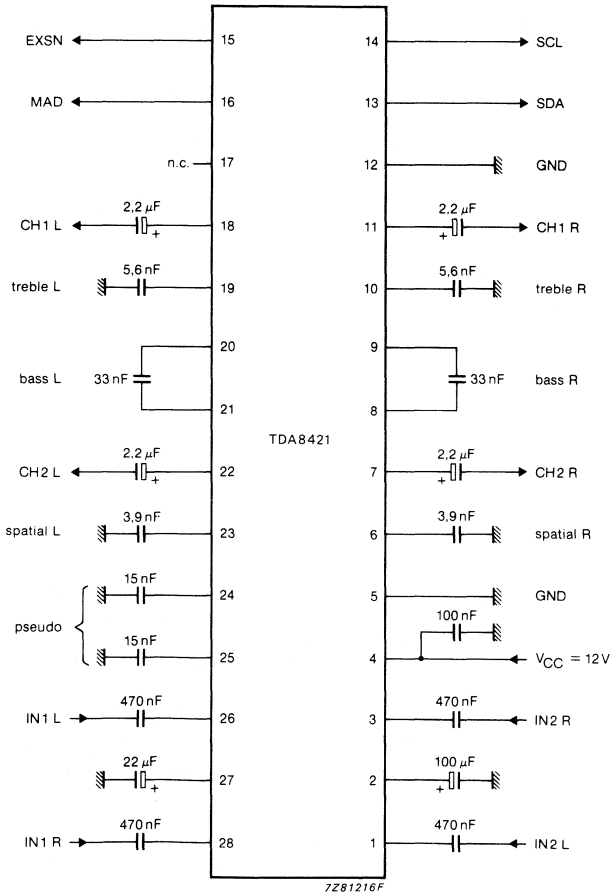
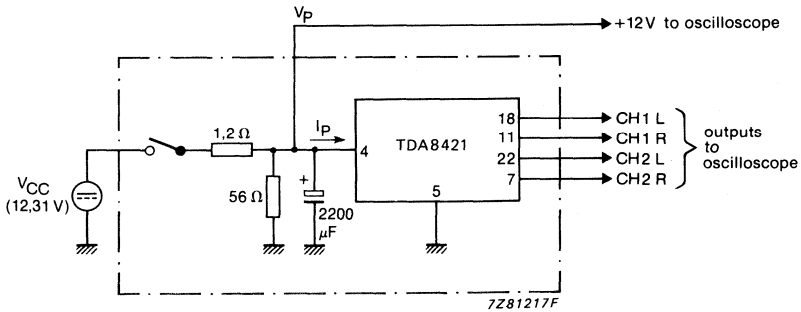


Fig. 16 Test and application circuit diagram.



I_{CC} = 45 mA;
I_{load} = 259 mA;
t_{on} = 2,64 ms;
t_{off} = 102 ms.

Fig. 17 Turn-on/off power supply circuit diagram.

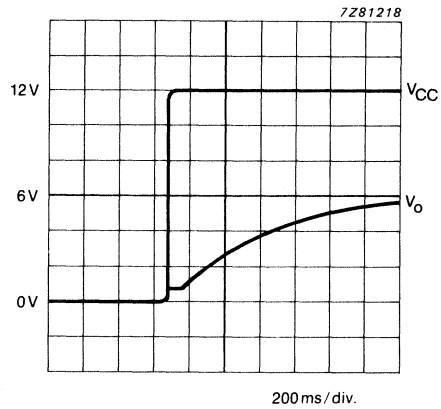


Fig. 18 Turn-on behaviour;
C = 2,2 µF; R_L = 10 kΩ.

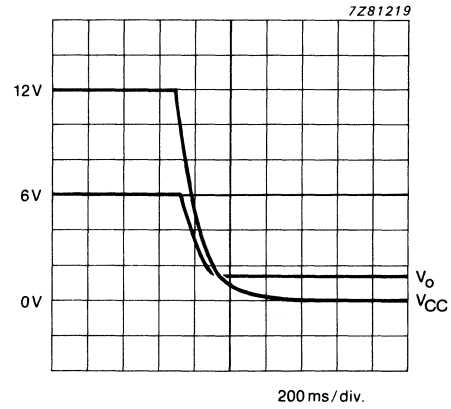


Fig. 19 Turn-off behaviour;
without modulation.

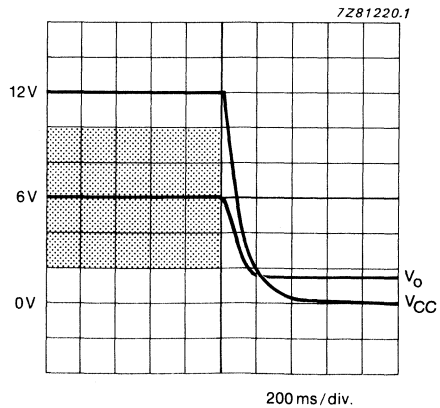


Fig. 20 Turn-off behaviour; with modulation (shaded area).

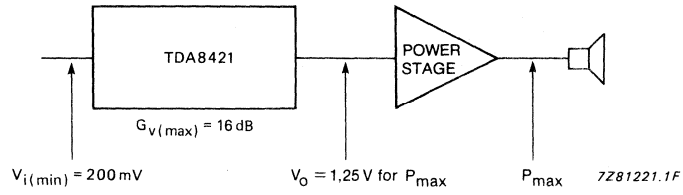


Fig. 21 Level diagram loudspeaker channel CH1 with $V_{i(min)}$ = 200 mV; V_o = 1,25 for P_{max}.

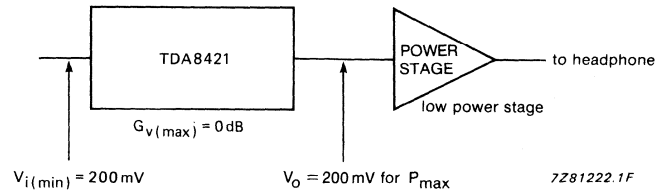


Fig. 22 Level diagram headphone channel CH2 with V_i = 200 mV; V_o = 200 mV for P_{max}.

SWITCH FOR CTV RECEIVERS

GENERAL DESCRIPTION

The TDA8440 is a versatile video/audio switch, intended to be used in CTV receivers equipped with an AUXILIARY VIDEO/AUDIO plug.

It provides two 3-state switches for audio channels and one 3-state switch for the video channel and a video amplifier with selectable gain (times 1 or times 2).

The integrated circuit can be used in conjunction with a microcontroller from the MAB8400 family, and is controlled via a bidirectional I^2C bus. Sufficient sub-addressing is provided for the I^2C bus mode. It can also be controlled directly by d.c. switching signals.

Features

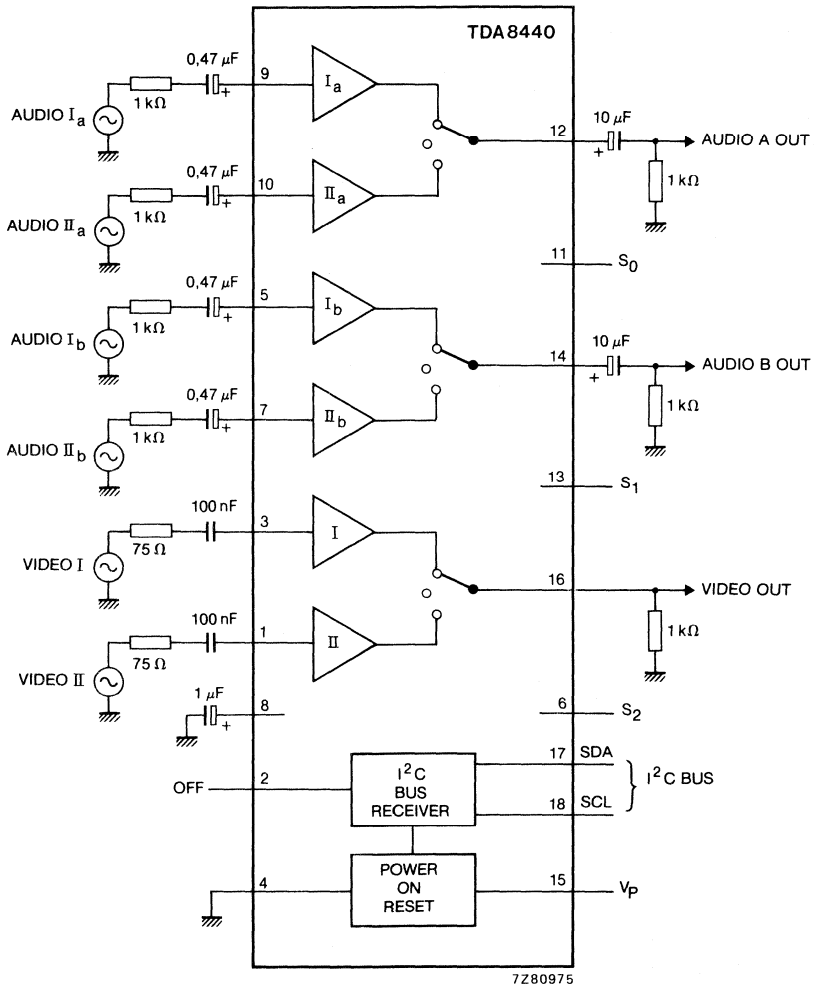
- Combined analogue and digital circuitry gives maximum flexibility in channel switching
- 3-state switches for all channels
- Selectable gain for the video channels
- Sub-addressing facility
- I^2C bus or non-I^2C bus mode (controlled by d.c. voltages)
- Slave receiver in the I^2C bus mode
- External OFF command
- System expansion possible up to 7 devices (14 sources)
- Static short-circuit proof outputs

QUICK REFERENCE DATA

Supply voltage range	V_{15-4}	10 to 13,2	V
Supply current (without load)	I_{15}	typ. 33 max. 50	mA mA
Storage temperature	T_{stg}	max. + 125	°C
Operating ambient temperature range	T_{amb}	0 to + 70	°C

PACKAGE OUTLINE

18-lead DIL; plastic (SOT-102H).



S0, S1, S2 and OFF (pins 11, 13, 6 and 2) connected to V_P or GND.
If more than 1 device is used, then the outputs and the pins 8 (bias decoupling of the audio inputs) mau may be connected in parallel.

Fig. 1 Block diagram and test circuit.

DEVELOPMENT DATA

FUNCTIONAL DESCRIPTION

The TDA8440 is a monolithic system of switches and can be used in CTV receivers equipped with an AUXILIARY VIDEO/AUDIO plug.

The IC incorporates 3-state switches they comprise:

a) An electronic video switch with selectable gain (times 1 or times 2) for switching between an internal video signal (from the IF amplifier) and an AUXILIARY input signal.

b) Two electronic audio switches, for two sound channels (stereo or dual language), for switching between internal audio sources and signals from the AUXILIARY VIDEO/AUDIO plug.

A selection can be made between two input signals and an OFF-state. The OFF-state is necessary if more than one TDA8440 device is used.

The SDA and SCL pins can be connected to the I^2C bus or to d.c. switching voltages. Inputs S_0 (pin 11), S_1 (pin 13), and S_2 (pin 6) are used for selection of sub-addresses or switching to the non-I^2C mode. Inputs S_0, S_1 and S_2 can be connected to the supply voltage (H) or to ground (L). In this way no peripheral components are required for selection.

Table 1 Sub-addressing

			sub-address		
S_2	S_1	S_0	A_2	A_1	A_0
L	L	L	0	0	0
L	L	H	0	0	1
L	H	L	0	1	0
L	H	H	0	1	1
H	L	L	1	0	0
H	L	H	1	0	1
H	H	L	1	1	0
H	H	H	non I^2C addressable		

NON-I^2C BUS CONTROL

If the TDA8440 switching device has to be operated via the AUXILIARY VIDEO/AUDIO plug, inputs S_2, S_1 and S_0 must be connected to the supply line (12 V).

The sources (internal and external) and the gain of the video amplifier can be selected via the SDA and SCL pins with the switching voltage from the AUXILIARY VIDEO/AUDIO plug:

- Sources I are selected if SDA = 12 V (external source)
- Sources II are selected if SDA = 0 V (TV mode)
- Video amplifier gain is 2 x if SCL = 12 V (external source)
- Video amplifier gain is 1 x if SCL = 0 V (TV mode)

If more than one TDA8440 device is used in the non-I^2C bus system, the OFF pin can be used to switch off the desired devices. This can be done via the 12 V switching voltage on the AUXILIARY VIDEO/AUDIO plug.

- All switches are in the OFF position if OFF = H (12 V)
- All switches are in the selected position via SDA and SCL pins if OFF = L (0 V)

I²C BUS CONTROL

Detailed information on the I²C bus is available on request.

Table 2 TDA8440 I²C bus protocol.

STA	A_6	A_5	A_4	A_3	A_2	A_1	A_0	R/W	AC	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	AC	STO

STA = start condition
A_6 = 1
A_5 = 0
A_4 = 0
A_3 = 1
} Fixed address bits
A_2 = sub-address bit, fixed via S_2 input
A_1 = sub-address bit, fixed via S_1 input
A_0 = sub-address bit, fixed via S_0 input
R/W = read/write bit (has to be 0, only write mode allowed)
AC = acknowledge bit (= 0) generated by the TDA8440
D_7 = 1 audio Ia is selected to audio output a
D_7 = 0 audio Ia is not selected
D_6 = 1 audio IIa is selected to audio output a
D_6 = 0 audio IIa is not selected
D_5 = 1 audio Ib is selected to audio output b
D_5 = 0 audio Ib output is not selected
D_4 = 1 audio IIb is selected to audio output b
D_4 = 0 audio IIb is not selected
D_3 = 1 video I is selected to video output
D_3 = 0 video I is not selected
D_2 = 1 video II is selected to video output
D_2 = 0 video II is not selected
D_1 = 1 video amplifier gain is times 2
D_1 = 0 video amplifier gain is times 1
D_0 = 1 OFF-input inactive
D_0 = 0 OFF-input active
STO = stop condition

OFF FUNCTION

With the OFF input all outputs can be switched off (mode high ohmic), depending on the value of D_0.

D_0/OFF gating

D_0	OFF input	Outputs
0 (off input active)	H	OFF
0	L	in accordance with last defined D_7-D_1 (may be entered while OFF = HIGH)
1 (off input inactive)	H	in accordance with D_7-D_1
1	L	in accordance with D_7-D_1

DEVELOPMENT DATA

Power-on reset

The circuit is provided with a power-on reset function.

When the power supply is switched on an internal pulse will be generated that will reset the internal memory S_0, in the initial state all the switches will be in the off position and the OFF input is active (D_7-D_0 = 0) (I^2C mode), position defined via SDA and SCL inputs (non-I^2C mode).

When the power supply decreases below 5 V a pulse will be generated and the internal memory will be reset. The behaviour of the switches will be the same as described above.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

		min.	typ.	max.	unit
Supply voltage	pin 15 V_P	–	–	14	V
Input voltage range	pin 17 V_{SDA}	−0,3	–	V_P + 0,3	V
	pin 18 V_{SCL}	−0,3	–	V_P + 0,3	V
	pin 2 V_{OFF}	−0,3	–	V_P + 0,3	V
	pin 11 V_{S0}	−0,3	–	V_P + 0,3	V
	pin 13 V_{S1}	−0,3	–	V_P + 0,3	V
	pin 6 V_{S2}	−0,3	–	V_P + 0,3	V
Video output current	pin 16 $-I_{16}$	–	–	50	mA
Storage temperature range	T_{stg}	–	–	+ 125	°C
Operating ambient temperature range	T_{amb}	0	–	+ 70	°C
Junction temperature	T_j	–	–	+ 150	°C

THERMAL RESISTANCE

From junction to ambient in free air	$R_{th\ j\text{-}a}$	=	50	K/W

CHARACTERISTICS

T_{amb} = 25 °C; V_P = 12 V; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply					
Supply voltage	$V_{15\text{-}4}$	10	–	13,2	V
Supply current (without load)	I_{15}	–	37	50	mA
Video switch					
Input coupling capacitor	C_1C_3	100	–	–	nF
Voltage gain (times 1; SLC = L)	$A_{3\text{-}16}$	−1	0	+ 1	dB
(times 2; SCL = H)	$A_{3\text{-}16}$	+5	+ 6	+ 7	dB
Voltage gain (times 1; SCL = L)	$A_{1\text{-}16}$	−1	0	+ 1	dB
(times 2; SCL = H)	$A_{1\text{-}16}$	+5	+ 6	+ 7	dB
Input video signal amplitude (gain times 1)	$V_{3\text{-}4}$	–	–	4,5	V
Input video signal amplitude (gain times 1)	$V_{1\text{-}4}$	–	–	4,5	V
Output impedance	$Z_{16\text{-}4}$	–	7	–	Ω
Output impedance in 'OFF' state	$Z_{16\text{-}4}$	100	–	–	kΩ
Isolation (off state) (f_o = 5 MHz)		60	–	–	dB
Signal-to-noise ratio (note 2)	S/S + N	60	–	–	dB
Output top-sync level	$V_{16\text{-}4}$	2,4	2,8	3,2	V
Differential gain	G	–	–	3	%
Minimum crosstalk attenuation (note 1)	$V_{16\text{-}4}$	60	–	–	dB
Supply voltage rejection (note 3)	RR	36	–	–	dB
Bandwidth (1 dB)	B	10	–	–	MHz
Crosstalk attenuation for interference caused by bus signals (source impedance 75 Ω)	α	60	–	–	dB
Audio switch a and b					
Input signal level	$V_{9\text{-}4(rms)}$	–	–	2	V
	$V_{10\text{-}4(rms)}$	–	–	2	V
	$V_{5\text{-}4(rms)}$	–	–	2	V
	$V_{7\text{-}4(rms)}$	–	–	2	V
Input impedance	$Z_{9\text{-}4}$	50	100	–	kΩ
	$Z_{10\text{-}4}$	50	100	–	kΩ
	$Z_{5\text{-}4}$	50	100	–	kΩ
	$Z_{7\text{-}4}$	50	100	–	kΩ
Output impedance	$Z_{12\text{-}4}$	–	–	10	Ω
	$Z_{14\text{-}4}$	–	–	10	Ω
Output impedance (off state)	$Z_{14\text{-}4}$	100	–	–	kΩ

parameter	symbol	min.	typ.	max.	unit
Voltage gain	$V_{9\text{-}12}$	−1	0	+ 1	dB
	$V_{10\text{-}12}$	−1	0	+ 1	dB
	$V_{5\text{-}14}$	−1	0	+ 1	dB
	$V_{7\text{-}14}$	−1	0	+ 1	dB
Isolation (off state) (f = 20 kHz)		90	–	–	dB
Signal-to-noise ratio (note 4)	S/S + N	90	–	–	dB
Total harmonic distortion (note 6)	THD	–	–	0,1	%
Crosstalk attenuation for interferences caused by video signals (note 5)					
Weighted	α	80	–	–	dB
Unweighted	α	80	–	–	dB
Crosstalk attenuation for interferences caused by sinusoidal sound signals (note 5)	α	80	–	–	dB
Crosstalk attenuation for interferences caused by the bus signal (weighted) (source impedance = 1 kΩ)		80	–	–	dB
Supply voltage rejection	RR	50	–	–	dB
Bandwidth (−1 dB)	B	50	–	–	kHz
I^2C bus inputs/outputs SDA (pin 17) and SCL (pin 18)					
Input voltage HIGH	V_{IH}	3	–	V_P	V
Input voltage LOW	V_{IL}	−0,3	–	+ 1,5	V
Input current HIGH*	I_{IH}	–	–	10	μA
Input current LOW*	I_{IL}	–	–	10	μA
Output voltage LOW at I_{OL} = 3 mA	V_{OL}	–	–	0,4	V
Maximum output sink current	I_{OL}	–	5	–	mA
Capacitance of SDA and SDL inputs, pins 17 and 18	C_I	–	–	10	pF
Sub-address inputs S_0 (pin 11), S_1 (pin 13), S_2 (pin 6)					
Input voltage HIGH	V_{IH}	3	–	V_P	V
Input voltage LOW	V_{IL}	−0,3	–	+ 0,4	V
Input current HIGH	I_{IH}	–	–	10	μA
Input current LOW	I_{IL}	−50	–	0	μA
OFF input (pin 2)					
Input voltage HIGH	V_{IH}	+3	–	V_P	V
Input voltage LOW	V_{IL}	−0,3	–	+ 0,4	V
Input current HIGH	I_{IH}	–	–	20	μA
Input current LOW	I_{IL}	−10	–	2	μA

* Also if the supply is switched off.

DEVELOPMENT DATA

CHARACTERISTICS (continued)

I^2C bus load conditions are as follows:
4 kΩ pull-up resistor to + 5 V; 200 pF to GND.
All values are referred to V_{IH} = 3 V and V_{IL} = 1,5 V.

parameter	symbol	min.	typ.	max.	unit
Bus free before start	t_{BUF}	4	–	–	μs
Start condition set-up time	$t_{s(STA)}$	4	–	–	μs
Start condition hold time	$t_{h(STA)}$	4	–	–	μs
SCL, SDA LOW period	t_{LOW}	4	–	–	μs
SCL, SDA HIGH period	t_{HIGH}	4	–	–	μs
SCL, SDA rise time	t_r	–	–	1	μs
SCL, SDA fall time	t_f	–	–	0,3	μs
Data set-up time (write)	$t_{s(DAT)}$	1	–	–	μs
Data hold time (write)	$t_{h(DAT)}$	1	–	–	μs
Acknowledge (from TDA8440) set-up time	$t_{s(CAC)}$	–	–	2	μs
Acknowledge (from TDA8440) hold time	$t_{h(CAC)}$	0	–	–	μs
Stop condition set-up time	$t_{s(STO)}$	4	–	–	μs

Notes to the characteristics

1. Caused by drive on any other input at maximum level, measured in B = 5 MHz, source impedance for the used input 75 Ω,

   $$\text{crosstalk} = 20 \log \frac{V_{out}}{V_{IN\ max}}.$$

2. $$S/N = 20 \log \frac{V_O \text{ video noise (p-p) (2 V)}}{V_O \text{ noise rms B = 5 MHz}}.$$

3. $$\text{Supply voltage ripple rejection} = 20 \log \frac{V_r \text{ supply}}{V_r \text{ on output}} \text{ at f = max. 100 kHz.}$$

4. $$S/N = 20 \log \frac{V_O \text{ nominal (0,5 V)}}{V_O \text{ noise B = 20 kHz}}.$$

5. Caused by drive of any other input at maximum level, measured in B = 20 kHz, source impedance of the used input = 1 kΩ,

   $$\text{crosstalk} = 20 \log \frac{V_{out}}{V_{in\ max}}$$ according to DIN 45405 (CCIR 468).

6. f = 20 Hz to 20 kHz.
7. All outputs are short-circuit proof (static).
8. The inputs and output (apart from SDA, SCL and OFF) withstand tests of MIL-STD-883 C. It is advisable to connected series resistors to these pins.
9. Timings $t_{S,\ DAT}$ and $t_{H,\ DAT}$ deviate from the I^2C bus specification. After reset has been activated, transmission may only be started after a 50 μs delay.

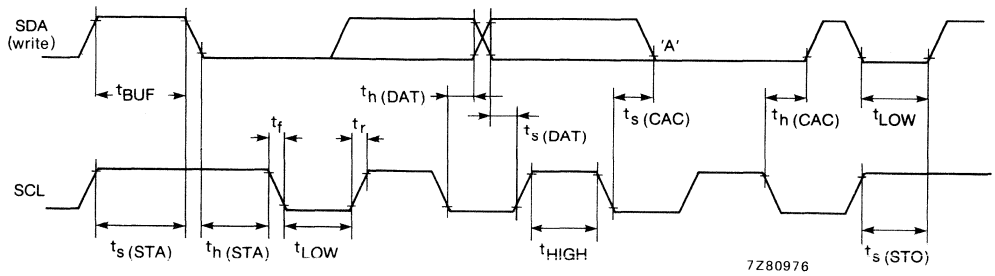


Fig. 2 Timing diagram I^2C bus.

DEVELOPMENT DATA

I²C BUS INTERFACE FOR COLOUR DECODERS

GENERAL DESCRIPTION

The TDA8442 provides control of four analogue functions and has one high-current and two switching outputs. Control of the IC is performed via the two-line, bidirectional I²C bus.

Features

- Four analogue control outputs
- One high-current output port (npn open emitter)
- Two switching output ports (npn collector with internal pull-up resistor)
- I²C bus slave receiver
- Power-down reset

QUICK REFERENCE DATA

Supply voltage	$V_P = V_{9-8}$	typ.	12 V
Supply current (no outputs loaded)	$I_P = I_9$	typ.	13 mA
Total power dissipation (no outputs loaded)	P_{tot}	max.	1 W
Operating ambient temperature range	T_{amb}		−20 to +70 °C

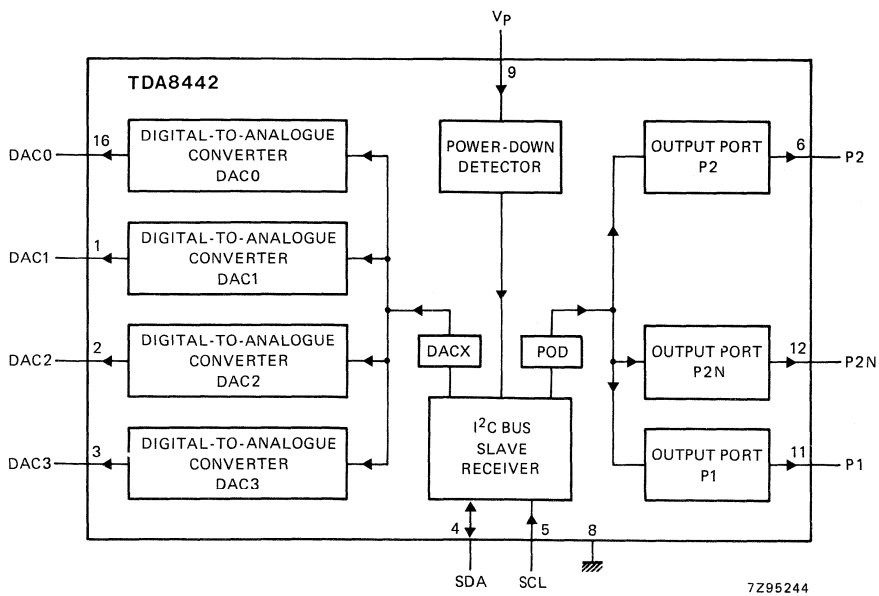


Fig. 1 Block diagram.

PACKAGE OUTLINE

16-lead DIL; plastic (SOT-38).

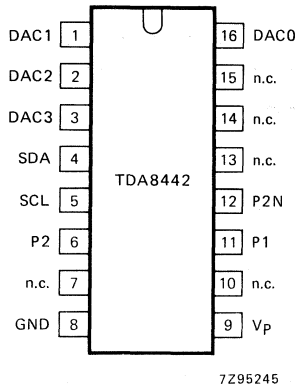


Fig. 2 Pinning diagram.

PINNING

1	DAC1	analogue output 1
2	DAC2	analogue output 2
3	DAC3	analogue output 3
4	SDA	serial data line } I^2C bus
5	SCL	serial clock line } I^2C bus
6	P2	port 2 npn collector output with internal pull-up resistor
7	n.c.	not connected
8	GND	supply return (ground)
9	V_P	positive supply voltage
10	n.c.	not connected
11	P1	port 1 open npn emitter output
12	P2N	inverted P2 output
13	n.c.	not connected
14	n.c.	not connected
15	n.c.	not connected
16	DAC0	analogue output 0

FUNCTIONAL DESCRIPTION

Control

Analogue control is facilitated by four 6-bit digital-to-analogue converters (DAC0 to DAC3). The values of the output voltages from the DACs are set via the I^2C bus.

The high-current output port (P1) is suitable for switching between internal and external RGB signals. It is an open npn emitter output capable of sourcing 14 mA (minimum).

The two output ports (P2 and P2N) can be used for NTSC/PAL switching. These are npn collector outputs with internal pull-up resistors of 10 kΩ (typical). Both outputs are capable of sinking up to 2 mA with a voltage drop of less than 400 mV. If one output is switched on (LOW), the the other output is switched off, and vice versa.

Reset

The power-down-reset mode occurs whenever the positive supply voltage falls below 8,5 V (typical) and resets all registers to a defined state.

OPERATION

Write

The TDA8442 is controlled via the I²C bus (specifications for the I²C bus will be supplied on request). Programming of the TDA8442 is performed using the format shown in Fig. 3.

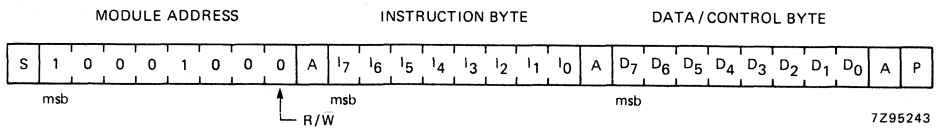
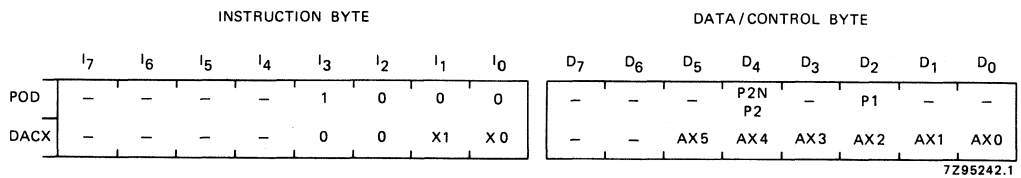


Fig. 3 TDA8442 programming format.

Acknowledge (A) is generated by the TDA8442 only when a valid address is received and the device is not in the power-down-reset mode ($V_P > 8{,}5$ V (typ)).

Control

Control is implemented by the instruction bytes POD (port output data) and DACX (digital-to-analogue convertor control) together with the corresponding data/control bytes (see Fig. 4).



– = don't care

Fig. 4 Control programming.

POD bit P1. If a '1' is programmed, the P1 output is switched on. If a '0' is programmed or after a power-down-reset, the P1 output is switched off (high-impedance state).

POD bit P2/P2N. If a '1' is programmed, the P2 output is switched off and the P2N output is switched on (LOW). If a '0' is programmed, or after a power-down-reset, the P2 output is switched on (LOW) and the P2N output is switched off.

DAX bits AX5 to AX0. The digital-to-analogue convertor selected corresponds to the decimal equivalent of the two bits X1 and X0. The output voltage of the selected DAC is programmed using bits AX5 to AX0, the lowest value being with all data AX5 to AX0 at '0' or when power-down-reset has been activated.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range (pin 9)	V_P	−0,3 to +13,2 V
Input/output voltage ranges		
(pin 4)	V_{SDA}	−0,3 to +13,2 V
(pin 5)	V_{SCL}	−0,3 to +13,2 V
(pin 6)	V_{P2}	−0,3 to V_P* V
(pin 12)	V_{P2N}	−0,3 to V_P* V
(pin 11)	V_{P1}	−0,3 to V_P* V
(pins 1 to 3 and pin 16)	V_{DAX}	−0,3 to V_P* V
Total power dissipation	P_{tot}	max. 1 W
Operating ambient temperature range	T_{amb}	−20 to +70 °C
Storage temperature range	T_{stg}	−55 to +125 °C

CHARACTERISTICS

T_{amb} = +25 °C; V_P = 12 V; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supplies					
Supply voltage (pin 9)	V_P	10,8	12,0	13,2	V
Supply currents (no outputs loaded) (pin 9)	I_P	6,5	13	20	mA
I²C bus inputs SDA (pin 4) **and SCL** (pin 5)					
Input voltage HIGH (note 1)	V_{IH}	3,0	–	V_P−1	V
Input voltage LOW	V_{IL}	−0,3	–	1,5	V
Input current HIGH (note 1)	I_{IH}	–	–	10	μA
Input current LOW (note 1)	I_{IL}	–	–	10	μA
I²C bus output SDA (pin 4) (open collector)					
Output voltage LOW at I_{OL} = 3,0 mA	V_{OL}	–	–	0,4	V
Maximum output sink current	I_{OL}	3	5	–	mA

* Pin voltage may exceed V_P if the current in that pin is limited to 10 mA.

parameter	symbol	min.	typ.	max.	unit
Ports P2 and P2N (pins 6 and 12) (npn collector output with pull-up resistor to V_P)					
Internal pull-up resistor to V_P	R_O	5	10	15	kΩ
Output voltage switched on (LOW) at I_{OL} = 2 mA	V_{OL}	–	–	0,4	V
Maximum output sink current	I_{OL}	2	5	–	mA
Leakage current output switched off	$-I_{leak}$	–	–	25	μA
Port P1 (pin 11) (open npn emitter output)					
Output current switched on V_O = 0 to 5 V	I_O	14	–	–	mA
Leakage current switched off V_O = 0 to V_P V	$\pm I_{leak}$	–	–	100	μA
Digital-to-analogue outputs (note 2)					
Output DAC0 (pin 16)					
Maximum output voltage (unloaded) (note 3)	V_{Omax}	3,0	–	–	V
Minimum output voltage (unloaded) (note 3)	V_{Omin}	–	–	1,0	V
Positive value of smallest step at I_O = 2 mA (1 lsb) (note 3)	V_{Olsb}	24	–	100	mV
Deviation from linearity at I_O = 2 mA	ΔV	–	–	150	mV
Output impedance at I_O = –2 to + 2 mA	Z_O	–	–	70	Ω
Maximum output source current	$-I_{OH}$	2	–	6,0	mA
Maximum output sink current	I_{OL}	2	8	–	mA
Output DAC1 (pin 1)					
Maximum output voltage (unloaded) (note 3)	V_{Omax}	4,0	–	–	V
Minimum output voltage (unloaded) (note 3)	V_{Omin}	–	–	1,7	V
Positive value of smallest step at I_O = 2 mA (1 lsb) (note 3)	V_{Olsb}	27	–	120	mV
Deviation from linearity at I_O = 2 mA		–	–	170	mV
Output impedance at I_O = –2 to + 2 mA	Z_O	–	–	70	Ω
Maximum output source current	$-I_{OH}$	2	–	6,0	mA
Maximum output sink current	I_{OL}	2	8	–	mA

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Output DAC2 (pin 2)					
Maximum output voltage (unloaded) (note 3)	V_{Omax}	4,0	–	–	V
Minimum output voltage (unloaded) (note 3)	V_{Omin}	–	–	1,7	V
Positive value of smallest step at I_O = 2 mA (1 lsb) (note 3)	V_{Olsb}	27	–	120	mV
Deviation from linearity at I_O = 2 mA		–	–	170	mV
Output impedance at I_O = −2 to + 2 mA	Z_O	–	–	70	Ω
Maximum output source current	$-I_{OH}$	2	–	6,0	mA
Maximum output sink current	I_{OL}	2	8	–	mA
Output DAC3 (pin 3)					
Maximum output voltage (unloaded) (note 3)	V_{Omax}	10,0	–	–	V
Minimum output voltage (unloaded) (note 3)	V_{Omin}	–	–	1,0	V
Positive value of smallest step at I_O = 2 mA (1 lsb) (note 3)	V_{Olsb}	107	–	350	mV
Deviation from linearity at I_O = 2 mA		–	–	0,50	V
Output impedance at I_O = −2 to + 2 mA	Z_O	–	–	70	Ω
Maximum output source current	$-I_{OH}$	2	–	6,0	mA
Maximum output sink current	I_{OL}	2	8	–	mA
Power-down reset					
Maximum value of V_P at which power-down reset is active	V_{PD}	6	–	10	V
Rise time of V_P during power-on (V_P rising from 0 V to V_{PD})	t_r	5	–	–	μs

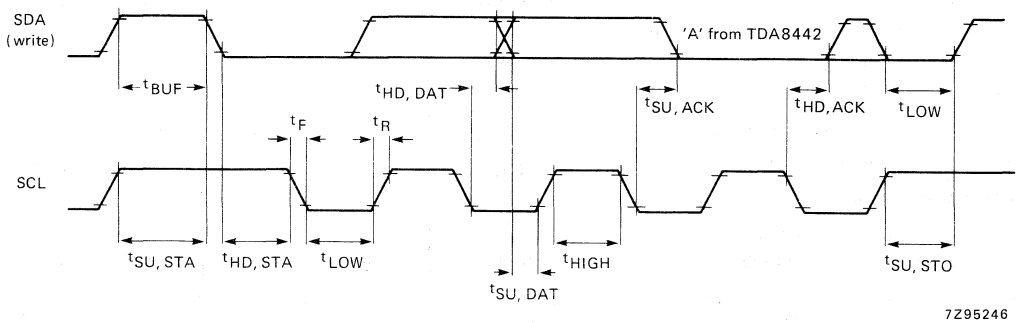
Notes to the characteristics

1. If $V_P < 1$ V, the input current is limited to 10 μA at input voltages up to 13,2 V.
2. Pure capacitive load should be avoided because of possible oscillations.
3. Values are proportional to V_P.

I²C BUS TIMING

Bus loading conditions: 4 kΩ pull-up resistor to +5 V; 200 pF capacitor to GND.
All values are referred to V_{IH} = 3 V and V_{IL} = 1,5 V.

parameter	symbol	min.	typ.	max.	unit
Bus free before start	t_{BUF}	4,0	–	–	μs
Start condition set-up time	$t_{SU,STA}$	4,0	–	–	μs
Start condition hold time	$t_{HD,STA}$	4,0	–	–	μs
LOW period SCL, SDA	t_{LOW}	4,0	–	–	μs
HIGH period SCL	t_{HIGH}	4,0	–	–	μs
Rise time SCL, SDA	t_R	–	–	1,0	μs
Fall time SCL, SDA	t_F	–	–	0,30	μs
Data set-up time (write)	$t_{SU,DAT}$	1	–	–	μs
Data hold time (write)	$t_{HD,DAT}$	1	–	–	μs
Acknowledge (from TDA8442) set-up time	$t_{SU,ACK}$	–	–	3,5	μs
Acknowledge (from TDA8442) hold time	$t_{HD,ACK}$	0	–	–	μs
Stop condition set-up time	$t_{SU,STO}$	4,0	–	–	μs



Reference levels are 10 and 90%

Fig. 5 I²C bus timing, TDA8442.

I²C BUS CONTROLLED YUV/RGB INTERFACE CIRCUIT

GENERAL DESCRIPTION

The TDA8443 and TDA8443A are intended for use in a colour television receiver equipped with a peritelevision connector, for switching and matrixing of external RGB and interval YUV signals. The ICs are controlled by an I²C bus, such as the MAB8400 family, with seven sub-addresses or they can be used in a non-I²C bus mode. In the non-I²C bus mode, control of the circuit is achieved by d.c. voltages. The difference between the two circuits is the output level (TDA8443A is designed for use with standard decoder levels and the TDA8443 is designed for use with computer controlled television levels).

Features

- Two RGB/YUV selectable clamped inputs with associated synchronization
- RGB/YUV matrix
- Tree state switching with an OFF-state
- Four amplifiers with selectable gain
- I²C bus or non-I²C bus mode
- Slave receiver in the I²C bus mode
- External OFF command
- Expansible system (upto seven devices)
- Fast switching to allow for mixed modes

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage	V_{18-22}	V_P	10,8	12,0	13,2	V
Supply current	I_{18}	I_P	–	65	90	mA
Operating ambient temperature range		T_{amb}	0	–	+ 70	°C
Output impedance		$\lvert Z_{19-22}\rvert$ $\lvert Z_{20-22}\rvert$ $\lvert Z_{21-22}\rvert$	–	7	30	Ω
3 dB bandwidth	mode 0 or 2		–	25	–	MHz
3 dB bandwidth	mode 1		–	10	–	MHz
Maximum output amplitude of YUV signal (peak-to-peak value)	gain x 1		2,1	–	–	V
	gain x 2		4,2	–	–	V

PACKAGE OUTLINE

24-lead DIL; plastic (with internal heat spreader)(SOT-101B).

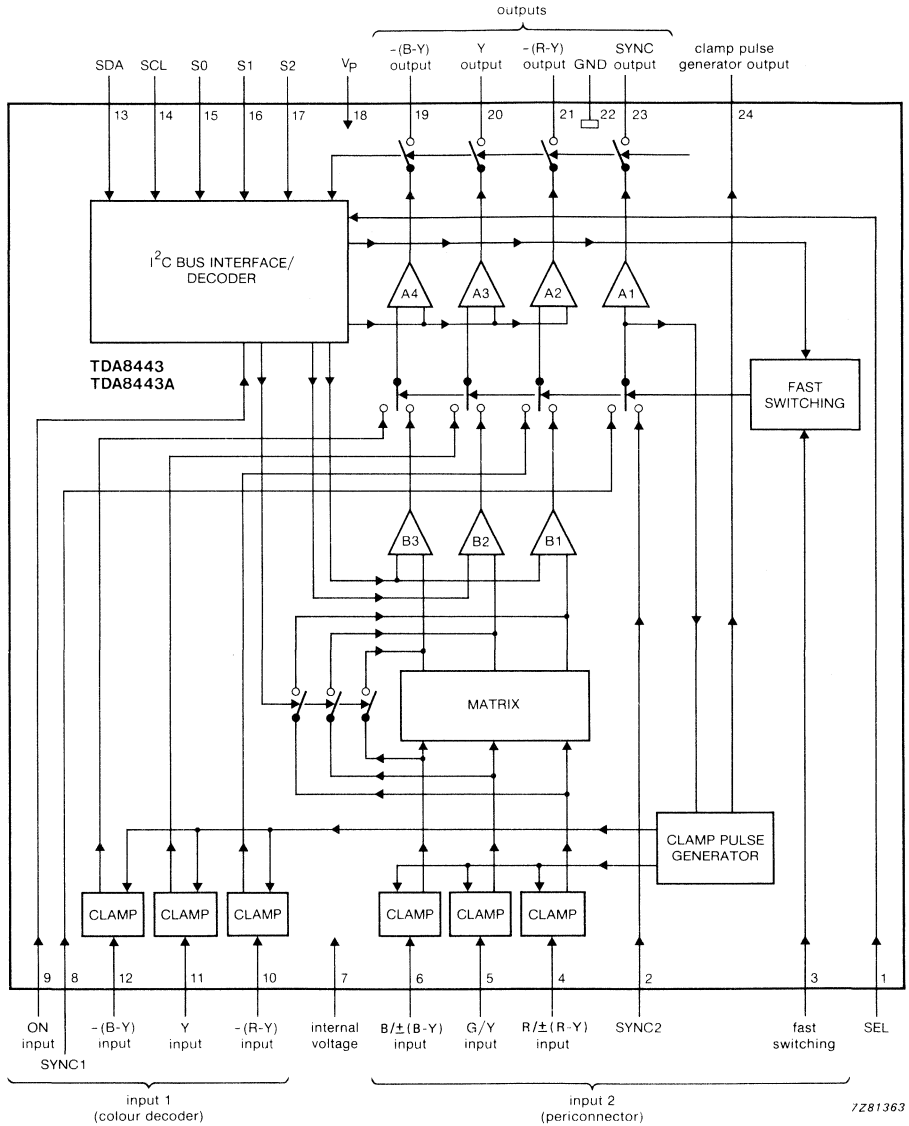


Fig. 1 Block diagram.

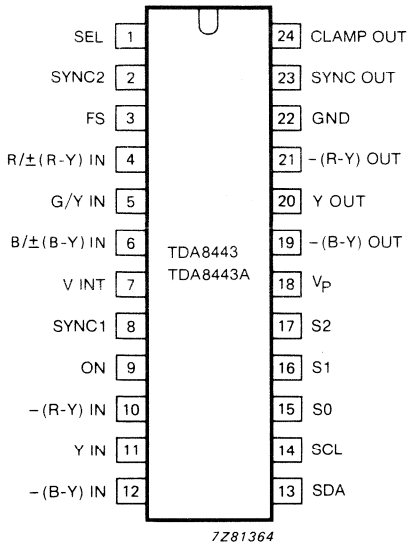


Fig. 2 Pinning diagram.

PINNING

1	SEL	select
2	SYNC2	synchronization input from the periconnector
3	FS	fast switching
4	R/±(R-Y) IN	R or (R-Y) input
5	G/Y IN	G or Y input
6	B/±(B-Y) IN	B or (B-Y) input
7	V INT	internal voltage supply
8	SYNC1	synchronization input from a standard colour decoder
9	ON	ON input
10	−(R-Y) IN	−(R-Y) input signal
11	Y IN	Y input signal
12	−(B-Y) IN	−(B-Y) input signal
13	SDA	I²C bus data input/output
14	SCL	I²C bus clock input/output
15	S0	I²C bus subaddress inputs
16	S1	
17	S2	
18	V_P	positive supply voltage
19	−(B-Y) OUT	−(B-Y) output signal
20	Y OUT	Y output signal
21	−(R-Y) OUT	−(R-Y) output signal
22	GND	ground
23	SYNC OUT	synchronization output
24	CLAMP OUT	clamping pulse generator output

DEVELOPMENT DATA

FUNCTIONAL DESCRIPTION

Each circuit contains two sets of inputs (see Fig. 1): input 1 receives colour difference signals from a colour decoder and input 2 receives RGB/YUV signals via a periconnector. Each set of inputs has its own synchronization input. The inputs are clamped by a clamping pulse, which is internally generated from the synchronization inputs.

In the RGB mode the signals are internally matrixed to form colour difference signals, before further processing is carried out by a control circuit (such as the TDA8461).

The outputs can be set in a high impedance OFF state, which allows the use of up to seven devices in parallel (I²C bus mode).

Control

The circuits can be controlled by an I²C bus or directly by d.c. voltages. The fast switching input can be operated via pin 16 of the periconnector.

I²C bus mode

The protocol for the devices in I²C bus mode is shown in Fig. 3.

STA : start condition
A6 : 1 ⎫
A5 : 1 ⎪
A4 : 0 ⎬ fixed address bits
A3 : 1 ⎭
A2 : subaddress bit set by S2
A1 : subaddress bit set by S1
A0 : subaddress bit set by S0
R/W : read/write bit (= 0 only write mode allowed)
AC : acknowledge, generated by the devices
D7 : MOD1 ⎫ mode control bits, see Table 2
D6 : MOD0 ⎭
D5 : G2 ⎫
D4 : G1 ⎬ gain control bits, see Table 4
D3 : G0 ⎭
D2 : PRIOR, priority bit
D1 : ON/OFF bit
D0 : ON/OFF active bit

STA	A6	A5	A4	A3	A2	A1	A0	R/W	AC	D7	D6	D5	D4	D3	D2	D1	D0	AC	STO

7Z81365

Fig. 3 I²C bus protocol.

Table 1 subaddressing

slave addressing bit			address select pins		
A2	A1	A3	S2	S1	S0
*	*	*	L	L	L
0	0	1	L	L	H
0	1	0	L	H	L
0	1	1	L	H	H
1	0	0	H	L	L
1	0	1	H	L	H
1	1	0	H	H	L
1	1	1	H	H	H

Note

L = input voltage LOW
H = input voltage HIGH
* = non-I²C bus operation

Table 2 Mode control

mode 1	mode 0	mode	function
0	0	0	input 2 is directly selected
0	1	1	input 2 is selected via RGB/YUV matrix
1	0	2	input 1 is directly selected
1	1	3	reserved, do not use

Table 3 Priority/fast switching

priority	fast switching	mode selected
0	X	set by mode control
1	0,4 V	mode 2
1	1-3 V	mode 1 if mode 1 is selected or mode 0 if mode 0 or 2 is selected

Table 4 Gain setting (see Fig. 1)

G2	G1	G0	A1	A2, A3, A4	TDA8443/ B1, B3	TDA8443A/ B1, B3	B2
0	0	0	1	1	−0,6	−1	0,45
0	0	1	1	1	1	1	1
0	1	0	reserved, do not use				
0	1	1	1	1	−0,6	−1	0,45
1	0	0	2	2	−0,6	−1	0,45
1	0	1	2	1	1	1	1
1	1	0	2	2	1	1	1
1	1	1	2	1	−0,6	−1	0,45

Matrix equations

The relationship between outputs and input signals of the matrix are as follows:

$Y = 0{,}3\ R + 0{,}59\ V + 0{,}11\ B$
$R\text{-}Y = 0{,}7\ R - 0{,}59\ V - 0{,}11\ B$
$B\text{-}Y = -0{,}3\ R - 0{,}59\ V + 0{,}89\ B$

Table 5 ON bit

ON	function
0	OFF, no output signal, high impedance OFF state
1	ON, normal function

Table 6 OFF active – ON (pin 9)

OFF active	ON	function
0	L	OFF
0	H	according to protocol, last defined D7 to D1 (may be entered whilst ON = L)
1	X	according to protocol, last defined D7 to D1

Power-on reset

If the circuits are switched on in the I^2C bus mode, all bits of D0 to D7 are set to zero.

Timing specifications

I^2C bus load conditions are as follows:
4 kΩ pull-up resistor to + 5 V; 200 pF capacitor to GND.
All values are referred to V_{IH} = 3 V and V_{IL} = 1,5 V.

parameter	symbol	min.	max.	unit
Bus free before start	t_{BUF}	4,0	–	μs
Start condition set-up time	$t_{SU;STA}$	4,0	–	μs
Start condition hold time	$t_{HD;STA}$	4,0	–	μs
SCL and SDA LOW period	t_{LOW}	4,0	–	μs
SCL HIGH period	t_{HIGH}	4,0	–	μs
SCL and SDA rise time	t_R	–	1,0	μs
SCL and SDA fall time	t_F	–	0,3	μs
Data set-up time (write)	$t_{SU;DAT}$	0,25	–	μs
Data hold time (write)	$t_{HD;DAT}$	1,0	–	μs
Acknowledge (from TDA8443) set-up time	$t_{SU,CAC}$	–	2	μs
Acknowledge (from TDA8443) hold time	$t_{HD,CAC}$	0	–	μs

Note

Timing $t_{HD,DAT}$ deviates from the I^2C bus specification. After reset has been activated, a delay of 50 μs must occur before transmission may be resumed.

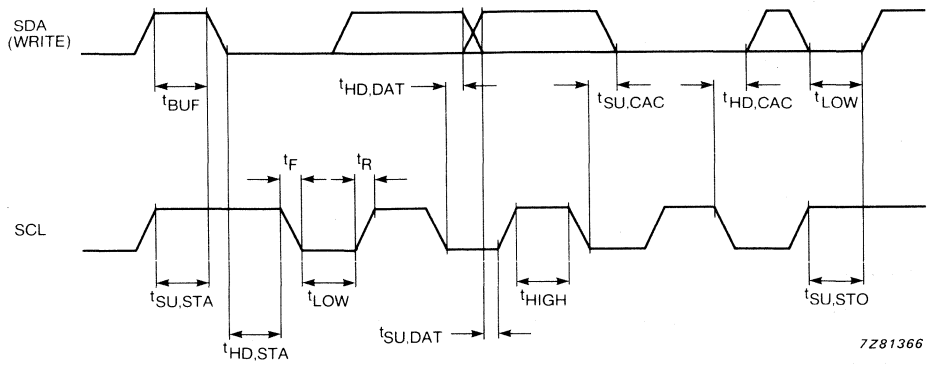


Fig. 4 I²C bus timing diagram.

Non-I²C bus mode

Table 7 non-I²C bus mode (S2 = S1 = S0 = L)

control			mode switched	gain settings		TDA8443	TDA8443A	
SDA	SCL	SEL	by FS	A1	A4, A3, A2	B1, B3	B1, B3	B2
L	L	L	2/0	1	1	1	1	1
L	L	H	2/0	1	2	1	1	1
L	H	L	2/1	1	1	−0,6	−1	0,45
L	H	H	2/0	1	1	−0,6	−1	0,45
H	L	L	2/0	2	1	1	1	1
H	L	H	2/0	2	2	1	1	1
H	H	L	2/1	2	1	−0,6	−1	0,45
H	H	H	2/0	2	1	−0,6	−1	0,45

Table 8 fast switching input

FS	mode selected
⩽ 0,4 V	mode 2
1 – 3 V	mode 0 or mode 1 as set by control

Table 9 ON input

ON	function
L	OFF, no output signal, high impedance OFF state
H	function is determined in table 7

DEVELOPMENT DATA

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage	V_{18-22}	V_P	–	14	V
Input voltage range	pin 13	VSDA	−0,3	14	V
	pin 14	VSCL	−0,3	14	V
	other pins		−0,3	V_P + 0,3	V
Maximum output current		I_O	–	20	mA
Storage temperature range		T_{stg}	−55	+ 125	°C
Operating ambient temperature range		T_{amb}	0	+ 70	°C
Maximum junction temperature			–	+ 125	°C

CHARACTERISTICS

V_P = 12 V; T_{amb} = 25 °C; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage	V_{18-22}	V_P	10,8	12,0	13,2	V
Supply current	I_{18}	I_P	–	65	90	mA
RGB/YUV channels						
Absolute gain difference	programmed value		–	0	10	%
Relative gain difference	between Y and the (R-Y) and (B-Y) channels		–	0	10	%
Relative gain difference	between any 2 other channels of any input		–	0	5	%
Input current		I_I	–	0,5	1,0	μA
Output impedance		$\lvert Z_{19-22}\rvert$ $\lvert Z_{20-22}\rvert$ $\lvert Z_{21-22}\rvert$	–	7	30	Ω
Bandwidth	3 dB, mode 0 or mode 2		–	25	–	MHz
Bandwidth	3 dB, mode 1		–	10	–	MHz
Mutual time difference at output	If all inputs of one source are connected together		–	–	25	ns

DEVELOPMENT DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Maximum output amplitude of YUV signals (peak-to-peak value)	gain x 1		2,1	–	–	V
	gain x 2		4,2	–	–	V
Crosstalk between inputs of same source	note 1 f = 5 MHz		–	–	–30	dB
Crosstalk between different sources			–	–	–40	dB
Isolation (OFF state)	f = 10 MHz		+ 50	–	–	dB
Differential gain at nominal output signals (peak-to-peak value):	R-Y = 1,05 V (p-p)		–	–	10	%
	B-Y = 1,33 V (p-p)		–	–	10	%
	Y = 0,34 V (p-p)		–	–	10	%
S/N ratio	note 2 B = 5 MHz nominal input		50	–	–	dB
Supply voltage rejection	note 3		30	–	–	dB
D.C. output levels	during clamping		–	5,3	–	V
Synchronization channels						
Gain difference	programmed value		–	–	10	%
Bandwidth	3 dB		–	50	–	MHz
Input Amplitude of sync. signal (peak-to-peak value)	for correct operation of clamp pulse generator		0,2	–	2,5	V
Output impedance		$\lvert Z_{23\text{-}22} \rvert$	–	20	30	Ω
Maximum output amplitude (peak-to-peak value)	pin 23 undistorted		2,5	–	–	V
D.C. level on top of sync. pulse	output		–	1,9	–	V
I²C bus inputs/outputs	SDA and SCL pins 13 and 14 respectively					
Input voltage HIGH		V_{IH}	3	–	V_P	V
Input voltage LOW		V_{IL}	–0,3	–	1,5	V
Input current HIGH		I_{IH}	–	–	10	μA
Input current LOW		I_{IL}	–	–	10	μA

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
SDA output	open collector					
Output voltage LOW	output current = 3 mA (LOW)	V_{OL}	–	–	0,4	V
Maximum output current LOW	sink current	I_{OL}	–	5	–	mA
Subaddresses inputs	S0, S1, S2 pins 15, 16, 17 respectively					
Input voltage HIGH		V_{IH}	3	–	V_P	V
Input voltage LOW		V_{IL}	−0,3	–	0,4	V
Input current HIGH		I_{IH}	–	0	10	μA
Input current LOW		I_{IL}	−50	−10	0	μA
Fast switching pin						
Input voltage HIGH	$V_{3\text{-}22}$	V_{IH}	1	–	3	V
Input voltage LOW	$V_{3\text{-}22}$	V_{IL}	−0,3	–	0,4	V
Input current HIGH	I_3	I_{IH}	–	–	500	μA
Input current LOW	I_3	I_{IL}	−100	–	–	μA
Switching delay	Fig. 5		–	20	–	ns
Switching time	Fig. 5		–	10	–	ns
Select pin	pin 1					
Input voltage HIGH	$V_{1\text{-}22}$	V_{IH}	3	–	V_P	V
Input voltage LOW	$V_{1\text{-}22}$	V_{IL}	−0,3	–	0,4	V
Input current HIGH	I_1	I_{IH}	–	0	10	μA
Input current LOW	I_1	I_{IL}	−50	−10	0	μA
ON pin						
Input voltage HIGH	$V_{9\text{-}22}$	V_{IH}	3	–	V_P	V
Input voltage LOW	$V_{9\text{-}22}$	V_{IL}	−0,3	–	1,5	V
Input current HIGH	I_9	I_{IH}	–	–	10	μA
Input current LOW	I_9	I_{IL}	–	–	10	μA

Notes to the characteristics

1. Crosstalk is defined as the ratio between the output signal originating from a not selected input and the signal from the selected input, both driven at their nominal level.
2. $S/N = 20 \log \frac{V_{O(p\text{-}p)}}{V_O \text{ noise (rms) } B = 5 \text{ MHz}}$
3. Supply voltage rejection $= 20 \log \frac{V_r \text{ supply}}{V_r \text{ on the output}}$

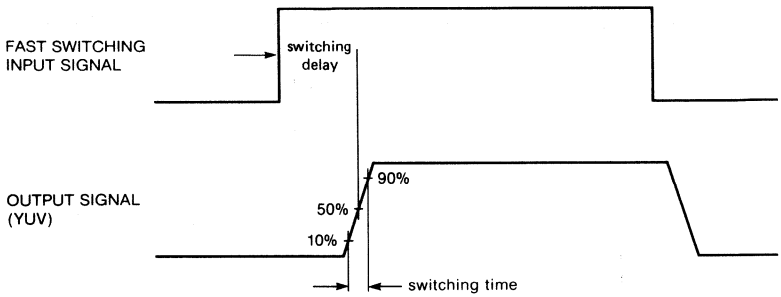


Fig. 5 Fast switching signal diagram.

DEVELOPMENT DATA

APPLICATION INFORMATION

Table 10 application information (TDA8443A)

input 1	input 2	output	mode	G2	G1	G0
Y = 0,34 V U = −1,33 V V = −1,05 V S = 0,3 V		Y = 0,34 V U = −1,33 V V = −1,05 V S = 0,6 V	2	1	1	1
	R = 0,75 V G = 0,75 V B = 0,75 V S = 0,3 V		1	1	1	1
Y = 0,34 V U = −1,33 V V = −1,05 V S = 0,3 V		Y = 0,68 V U = −2,66 V V = −2,10 V S = 0,6 V	2	1	0	0
	R = 0,75 V G = 0,75 V B = 0,75 V S = 0,3 V		1	1	0	0
Y = 0,34 V U = −1,33 V V = −1,05 V S = 0,3 V		Y = 0,34 V U = −1,33 V V = −1,05 V S = 0,6 V	2	1	0	1
	Y = 0,34 V U = −1,33 V V = −1,05 V S = 0,3 V		0	1	0	1
Y = 0,34 V U = −1,33 V V = −1,05 V S = 0,3 V		Y = 0,68 V U = −2,66 V V = −2,10 V S = 0,6 V	2	1	1	0
	Y = 0,34 V U = −1,33 V V = −1,05 V S = 0,3 V		0	1	1	0

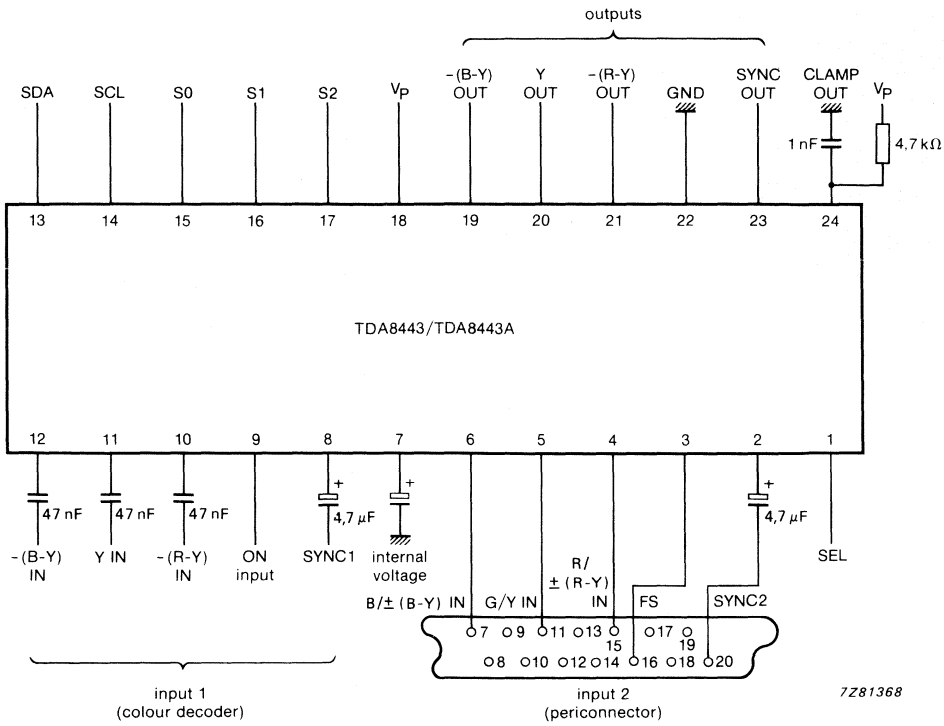


Fig. 6 Application diagram.

OCTUPLE 6-BIT DAC WITH I²C BUS

GENERAL DESCRIPTION

The TDA8444 comprises eight digital-to-analogue converters (DACs) each controlled via the two-wire I²C bus. The DACs are individually programmed using a 6-bit word to select an output from one of 64 voltage steps. The maximum output voltage of all DACs is set by the input V_{max} and the resolution is approximately $V_{max}/64$. At power-on all DAC outputs are set to their lowest value. The I²C bus slave receiver has a 7-bit address of which 3 bits are programmable via pins A0, A1 and A2.

Features

- Eight discrete DACs
- I²C bus slave receiver
- 16-pin DIL package

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage	pin 1	V_P	10,8	12,0	13,2	V
Supply current	no loads; $V_{max} = V_P$; all data = 00	I_{CC}	8	11	15	mA
Total power dissipation	no loads; $V_{max} = V_P$; all data = 00	P_{tot}	–	130	–	mW
Effective range of V_{max} input	V_P = 12 V	V_{max}	1	–	10,5	V
DAC output voltage range	pins 9,10,11,12,13,14, 15 or 16	V_O	0,1	–	V_P–0,5	V
Step value of 1 LSB	$V_{max} = V_P$	V_{LSB}	100	160	250	mV

PACKAGE OUTLINE

16-lead DIL; plastic (SOT-38).

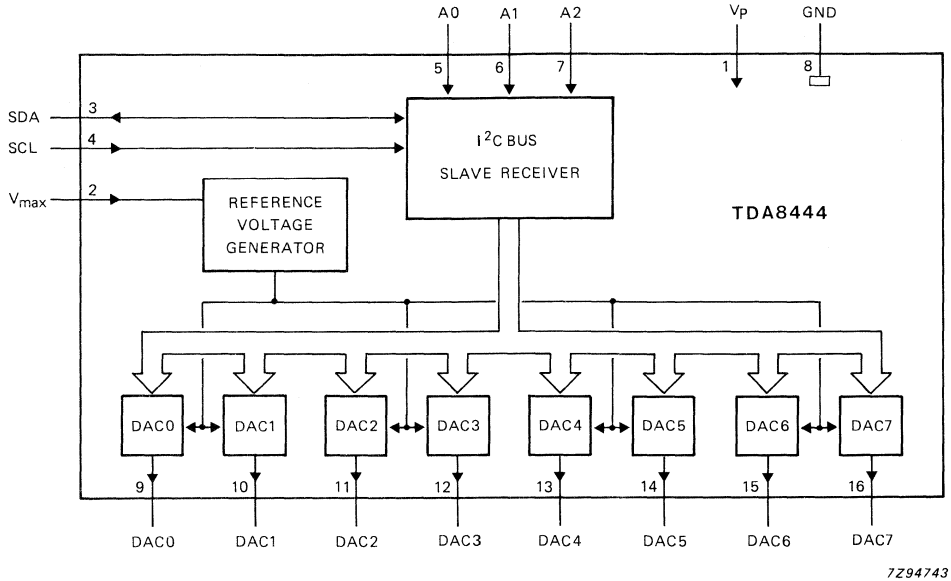


Fig. 1 Block diagram.

PINNING

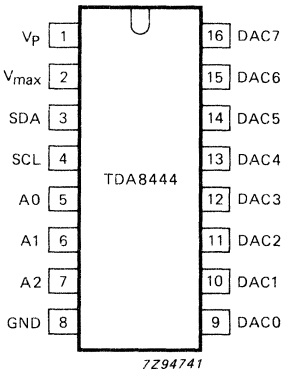


Fig. 2 Pinning diagram.

1	V_P	positive supply voltage
2	V_{max}	control input for DAC maximum output voltage
3	SDA	I^2C bus serial data input/output
4	SCL	I^2C bus serial data clock
5	A0	programmable address bits for I^2C bus slave receiver
6	A1	
7	A2	
8	GND	ground
9-16	DAC0-7	analogue voltage outputs

FUNCTIONAL DESCRIPTION

I²C bus

The TDA8444 I²C bus interface is a receive-only slave. Data is accepted from the I²C bus in the following format:

S	0 1 0 0 A2 A1 A0 0	A	I3 I2 I1 I0 SD SC SB SA	A	X X D5 D4 D3 D2 D1 D0	A	P
	◄— address byte —►		◄— instruction byte —►		◄— first data byte —►		

Where:

S = start condition
P = stop condition
A = acknowledge
X = don't care

A2, A1, A0 = programmable address bits
I3, I2, I1, I0 = instruction bits
SD, SC, SB, SA = subaddress bits
D5, D4, D3, D2, D1, D0 = data bits

Fig. 3 Data format.

Address byte

Valid addresses are 40, 42, 44, 46, 48, 4A, 4C, 4E (hexadec), depending on the programming of bits A2, A1 and A0. With these addresses, up to eight TDA8444 ICs can be operated independently from one I²C bus. No other addresses are acknowledged by the TDA8444.

Instruction and data bytes

Valid instructions are 00 to 0F and F0 to FF (hexadec); the TDA8444 will not respond to other instruction values.

Instructions 00 to 0F cause auto-incrementing of the subaddress (bits SD to SA) when more than one data byte is sent within one transmission. With auto-incrementing, the first data byte is written into the DAC addressed by bits SD to SA and then the subaddress is automatically incremented by one position for the next data byte in the series.

Auto-incrementation does not occur with instructions F0 to FF. Other than auto-incrementation there is no difference between instructions 00 to 0F and F0 to FF. When only one data byte per transmission is present, the DAC addressed by the subaddress will always receive the data.

Valid subaddresses (bits SD to SA) are 0 to 7 (hexadec) relating numerically to DAC0 to DAC7. When the auto-incrementing function is used, the subaddress will sequence through all possible values (0 to F, 0 to F, etc.).

I²C bus

Input SCL (pin 3) and input/output SDA (pin 4) conform to I²C bus specifications.* Pins 3 and 4 are protected against positive voltage pulses by internal zener diodes connected to the ground plane and therefore the normal bus line voltage should not exceed 5,5 V.

The address inputs A0, A1, A2 are programmed by a connection to GND for An = 0 or to Vp for An = 1. If the inputs are left floating, An = 1 will result.

* I²C bus specifications can be supplied on request.

FUNCTIONAL DESCRIPTION (continued)

Input V_{max}

Input V_{max} (pin 2) provides a means of compressing the output voltage swing of the DACs. The maximum DAC output voltage is restricted to approximately V_{max} while the 6-bit resolution is maintained, so giving a finer voltage resolution of smaller output swings.

Digital-to-analogue converters

Each DAC comprises a 6-bit data latch, current switches and an output driver. Current sources with values weighted by 2^0 up to 2^5 are switched according to the data input so that the sum of the selected currents gives the required analogue voltage from the output driver. The range of the output voltage is approximately 0,5 to 10,5 V when $V_{max} = V_P$.

The DAC outputs are protected against short-circuits to V_P and GND.

To avoid the possibility of oscillations, capacitive loading at the DAC outputs should not exceed 2 nF.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage	pin 1	$V_P = V_{1-8}$	0,5	18	V
Supply current	source current	$-I_P = -I_1$	–	10	mA
		$I_P = I_I$	–	25	mA
I^2C bus line voltage	pins 3 and 4	$V_{3,\,4-8}$	−0,5	5,9	V
Input voltage	pins 2 and 5 to 7	V_I	−0,5	V_P+0,5	V
Output voltage	pins 9 to 16	V_O	−0,5	V_P+0,5	V
Maximum current on any pin	pins 2 to 7, and 9 to 16	$\pm I_{max}$	–	10	mA
Total power dissipation		P_{tot}	–	500	mW
Operating ambient temperature range		T_{amb}	−20	+70	°C
Storage temperature range		T_{stg}	−55	+125	°C

THERMAL RESISTANCE

From junction to ambient $R_{th\ j-a}$ 75 K/W

CHARACTERISTICS

All voltages are with respect to GND; T_{amb} = 25 °C

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage	pin 1	$V_P = V_{1-8}$	10,8	12,0	13,2	V
Voltage level for power-on reset	pin 1	V_1	1	–	4,6	V
Supply current	no loads; $V_{max} = V_P$; all data = 00	$I_P = I_1$	8	11	15	mA
Total power dissipation	no loads; $V_{max} = V_P$; all data = 00	P_{tot}	–	130	–	mW
Effective range of V_{max} input	pin 2; V_P = 12 V	$V_{max} = V_2$	1,0	–	10,5	V
Pin 2 current		$-I_2$	–	–	10	μA
SDA, SCL inputs						
Input voltage range	pins 3 and 4	V_I	0	–	5,5	V
Input voltage LOW	pins 3 and 4	V_{IL}	–	–	1,5	V
Input voltage HIGH	pins 3 and 4	V_{IH}	3,0	–	–	V
Input current LOW	pins 3 and 4	I_{IL}	–	–	10	μA
Input current HIGH	pins 3 and 4	I_{IH}	–	–	10	μA
SDA output						
Output voltage LOW	pin 3; I_3 = 3 mA	V_{OL}	–	–	0,4	V
Sink current	pin 3	I_O	3	5	–	mA
Address inputs						
Input voltage range	pins 5, 6 and 7	V_I	0	–	V_P	V
Input voltage LOW	pins 5, 6 and 7	V_{IL}	–	–	1,4	V
Input voltage HIGH	pins 5, 6 and 7	V_{IH}	2,1	–	–	V
Input current LOW	pins 5, 6 and 7	$-I_{IL}$	–	5	10	μA
Input current HIGH	pins 5, 6 and 7	I_{IH}	–	–	1	μA

DEVELOPMENT DATA

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
DAC outputs						
Output voltage range	pins 9 to 16	V_O	0,1	–	V_P–0,5	V
Minimum output voltage	pins 9 to 16 data = 00; I_O = 0 mA	V_{Omin}	0,1	0,4	0,8	V
Maximum output voltage	pins 9 to 16 data = 3F; I_O = 0 mA					
at $V_{max} = V_P$ = 12 V		V_{Omax}	10	10,5	11,5	V
at $1 < V_{max} < 10,5$ V		V_{Omax}		see note		V
Output sink current	pins 9 to 16	I_O	2	8	15	mA
Output source current	pins 9 to 16	$-I_O$	2	–	6	mA
Output impedance	pins 9 to 16 $-2 \leqslant I_O \leqslant +2$ mA	Z_O	–	2	70	Ω
Step value of 1 LSB	$V_{max} = V_P$	V_{LSB}	100	160	250	mV
Deviation from linearity			0	–	50	mV

Note.

$V_{Omax} = 0,95\ V_{max} + V_{Omin} + 0,5$ V

APPLICATION INFORMATION

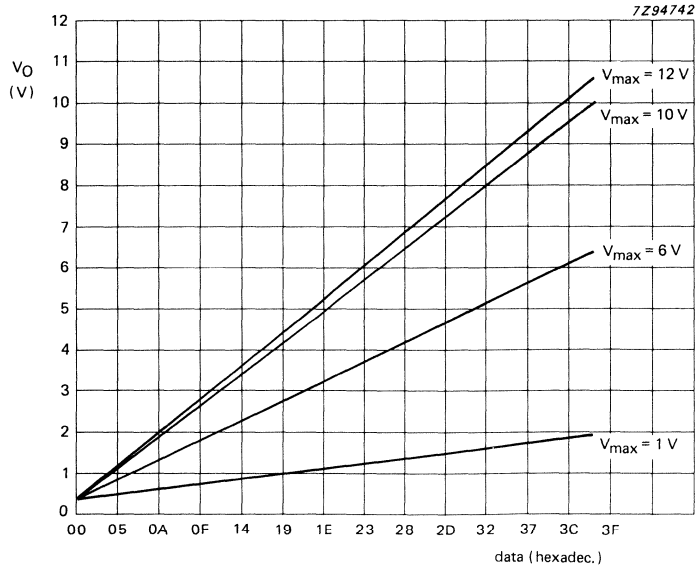


Fig. 4 Graph showing output voltage as a function of the input data value for V_{max} values of 1, 6, 10 and 12 V; V_P = 12 V.

FM/IF SYSTEM
AND MICROCOMPUTER-BASED TUNING INTERFACE

GENERAL DESCRIPTION

The TEA6000 is an FM/IF system circuit intended for microcomputer controlled radio receivers. The circuit includes an AM/FM-IF counter and an analogue-to-digital interface. The i.f. counter generates AM/FM precision tuning and accurate stop information.

Features

- 3-stage IF limiter for driving a ratio detector
- 2-stage level detector with current output
- operational amplifier for active filtering (e.g. multipath detector)
- high resolution frequency counter for FM and AM IF-signals
- time base reference from crystal oscillator or external source (SAA1057)
- serial two wire bidirectional computer interface (I^2C-bus)
- multiplexed 3 bit A/D converter for two input signals
- software controlled sensitivity for both ADC inputs

QUICK REFERENCE DATA

Supply voltages (V_{P1} and V_{P2})	V_P	typ.	8,4 V
Supply current; ($I_{P1} + I_{P2}$)	I_P	typ.	36 mA
FM/IF sensitivity			
at −3 dB before limiting	V_i	typ.	150 μV
Signal to noise ratio for V_i = 10 mV	S/N	typ.	80 dB
Audio output voltage			
Δf = 22,5 kHz; V_i = 1 mV	V_O	typ.	170 mV
Δf = 75 kHz; V_i = 1 mV	V_O	typ.	520 mV
AM suppression at V_i = 10 mV	AMS	typ.	58 dB
Frequency counter sensitivity			
AM (pin 18)	$V_{i(am)}$	typ.	60 μV
FM (pin 16)	$V_i(fm)$	typ.	80 μV
Resolution frequency counter			
AM	$f_{s(am)}$	typ.	·250 Hz
FM	$f_{s(fm)}$	typ.	6,4 kHz
Power dissipation	P_{tot}	max.	1300 mW
Storage temperature	T_{stg}	−55 to + 150	°C
Operating ambient temperature	T_{amb}	−30 to + 85	°C

PACKAGE OUTLINE

18-lead DIL; plastic (SOT-102H).

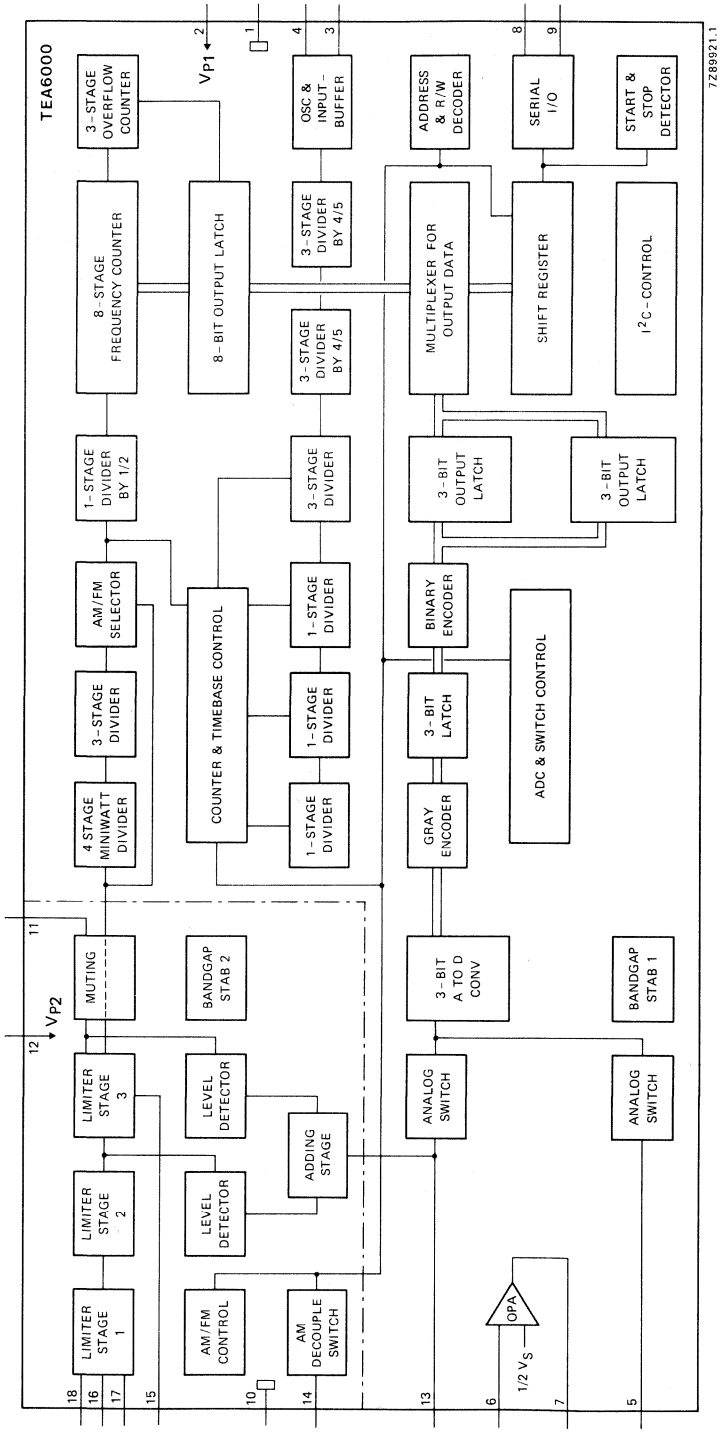


Fig. 1 Block diagram.

FUNCTIONAL DESCRIPTION

The IF SECTION consists of three balanced differential stages with separated FM and AM inputs, directly coupled by emitter followers. The last stage also has separated outputs, which are intended for driving a ratio detector and the frequency measuring system respectively.

The last two stages are coupled via low-value capacitors to two LEVEL DETECTORS which generate a signal-dependent d.c. current for controlling channel separation and frequency response of a stereo decoder, multipath detector circuitry, AGC and the internal ADC.

The IF MUTING circuit has been incorporated to decrease the interstation noise by about 15 dB.

The 3-bit A/D CONVERTER has two inputs, which are selected via two multiplexed analogue switches. One of these switches is internally connected to the level detector output but can also serve as an external input, as the level detector output can be switched off. The outputs of the ADC are converted to a Gray code, latched and reconverted to a binary code to obtain glitch-free output data. The sensitivity of both inputs can be selected independently via software on two levels.

The reference for the ADC is derived from a BAND-GAP STABILIZER circuit. Multipath distortion on FM will generate an AM modulation on the d.c. voltage from the level detectors. This AM modulation can be filtered and rectified to obtain a multipath-dependent d.c. voltage. This voltage can be applied to the other input of the ADC.

To facilitate filtering an OPERATIONAL AMPLIFIER (OPA) is incorporated on the chip. The typical circuit diagram for a multipath filter is given in Fig. 4.

The FREQUENCY COUNTER is preceded by a 7-stage prescaler for FM, and FM/AM selector stage and a divider by 1 or 2. The actual counter is a presetable and resetable 8-stage counter with a 3-stage data disable overflow counter, which can be switched off. The eight significant output bits are situated symmetrically around 10,7 MHz and 460 kHz, when the external timebase source is used (e.g. SAA1057). See Table 1.

The reference for the TIMEBASE is primarily thought to be the SAA1057. This circuit generates from its 4 MHz crystal oscillator a 32 or 40 kHz signal. This signal is buffered and applied to the timebase circuitry (mode I). The circuit diagram for this mode I is given in Fig. 5a.
In the timebase, the selection is made for reference frequency (32 to 40 kHz), FM or AM mode and the width of the measuring window, all under software control. Accuracy $\pm$ ½ bit when the window is set to wide (see Fig. 2) and $\pm$ 1 bit when set to narrow. A special feature is the synchronization of the measuring cycle with the input DATA of the I^2C-bus, meaning the measuring cycle starts immediately after a "WRITE" instruction via the I^2C-bus.

For those who do not use the SAA1057 as reference, a 2^{15} Hz crystal (32 768 Hz) can be connected to the reference inputs directly, obtaining a quartz-oscillator reference. See Fig. 5b for the circuit diagram for this mode II.

When the circuit is used in mode II a correction has to be made to the values of window width and resolution as the cheap watch crystals differ by about 2,4% from the frequency generated by the SAA1057 (32 768 and 32 000 kHz respectively) See Table 2.

Communication between MUSTI and the microcomputer is accomplished via the two-wire bidirectional I^2C-bus (slave transceiver version); the SDA (serial data) and SCL (serial clock).

To prevent crosstalk between the digital and analogue parts of the circuit the power supply lines are fully isolated.

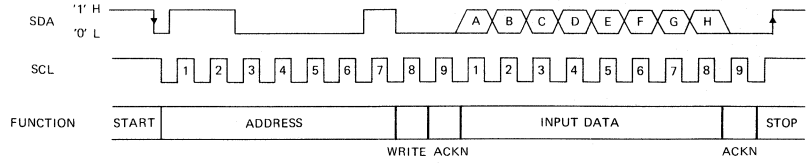


Fig. 2 Input data format waveforms.

Input bits

bit	function	"0"	"1"	reference to Fig. 2
1	reference frequency	32 kHz	40 kHz	A
2	sensitivity ADC2	LOW	HIGH	B
3	sensitivity ADC1	LOW	HIGH	C
4	level detector output	off	on	D
5	AM/FM	AM	FM	E
6	overflow counter	off	on	F
7	measuring window	narrow	wide	G
8	test mode	off	on	H

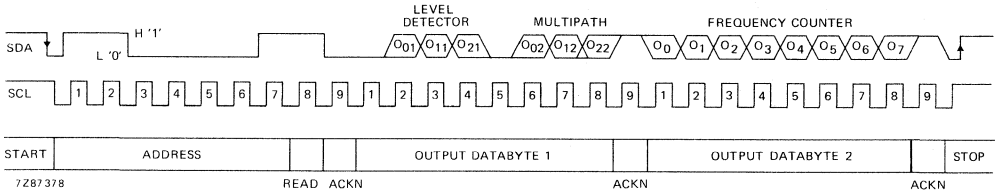


Fig. 3 Output data format waveforms.

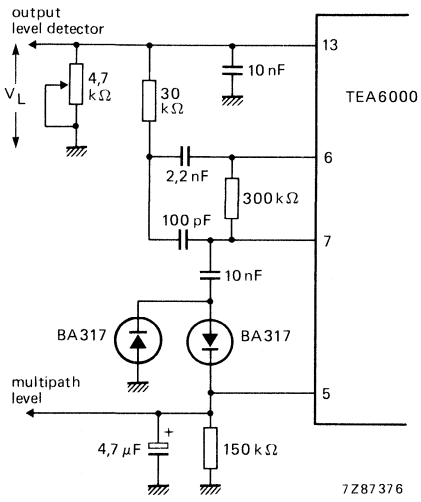


Fig. 4 Multipath detector circuit.

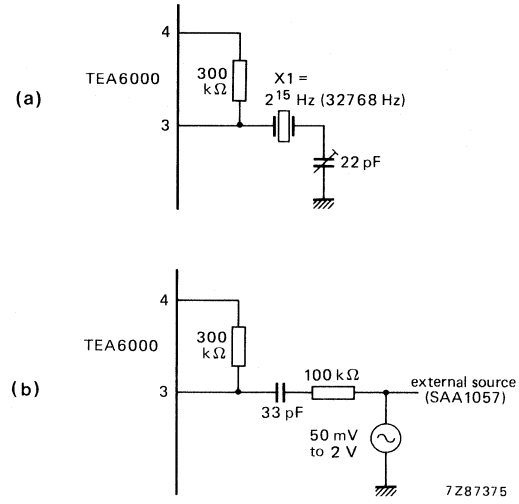


Fig. 5 Oscillator/buffer circuits.
X1 = 2^{15} Hz (32 768 Hz).

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage			
pin 2	V_{P1}	max.	13,2 V
pin 12	V_{P2}	max.	13,2 V
Power dissipation	P_{tot}	max.	1300 mW
Storage temperature	T_{stg}		−55 to + 150 °C
Operating ambient temperature	T_{amb}		−30 to + 85 °C

THERMAL RESISTANCE

From crystal to ambient	$R_{th\ c\text{-}a}$	=	50 K/W

D.C. CHARACTERISTICS

$V_{P1} = V_{P2} = 8{,}4$ V; $T_{amb} = 25$ °C, unless otherwise specified.

parameter	symbol	min.	typ.	max.	unit
Supply voltage					
(pin 2)	V_{P1}	7,6	8,4	9,2	V
(pin 12)	V_{P2}	7,6	8,4	9,2	V
Supply current AM mode					
pin 2	I_{P1}	–	18,5	–	mA
pin 12	I_{P2}	–	17,4	–	mA
Supply current FM mode					
pin 2	I_{P1}	–	19,2	–	mA
pin 12	I_{P2}	–	16,4	–	mA
Power dissipation	P_{tot}	–	350	–	mW

A.C. CHARACTERISTICS (see Fig. 6)

$V_{P1} = V_{P2} = 8{,}4$ V; $V_{16\text{-}10} = 1$ mV; f = 10,7 MHz; $\Delta f = 22{,}5$ kHz; $f_m = 1$ kHz; unless otherwise specified.

parameter	symbol	min.	typ.	max.	unit
Sensitivity					
at −3 dB before limiting	$V_{I(FM)}$	–	150	–	μV
Signal-to-noise ratio, FM input					
V_i = 20 μV	S/N	40	46	–	dB
V_i = 150 μV	S/N	–	64	–	dB
V_i = 1 mV	S/N	–	76	–	dB
V_i = 10 mV	S/N	–	80	–	dB
Noise output voltage					
V_i = 0 V; with muting, switch S1 on	V_{no}	–	55	–	μV
V_i = 0 V; without muting, S1 off	V_{no}	–	420	–	μV
Audio output voltage					
Δf = 22,5 kHz	V_O	–	170	–	mV
Δf = 75 kHz	V_O	–	520	–	mV

A.C. CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
AM suppression					
ratio of the AM output signal referred to the FM signal (m = 0,3)					
V_i = 150 μV	AMS	–	46	–	dB
V_i = 1 mV	AMS	–	62	–	dB
V_i = 10 mV	AMS	–	58	–	dB
V_i = 100 mV	AMS	–	60	–	dB
Level detector output voltage (Fig. 4)					
$R_{13\text{-}10}$ = 4,7 kΩ; V_i = 10 mV, FM mode	V_L	–	6,2	–	V
Level detector output voltage slope					
$R_{13\text{-}10}$ adjusted in FM mode for V_L = 5,5 V at V_i = 10 mV; f = 10,7 MHz					
V_i = 0 V (pin 16)	$V_{L(FM)}$	–	130	–	mV
V_i = 140 μV	$V_{L(FM)}$	–	1,3	–	V
V_i = 1 mV	$V_{L(FM)}$	–	2,7	–	V
V_i = 3 mV	$V_{L(FM)}$	–	4,4	–	V
$R_{13\text{-}10}$ adjusted in FM mode (see above)					
V_i = 0 V, f = 460 kHz (pin 18)	$V_{L(AM)}$	–	200	–	mV
V_i = 1 mV, f = 460 kHz (pin 18)	$V_{L(AM)}$	–	1,4	–	V
V_i = 10 mV, f = 460 kHz (pin 18)	$V_{L(AM)}$	–	2,7	–	V
Frequency counter sensitivity					
AM input voltage (pin 18)	$V_{I(AM)}$	–	60	–	μV
FM input voltage (pin 16)	$V_{I(FM)}$	–	80	–	μV
AM input impedance	R_i	–	30	–	kΩ
BUS inputs					
SDA and SCL (pins 9 and 8)					
input voltage HIGH	V_{IH}	3,0	–	V_{P1}	V
input voltage LOW	V_{IL}	−0,3	–	1,5	V
input current HIGH	I_{IH}	–	–	10	μA
input current LOW	I_{IL}	–	–	10	μA
acknowledge sink current	I_{ack}	–	–	2	mA
maximum input frequency	$f_{i\ max}$	100	–	–	kHz
Output voltage SDA					
HIGH; 4 kΩ to 8,4 V	V_{OH}	8,0	–	–	V
LOW; I = 2 mA	V_{OL}	–	–	0,4	V

parameter	symbol	min.	typ.	max.	unit
A/D converter (pin 5 and 13)					
input resistance	R_i		t.b.f.		kΩ
input capacitance	C_i		t.b.f.		pF
Trip levels, sensitivity bit HIGH					
level 1	V_T	–	0,6	–	V
level 2	V_T	–	1,06	–	V
level 3	V_T	–	1,38	–	V
level 4	V_T	–	1,84	–	V
level 5	V_T	–	2,14	–	V
level 6	V_T	–	2,55	–	V
level 7	V_T	–	2,97	–	V
Trip levels, sensitivity bit LOW					
level 1	V_T	–	0,96	–	V
level 2	V_T	–	1,78	–	V
level 3	V_T	–	2,44	–	V
level 4	V_T	–	3,26	–	V
level 5	V_T	–	3,92	–	V
level 6	V_T	–	4,63	–	V
level 7	V_T	–	5,38	–	V
Crystal oscillator (see Fig. 5)					
reference frequency	f_{ref}	32	32,768	40	kHz
temperature coefficient	TC		t.b.f.		10^{-6}
input resistance	R_i		t.b.f.		kΩ
input capacitance	C_i		t.b.f.		pF
Operational amplifier (pins 6 and 7)					
voltage gain	G_V	–	10^4	–	
input bias current	I_{bias}	–	30	100	nA
output sink current at V_O = 1 V	I_O	–	0,2	–	mA
output source current at V_O = 7,4 V	I_O	5,5	10	–	mA
output voltage swing	$V_{7(p-p)}$	–	5,5	–	V
Frequency measuring system (see pages 8 and 9)					
measuring windows; f_{ref} = 32 or 40 kHz					
AM					
window "0" (LOW)	t_{gate}	–	4	–	ms
window "1" (HIGH)	t_{gate}	–	8	–	ms
FM					
window "0" (LOW)	t_{gate}	–	20	–	ms
window "1" (HIGH)	t_{gate}	–	40	–	ms
resolution frequency counter					
AM	$f_{s(am)}$	–	250	–	Hz
FM	$f_{s(fm)}$	–	6,4	–	kHz

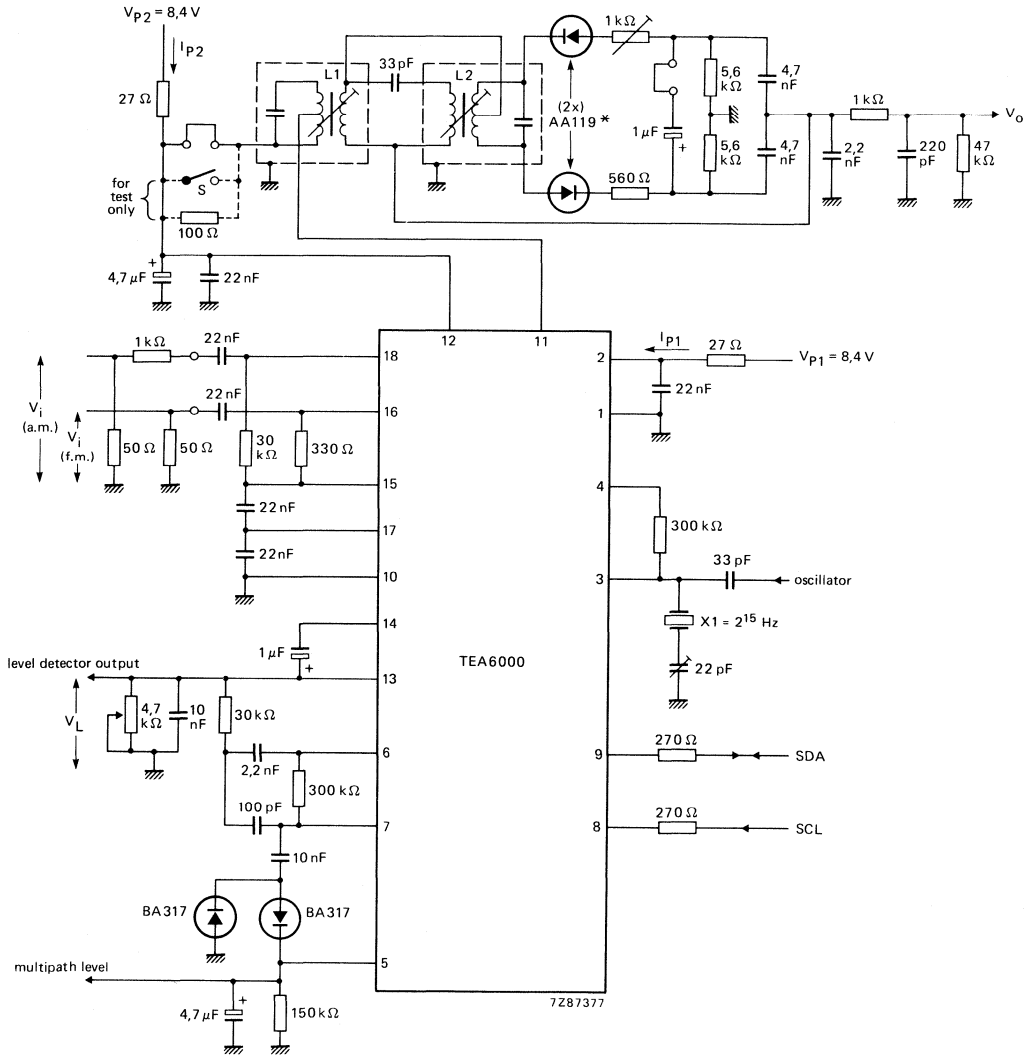
t_{gate} has to be multiplied by 32 000/32 768 for a f_{ref} of 2^{15} Hz.
f_s has to be multiplied by 32 768/32 000 for a f_{ref} of 2^{15} Hz.

TABLE 1 REFERENCE FREQUENCY 32 000 Hz (SAA1057)

AM (kHz)	READ OUT	FM (MHz)	AM (kHz)	READ OUT	FM (MHz)	AM (kHz)	READ OUT	FM (MHz)	AM (kHz)	READ OUT	FM (MHz)	AM (kHz)	READ OUT	FM (MHz)
428.25	'00'	9.888	441.00	'33'	10.214	453.75	'66'	10.541	466.50	'99'	10.867	479.25	'CC'	11.194
428.50	'01'	9.894	441.25	'34'	10.221	454.00	'67'	10.547	466.75	'9A'	10.874	479.50	'CD'	11.200
428.75	'02'	9.901	441.50	'35'	10.227	454.25	'68'	10.554	467.00	'9B'	10.880	479.75	'CE'	11.206
429.00	'03'	9.907	441.75	'36'	10.234	454.50	'69'	10.560	467.25	'9C'	10.886	480.00	'CF'	11.213
429.25	'04'	9.914	442.00	'37'	10.240	454.75	'6A'	10.566	467.50	'9D'	10.893	480.25	'D0'	11.219
429.50	'05'	9.920	442.25	'38'	10.246	455.00	'6B'	10.573	467.75	'9E'	10.899	480.50	'D1'	11.226
429.75	'06'	9.926	442.50	'39'	10.253	455.25	'6C'	10.579	468.00	'9F'	10.906	480.75	'D2'	11.232
430.00	'07'	9.933	442.75	'3A'	10.259	455.50	'6D'	10.586	468.25	'A0'	10.912	481.00	'D3'	11.238
430.25	'08'	9.939	443.00	'3B'	10.266	455.75	'6E'	10.592	468.50	'A1'	10.918	481.25	'D4'	11.245
430.50	'09'	9.946	443.25	'3C'	10.272	456.00	'6F'	10.598	468.75	'A2'	10.925	481.50	'D5'	11.251
430.75	'0A'	9.952	443.50	'3D'	10.278	456.25	'70'	10.605	469.00	'A3'	10.931	481.75	'D6'	11.258
431.00	'0B'	9.958	443.75	'3E'	10.285	456.50	'71'	10.611	469.25	'A4'	10.938	482.00	'D7'	11.264
431.25	'0C'	9.965	444.00	'3F'	10.291	456.75	'72'	10.618	469.50	'A5'	10.944	482.25	'D8'	11.270
431.50	'0D'	9.971	444.25	'40'	10.298	457.00	'73'	10.624	469.75	'A6'	10.950	482.50	'D9'	11.277
431.75	'0E'	9.978	444.50	'41'	10.304	457.25	'74'	10.630	470.00	'A7'	10.957	482.75	'DA'	11.283
432.00	'0F'	9.984	444.75	'42'	10.310	457.50	'75'	10.637	470.25	'A8'	10.963	483.00	'DB'	11.290
432.25	'10'	9.990	445.00	'43'	10.317	457.75	'76'	10.643	470.50	'A9'	10.970	483.25	'DC'	11.296
432.50	'11'	9.997	445.25	'44'	10.323	458.00	'77'	10.650	470.75	'AA'	10.976	483.50	'DD'	11.302
432.75	'12'	10.003	445.50	'45'	10.330	458.25	'78'	10.656	471.00	'AB'	10.982	483.75	'DE'	11.309
433.00	'13'	10.010	445.75	'46'	10.336	458.50	'79'	10.662	471.25	'AC'	10.989	484.00	'DF'	11.315
433.25	'14'	10.016	446.00	'47'	10.342	458.75	'7A'	10.669	471.50	'AD'	10.995	484.25	'E0'	11.322
433.50	'15'	10.022	446.25	'48'	10.349	459.00	'7B'	10.675	471.75	'AE'	11.002	484.50	'E1'	11.328
433.75	'16'	10.029	446.50	'49'	10.355	459.25	'7C'	10.682	472.00	'AF'	11.008	484.75	'E2'	11.334
434.00	'17'	10.035	446.75	'4A'	10.362	459.50	'7D'	10.688	472.25	'B0'	11.014	485.00	'E3'	11.341
434.25	'18'	10.042	447.00	'4B'	10.368	459.75	'7E'	10.694	472.50	'B1'	11.021	485.25	'E4'	11.347
434.50	'19'	10.048	447.25	'4C'	10.374	460.00	'7F'	10.701	472.75	'B2'	11.027	485.50	'E5'	11.354
434.75	'1A'	10.054	447.50	'4D'	10.381	460.25	'80'	10.707	473.00	'B3'	11.034	485.75	'E6'	11.360
435.00	'1B'	10.061	447.75	'4E'	10.387	460.50	'81'	10.714	473.25	'B4'	11.040	486.00	'E7'	11.366
435.25	'1C'	10.067	448.00	'4F'	10.394	460.75	'82'	10.720	473.50	'B5'	11.046	486.25	'E8'	11.373
435.50	'1D'	10.074	448.25	'50'	10.400	461.00	'83'	10.726	473.75	'B6'	11.053	486.50	'E9'	11.379
435.75	'1E'	10.080	448.50	'51'	10.406	461.25	'84'	10.733	474.00	'B7'	11.059	486.75	'EA'	11.386
436.00	'1F'	10.086	448.75	'52'	10.413	461.50	'85'	10.739	474.25	'B8'	11.066	487.00	'EB'	11.392
436.25	'20'	10.093	449.00	'53'	10.419	461.75	'86'	10.746	474.50	'B9'	11.072	487.25	'EC'	11.398
436.50	'21'	10.099	449.25	'54'	10.426	462.00	'87'	10.752	474.75	'BA'	11.078	487.50	'ED'	11.405
436.75	'22'	10.106	449.50	'55'	10.432	462.25	'88'	10.758	475.00	'BB'	11.085	487.75	'EE'	11.411
437.00	'23'	10.112	449.75	'56'	10.438	462.50	'89'	10.765	475.25	'BC'	11.091	488.00	'EF'	11.418
437.25	'24'	10.118	450.00	'57'	10.445	462.75	'8A'	10.771	475.50	'BD'	11.098	488.25	'F0'	11.424
437.50	'25'	10.125	450.25	'58'	10.451	463.00	'8B'	10.778	475.75	'BE'	11.104	488.50	'F1'	11.430
437.75	'26'	10.131	450.50	'59'	10.458	463.25	'8C'	10.784	476.00	'BF'	11.110	488.75	'F2'	11.437
438.00	'27'	10.138	450.75	'5A'	10.464	463.50	'8D'	10.790	476.25	'C0'	11.117	489.00	'F3'	11.443
438.25	'28'	10.144	451.00	'5B'	10.470	463.75	'8E'	10.797	476.50	'C1'	11.123	489.25	'F4'	11.450
438.50	'29'	10.150	451.25	'5C'	10.477	464.00	'8F'	10.803	476.75	'C2'	11.130	489.50	'F5'	11.456
438.75	'2A'	10.157	451.50	'5D'	10.483	464.25	'90'	10.810	477.00	'C3'	11.136	489.75	'F6'	11.462
439.00	'2B'	10.163	451.75	'5E'	10.490	464.50	'91'	10.816	477.25	'C4'	11.142	490.00	'F7'	11.469
439.25	'2C'	10.170	452.00	'5F'	10.496	464.75	'92'	10.822	477.50	'C5'	11.149	490.25	'F8'	11.475
439.50	'2D'	10.176	452.25	'60'	10.502	465.00	'93'	10.829	477.75	'C6'	11.155	490.50	'F9'	11.482
439.75	'2E'	10.182	452.50	'61'	10.509	465.25	'94'	10.835	478.00	'C7'	11.162	490.75	'FA'	11.488
440.00	'2F'	10.189	452.75	'62'	10.515	465.50	'95'	10.842	478.25	'C8'	11.168	491.00	'FB'	11.494
440.25	'30'	10.195	453.00	'63'	10.522	465.75	'96'	10.848	478.50	'C9'	11.174	491.25	'FC'	11.501
440.50	'31'	10.202	453.25	'64'	10.528	466.00	'97'	10.854	478.75	'CA'	11.181	491.50	'FD'	11.507
440.75	'32'	10.208	453.50	'65'	10.534	466.25	'98'	10.861	479.00	'CB'	11.187	491.75	'FE'	11.514

TABLE 2 REFERENCE FREQUENCY 32 768 Hz (2^{15} Hz)

AM (kHz)	READ OUT	FM (MHz)	AM (kHz)	READ OUT	FM (MHz)	AM (kHz)	READ OUT	FM (MHz)	AM (kHz)	READ OUT	FM (HMz)	AM (kHz)	READ OUT	FM (MHz)
438.53	'00'	10.125	451.58	'33'	10.460	464.64	'66'	10.794	477.70	'99'	11.128	490.75	'CC'	11.462
438.78	'01'	10.132	451.84	'34'	10.466	464.90	'67'	10.800	477.95	'9A'	11.135	491.01	'CD'	11.469
439.04	'02'	10.138	452.10	'35'	10.473	465.15	'68'	10.807	478.21	'9B'	11.141	491.26	'CE'	11.475
439.30	'03'	10.145	452.35	'36'	10.479	465.41	'69'	10.813	478.46	'9C'	11.148	491.52	'CF'	11.482
439.55	'04'	10.152	452.61	'37'	10.486	465.66	'6A'	10.820	478.72	'9D'	11.154	491.78	'D0'	11.488
439.81	'05'	10.158	452.86	'38'	10.492	465.92	'6B'	10.827	478.98	'9E'	11.161	492.03	'D1'	11.495
440.06	'06'	10.165	453.12	'39'	10.499	466.18	'6C'	10.833	479.23	'9F'	11.167	492.29	'D2'	11.502
440.32	'07'	10.171	453.38	'3A'	10.505	466.43	'6D'	10.840	479.49	'A0'	11.174	492.54	'D3'	11.508
440.58	'08'	10.178	453.63	'3B'	10.512	466.69	'6E'	10.846	479.74	'A1'	11.180	492.80	'D4'	11.515
440.83	'09'	10.184	453.89	'3C'	10.519	466.94	'6F'	10.853	480.00	'A2'	11.187	493.06	'D5'	11.521
441.09	'0A'	10.191	454.14	'3D'	10.525	467.20	'70'	10.859	480.26	'A3'	11.194	493.31	'D6'	11.528
441.34	'0B'	10.197	454.40	'3E'	10.532	467.46	'71'	10.866	480.51	'A4'	11.200	493.57	'D7'	11.534
441.60	'0C'	10.204	454.66	'3F'	10.538	467.71	'72'	10.872	480.77	'A5'	11.207	493.82	'D8'	11.541
441.86	'0D'	10.211	454.91	'40'	10.545	467.97	'73'	10.879	481.02	'A6'	11.213	494.08	'D9'	11.547
442.11	'0E'	10.217	455.17	'41'	10.551	468.22	'74'	10.886	481.28	'A7'	11.220	494.34	'DA'	11.554
442.37	'0F'	10.224	455.42	'42'	10.558	468.48	'75'	10.892	481.54	'A8'	11.226	494.59	'DB'	11.561
442.62	'10'	10.230	455.68	'43'	10.564	468.74	'76'	10.899	481.79	'A9'	11.233	494.85	'DC'	11.567
442.88	'11'	10.237	455.94	'44'	10.571	468.99	'77'	10.905	482.05	'AA'	11.239	495.10	'DD'	11.574
443.14	'12'	10.243	456.19	'45'	10.578	469.25	'78'	10.912	482.30	'AB'	11.246	495.36	'DE'	11.580
443.39	'13'	10.250	456.45	'46'	10.584	469.50	'79'	10.918	482.56	'AC'	11.253	495.62	'DF'	11.587
443.65	'14'	10.256	456.70	'47'	10.591	469.76	'7A'	10.925	482.82	'AD'	11.259	495.87	'E0'	11.593
443.90	'15'	10.263	456.96	'48'	10.597	470.02	'7B'	10.931	483.07	'AE'	11.266	496.13	'E1'	11.600
444.16	'16'	10.269	457.22	'49'	10.604	470.27	'7C'	10.938	483.33	'AF'	11.272	496.38	'E2'	11.606
444.42	'17'	10.276	457.47	'4A'	10.610	470.53	'7D'	10.945	483.58	'B0'	11.279	496.64	'E3'	11.613
444.67	'18'	10.283	457.73	'4B'	10.617	470.78	'7E'	10.951	483.84	'B1'	11.285	496.90	'E4'	11.620
444.93	'19'	10.289	457.98	'4C'	10.623	471.04	'7F'	10.958	484.10	'B2'	11.292	497.15	'E5'	11.626
445.18	'1A'	10.296	458.24	'4D'	10.630	471.30	'80'	10.964	484.35	'B3'	11.298	497.41	'E6'	11.633
445.44	'1B'	10.302	458.50	'4E'	10.636	471.55	'81'	10.971	484.61	'B4'	11.305	497.66	'E7'	11.639
445.70	'1C'	10.309	458.75	'4F'	10.643	471.81	'82'	10.977	484.86	'B5'	11.312	497.92	'E8'	11.646
445.95	'1D'	10.315	459.01	'50'	10.650	472.06	'83'	10.984	485.12	'B6'	11.318	498.18	'E9'	11.652
446.21	'1E'	10.322	459.26	'51'	10.656	472.32	'84'	10.990	485.38	'B7'	11.325	498.43	'EA'	11.659
446.46	'1F'	10.328	459.52	'52'	10.663	472.58	'85'	10.997	485.63	'B8'	11.331	498.69	'EB'	11.665
446.72	'20'	10.335	459.78	'53'	10.669	472.83	'86'	11.003	485.89	'B9'	11.338	498.94	'EC'	11.672
446.98	'21'	10.342	460.03	'54'	10.676	473.09	'87'	11.010	486.14	'BA'	11.344	499.20	'ED'	11.679
447.23	'22'	10.348	460.29	'55'	10.682	473.34	'88'	11.017	486.40	'BB'	11.351	499.46	'EE'	11.685
447.49	'23'	10.355	460.54	'56'	10.689	473.60	'89'	11.023	486.66	'BC'	11.357	499.71	'EF'	11.692
447.74	'24'	10.361	460.80	'57'	10.695	473.86	'8A'	11.030	486.91	'BD'	11.364	499.97	'F0'	11.698
448.00	'25'	10.368	461.06	'58'	10.702	474.11	'8B'	11.036	487.17	'BE'	11.370	500.22	'F1'	11.705
448.26	'26'	10.374	461.31	'59'	10.709	474.37	'8C'	11.043	487.42	'BF'	11.377	500.48	'F2'	11.711
448.51	'27'	10.381	461.57	'5A'	10.715	474.62	'8D'	11.049	487.68	'C0'	11.384	500.74	'F3'	11.718
448.77	'28'	10.387	461.82	'5B'	10.722	474.88	'8E'	11.056	487.94	'C1'	11.390	500.99	'F4'	11.724
449.02	'29'	10.394	462.08	'5C'	10.728	475.14	'8F'	11.062	488.19	'C2'	11.397	501.25	'F5'	11.731
449.28	'2A'	10.401	462.34	'5D'	10.735	475.39	'90'	11.069	488.45	'C3'	11.403	501.50	'F6'	11.737
449.54	'2B'	10.407	462.59	'5E'	10.741	475.65	'91'	11.076	488.70	'C4'	11.410	501.76	'F7'	11.744
449.79	'2C'	10.414	462.85	'5F'	10.748	475.90	'92'	11.082	488.96	'C5'	11.416	502.02	'F8'	11.751
450.05	'2D'	10.420	463.10	'60'	10.754	476.16	'93'	11.089	489.22	'C6'	11.423	502.27	'F9'	11.757
450.30	'2E'	10.427	463.36	'61'	10.761	476.42	'94'	11.095	489.47	'C7'	11.429	502.53	'FA'	11.764
450.56	'2F'	10.433	463.62	'62'	10.768	476.67	'95'	11.102	489.73	'C8'	11.436	502.78	'FB'	11.770
450.82	'30'	10.440	463.87	'63'	10.774	476.93	'96'	11.108	489.98	'C9'	11.443	503.04	'FC'	11.777
451.07	'31'	10.446	464.13	'64'	10.781	477.18	'97'	11.115	490.24	'CA'	11.449	503.30	'FD'	11.783
451.33	'32'	10.453	464.38	'65'	10.787	477.44	'98'	11.121	490.50	'CB'	11.456	503.55	'FE'	11.790



L1 = 3122 138 2021/TOKO 85 ACS-4238 A
L2 = 3122 138 2022/TOKO 85 ACS-4260 SEJ

Fig. 6 MUSTI test and application circuit.
Germanium diodes AA119 are required in the test circuit only.
In a complete FM channel (inclusive FM front end) the silicon diodes BA281 are recommended.

S open = without muting
S closed = with muting
} for measuring purpose only.

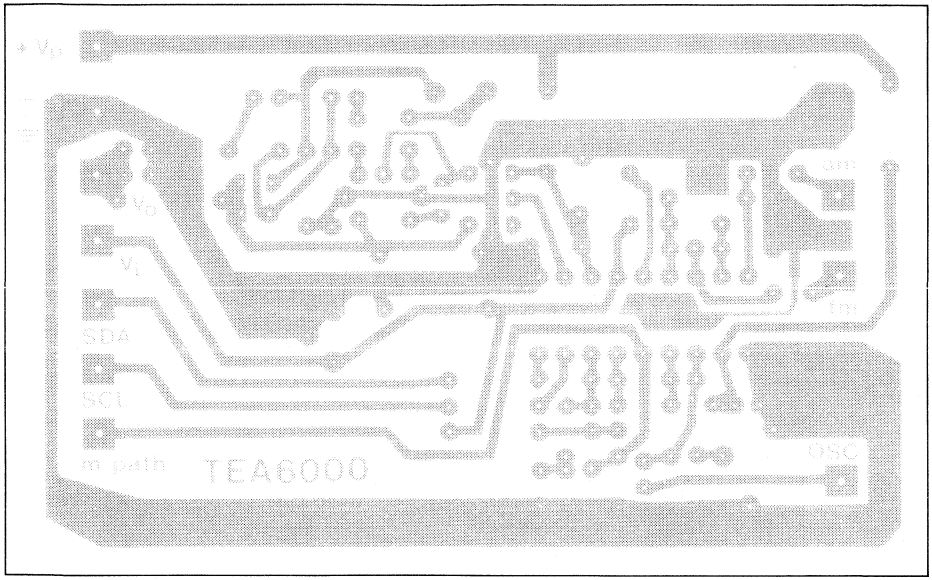


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Fig. 7 Track side of printed-circuit board.

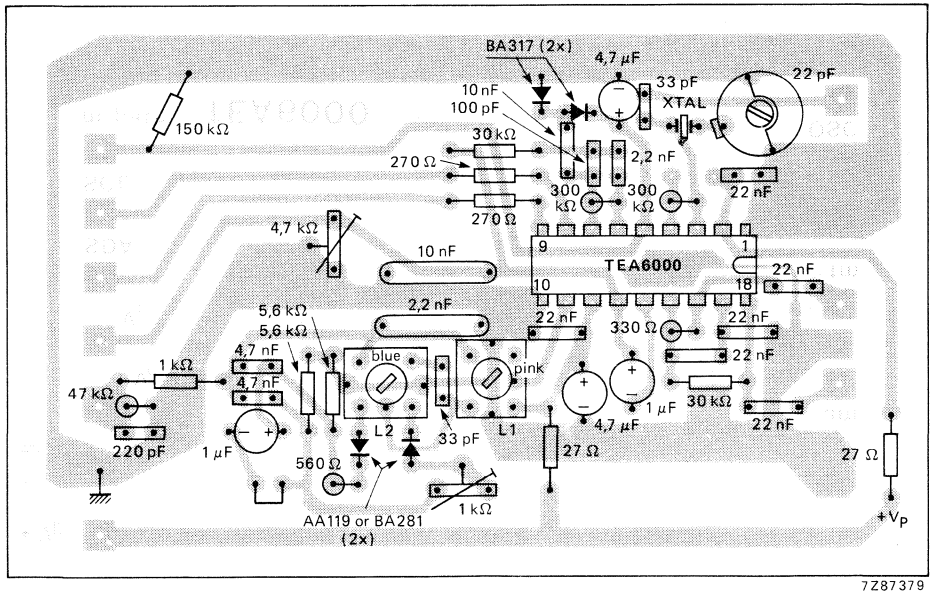

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Fig. 8 Component side of printed-circuit board.

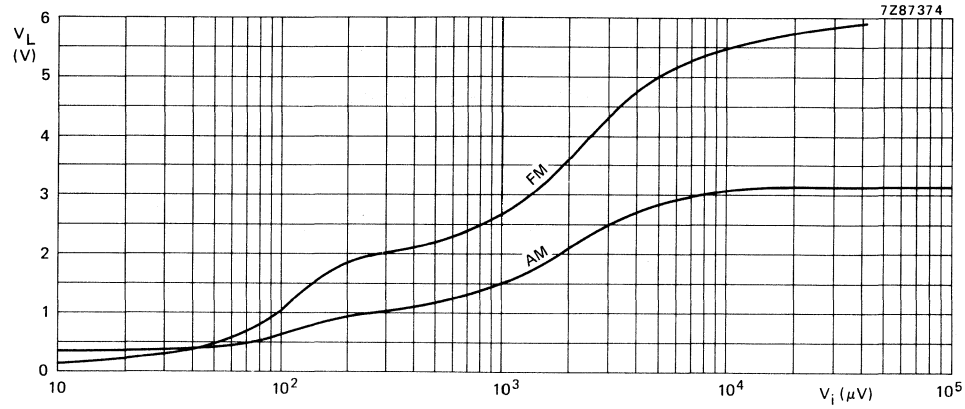


Fig. 9 Level detector output as a function of input voltage.

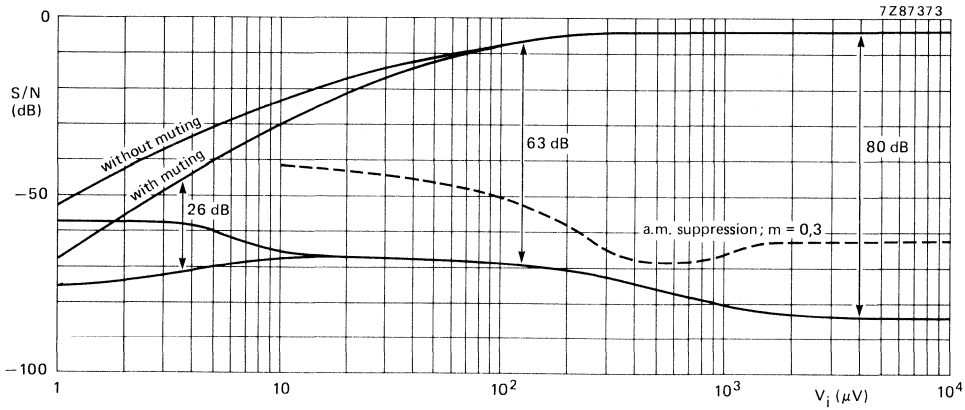


Fig. 10 Signal-to-noise ratio as a function of FM input voltage.
f_i = 10,7 MHz; Δf = 22,5 kHz; f_{mod} = 1 kHz; 0 dB = 245 mV.

FM/IF SYSTEM AND MICROCOMPUTER-BASED TUNING INTERFACE

GENERAL DESCRIPTION

The TEA6100 is a FM/IF system circuit intended for microcomputer controlled radio receivers. The circuit includes highly sensitive analogue circuitry. The digital circuitry, including an I^2C bus, controls the analogue circuitry and the AM/FM tuning and stop information for the microcomputer.

Features

- 4-stage symmetrical IF limiting amplifier
- Software selectable AM or FM input
- Symmetrical quadrature demodulator
- Single-ended LF output stage
- D.C. output level determined by the input signal
- Semi-adjustable AM and FM level voltage
- Multi-path detector/rectifier/amplifier circuitry
- 3-bit level information and 3-bit multi-path information
- Signal dependent 'soft' muting circuit; externally adjustable
- Reference voltage output (FM mode only)
- 8-bit AM/FM frequency counter with selectable counter resolution
- Possibility to measure the AM IF frequency at 460 kHz (250 Hz resolution) and 10,7 MHz (500 Hz resolution)
- Reference frequency can be directly connected to the reference frequency output of a frequency synthesizer (TSA6057, 40 kHz)

PACKAGE OUTLINE

20-lead DIL; plastic (SOT-146).

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage		V_{P1}, V_{P2}	–	8,5	–	V
Supply current		$I_{P1} + I_{P2}$	–	35	–	mA
FM/IF sensitivity	–3 dB before limiting	V_i	–	15	–	μV
Signal plus noise to noise ratio	Δf = 75 kHz; V_I = 10 mV	(S + N)/N	–	85	–	dB
Audio output voltage after limiting	Δf = 22,5 kHz	V_o	–	200	–	mV
AM suppression	V_{IFM} = 600 μV to 600 mV; m = 0,3	AMS	–	60	–	dB
Frequency counter sensitivity						
AM	pin 19, f = 10,7 MHz	$V_{i(AM)}$	–	45	–	μV
	f = 460 kHz	$V_{i(AM)}$	–	20	–	μV
FM	pin 18, f = 10,7 MHz	$V_{i(FM)}$	–	45	–	μV
Resolution of the frequency counter	reference frequency of 40 kHz;					
AM	IF = 460 kHz	f_s (AM)	–	250	–	Hz
	IF = 10,7 MHz	f_s (AM)	–	500	–	Hz
FM		f_s (FM)	–	6,4	–	kHz

DEVELOPMENT DATA

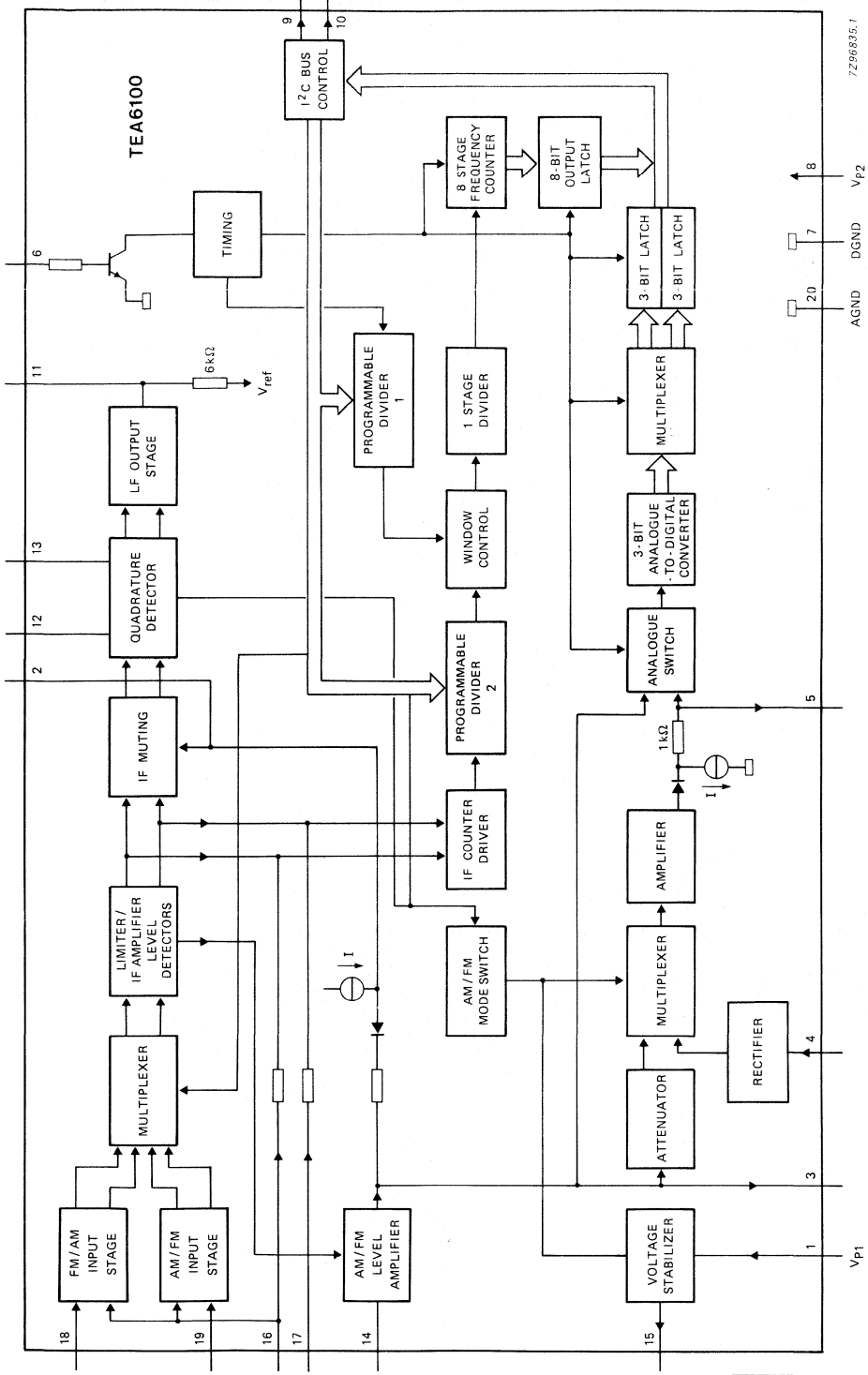


Fig. 1 Block diagram.

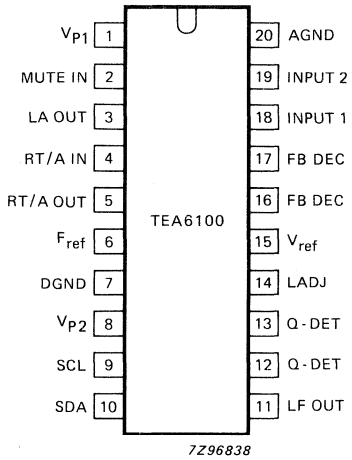


Fig. 2 Pinning diagram.

PINNING

1	V_{P1}	analogue supply voltage
2	MUTE IN	mute input
3	LA OUT	level amplifier output
4	RT/A IN	rectifier/amplifier input
5	RT/A OUT	rectifier/amplifier output
6	F_{ref}	reference frequency input
7	DGND	digital ground
8	V_{P2}	digital supply voltage
9	SCL	serial clock line) I^2C bus
10	SDA	serial data line)
11	LF OUT	audio output signal
12	Q-DET	phase shift for quadrature detector
13	Q-DET	phase shift for quadrature detector
14	LADJ	level amplifier adjustment
15	V_{ref}	reference voltage
16	FB DEC	decoupled feedback
17	FB DEC	decoupled feedback
18	INPUT 1	FM/AM IF input
19	INPUT 2	AM/FM IF input
20	AGND	analogue ground

FUNCTIONAL DESCRIPTION (see Figs 1 and 13)

The IF amplifier consists of four balanced limiting amplifier stages, two separate inputs (AM and FM) and one output. Software programming (see Table 2; Figs 4 and 5) allows the input signals (AM/FM) to be inserted on either input (pin 18 or 19). The output drives the frequency counter and via the mute stage, drives the quadrature detector. The output of the quadrature detector is applied to an audio stage (which has a single-ended output). The AM/FM level amplifier, which is driven by 5 IF level detectors, generates a signal dependent d.c. voltage. The level output voltage is used internally to control the mute stage and, if required, the signal can be used externally to control the stereo channel separation and frequency response of a stereo decoder. The signal is also feed to the analogue-to-digital converter (ADC). Due to the front-end spread in the amplification, the level voltage is made adjustable (LADJ, pin 14). The level voltage amplifier controls the mute stage and this insures the −3 dB limiting point remains constant, independent of the front-end spread. AM and FM mode have different front-end circuitry, therefore LADJ must be adjustable for both inputs.

The output voltage of the level amplifier is dependent upon the field strength of the input signal. The multi-path of the FM signal exists in the AM modulation of the input signal. The following method is used to determine the level information and the amount of multi-path (as a DC voltage):

- the IF level detector detects the multi-path and feds the signal, via the level amplifiers, to the external bandpass filter (pin 3) and ADC1
- the signal is then fed to an internal rectifier
- the rectified signal is then fed to an amplifier, so at pin 5 the DC level information is externally available and internally used by ADC2

In the FM mode, the DC information concerning the multi-path is available at pin 5 and the level information is available at pin 3.

In the AM mode, the level information at pin 3 cannot be directly used owing to AM modulation on the output signal of the level amplifier. This signal requires filtering, which is achieved by the following method:

- the multiplexer is switched to a position which causes the signal to be applied to the attenuator
- after attenuation the signal is fed to an amplifier (the resultant gain of attenuator and amplifier is unity), after amplification the signal is filtered by an internal resistor and external capacitor
- after filtering the signal is applied to ADC2 and is externally available

In AM mode pin 5 contains the level information.

The voltages on pin 3 and 5 are converted into two 3-bit digital words by the ADC, which can then be read out by the I^2C bus. The meaning of the 3-bit words is shown in Table 1.

Table 1 3-bit words

word	position	
	FM	AM
1	multipath	level without modulation
2	level	level with modulation

The FM modulated signal is converted into an audio signal by the symmetrical quadrature detector. The main advantage of such a detector is that it requires few external components.

An FM signal requires good AM suppression, and as a result, the IF amplifiers must act as limiters. To achieve good suppression on small input signals the IF amplifiers must have a high gain and thus a high sensitivity. High sensitivity is an undesirable property when used in car radio applications, this problem is solved by having an externally adjustable mute stage to control the overall sensitivity of the device.

The IF mute stage is controlled by the level amplifier (soft muting) and is only active in FM mode. If the input falls below a predetermined level, the mute stage becomes active. To avoid the 'ON/OFF' effect of the audio signal due to fluctuations of the input signal, the mute stage is activated rapidly but de-activated slowly. The mute stage is de-activated slowly, via a current source and an external capacitor at pin 2, to avoid aggressive behaviour of the audio signal. It is possible to adjust the '−3 dB limiting point' of the audio output via the level voltage due to the level signal being externally adjustable. If hard muting is required then pin 2 must be switched to ground.

The 8-bit counter allows accurate stop information to be obtained, because exact tuning is achieved when the measured frequency is equal to the centre frequency of the IF filter.

To measure the input frequency, the number of pulses which occur in a defined time must be counted. This defined time is refered to as 'window'. A wide window indicates a long measuring time and therefore a high accuracy. The counter resolution is defined as Hertz per count. Due to the TEA6100 having to measure the IF frequencies of AM and FM, the counter resolution must be adjustable (different channel spacing). The counter resolution depends on the setting of dividers 1 (N1), divider 2 (N2) and the reference frequency (F_{ref}). The divider ratios of N1 and N2 are controlled by software (see section PROGRAMMING INFORMATION). In Table 3 the window and counter resolution has been calculated for a reference frequency of 40 kHz. The accuracy is controlled by bit 7 of the input word. Although the resolution is the same for bit 7 = logic 0 and bit 7 = logic 1, the width of the window doubles when bit 7 = logic 1.

- bit 7 = 0, accuracy = ± counter resolution
- bit 7 = 1, accuracy = $\pm \frac{1}{2}$ counter resolution

Communication between TEA6100 and the microcomputer is via a two wire bidirectional I^2C bus. The power supply lines are fully isolated to avoid cross talk between the digital and analogue parts of the circuit.

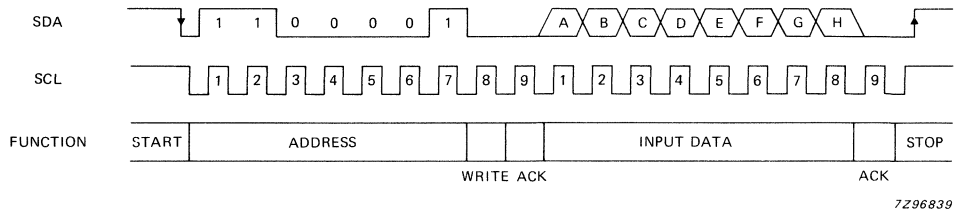


Fig. 3 Input data format waveforms.

Table 2 Input bits

bit	function	logic 0	logic 1	see Figs. 5 and 6
1	reference frequency	32 kHz	40 kHz	A
2	IF mode	AM	FM	B
3	IF input	pin 19	pin 18	C
4	counter input	460 kHz	10,7 MHz	D
5	counter mode	AM	FM	E
6	resolution	divide by 8	divide by 1	F
7	accuracy	LOW	HIGH	G
8	test mode	OFF	ON	H

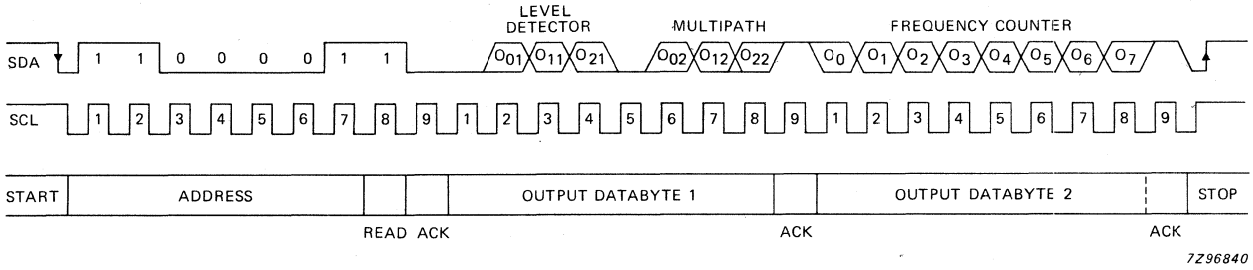


Fig. 4 Output data format waveforms.

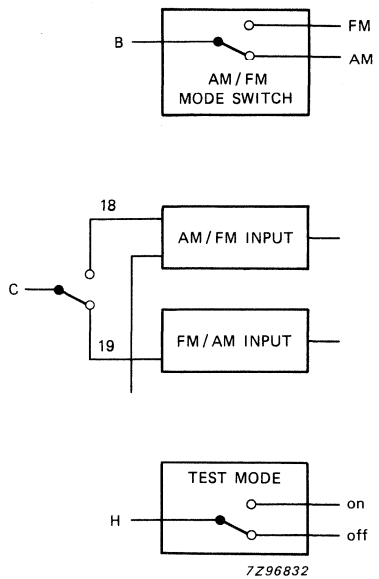


Fig. 5 Switch positions, analogue part (switches drawn in logic 0 state).

DEVELOPMENT DATA

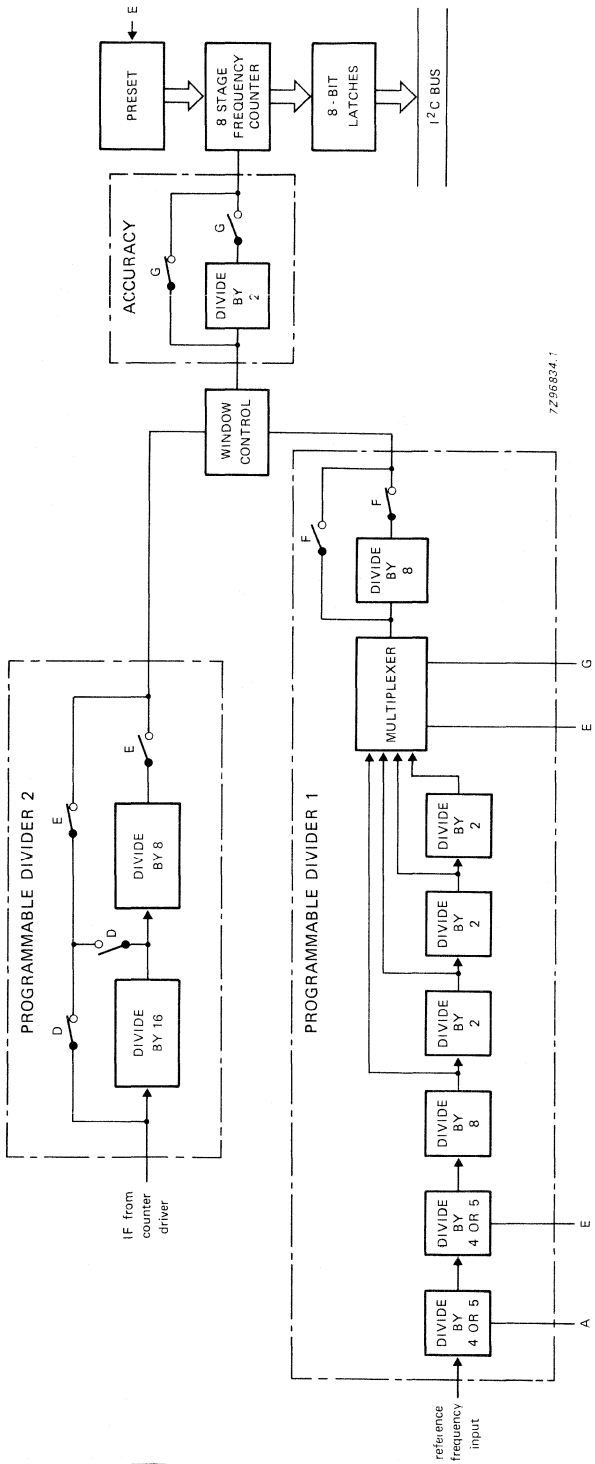


Fig. 6 Switch positions, digital part (switches drawn in logic 0 state, see Tables 2 and 3).

Table 3 Possible window settings and counter resolutions with a 40 kHz reference frequency (see Figs. 5 and 6)

position of switch ADEFG	window (ms)	counter resolution Hz/count	IF frequency (kHz)	read out by IF frequency (hex)	range (kHz)	
					min.	max.
00000	25,6	39,1	460,0	4F	456,914	466,875
10000	32,0	31,3	460,0	CF	453,531	461,500
00001	51,2	39,1	460,0	4F	456,914	466,875
10001	64,0	31,3	460,0	CF	453,531	461,500
00100	128,0	1000,0	460,0	C3	265,000	520,000
10100	160,0	800,0	460,0	36	416,800	620,800
00101	256,0	1000,0	460,0	C3	256,000	520,000
10101	320,0	800,0	460,0	36	416,800	620,800
00010	3,2	312,5	460,0	0F	455,312	535,000
10010	4,0	250,0	460,0	7F	428,250	492,000
00011	6,1	312,5	460,0	0F	455,312	535,000
10011	8,0	250,0	460,0	7F	428,250	492,000
00110	16,0	8000,0	460,0	30	76,000	2116,000
10110	20,0	6400,0	460,0	3F	56,800	1688,800
00111	32,0	8000,0	460,0	30	76,800	2116,000
10111	40,0	6400,0	460,0	3F	56,800	1688,800
01000	25,6	625,0	10700,0	2F	10670,625	10830,000
11000	32,0	500,0	10700,0	E7	10584,500	10712,000
01001	51,2	625,0	10700,0	2F	10670,625	10830,000
11001	64,0	500,0	10700,0	E7	10584,000	10712,000
01100	128,0	1000,0	10700,0	C3	10505,000	10760,000
11100	160,0	800,0	10700,0	36	10656,800	10860,800
01101	256,0	1000,0	10700,0	C3	10505,000	10760,000
11101	320,0	800,0	10700,0	36	10656,800	10860,000
01010	3,2	5000,0	10700,0	AB	9845,000	11120,000
11010	4,0	4000,0	10700,0	C2	9924,000	10944,000
01011	6,4	5000,0	10700,0	AB	9845,000	11120,000
11011	8,0	4000,0	10700,0	C2	9924,000	10944,000
01110	16,0	8000,0	10700,0	30	10316,000	12356,000
11110	20,0	6400,0	10700,0	7F	9887,200	11519,200
01111	32,0	8000,0	10700,0	30	10316,000	12356,000
11111	40,0	6400,0	10700,0	7F	9887,200	11519,200

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage	pins 1 and 8	V_{P1}, V_{P2}	0	13,2	V
Total power dissipation		P_{tot}	see Fig. 7		
Storage temperature range		T_{stg}	−65	+150	°C
Operating ambient temperature range		T_{amb}	−30	+85	°C

THERMAL RESISTANCE

From junction to ambient $R_{th\ j\text{-}a}$ 70 K/W

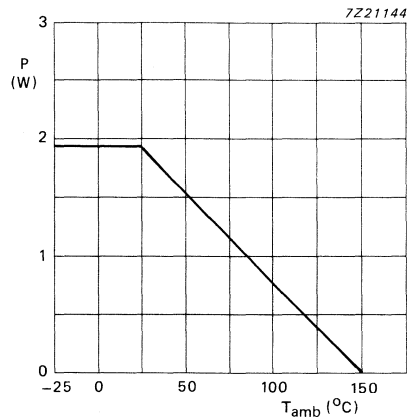


Fig. 7 Power derating curve.

DC CHARACTERISTICS (note)

$V_{P1} = V_{P2} = 8{,}5$ V; $T_{amb} = 25$ °C; all currents positive into the IC; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage	pins 1 and 8	V_{P1}, V_{P2}	7,5	8,5	12	V
Supply current						
FM mode	$V_{ADJ} > 2{,}4$ V	I_{P1}	–	19	25	mA
AM mode	$V_{ADJ} > 2{,}4$ V	I_{P1}	–	15	25	mA
digital part		I_{P2}	–	16	23	mA
Power dissipation		P_d	–	280	–	mW

DEVELOPMENT DATA

AC CHARACTERISTICS (note 1)

V_P = 8,5 V; $V_{i(FM)}$ = 1 mV; f = 10,7 MHz; Δf = 22,5 kHz; f_m = 1 kHz; FM mode; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
IF amplifier, quadrature detector and LF amplifier output	pin 11					
Sensitivity	−3 dB before limiting; inactive mute	$V_{i(FM)}$	–	15	30	μV
Sensitivity	S/N = 26 dB; inactive mute	$V_{i(FM)}$	–	12	–	μV
Signal plus noise to noise ratio	$V_{i(FM)}$ = 10 mV; bandwith = 0,3 to 15 kHz; Δf = 75 kHz	(S + N)/N	–	85	–	dB
IF input range	AM suppression > 40 dB	$V_{i(FM)}$	–	0,09 to 1000	–	mV
Audio output voltage after limiting	Δf = 22,5 kHz	V_o	160	200	240	mV
Total harmonic distortion for single tuned circuit	Δf = 75 kHz	THD	–	0,65	–	%
AM suppression	note 2; see Fig. 8;					
	$V_{i(AM)}$ range = 200 μV to 600 mV	AMS	–	60	–	dB
	$V_{i(AM)}$ range = 200 μV to 600 μV	AMS	–	55	–	dB
Supply voltage ripple rejection	200 Hz; 20 log (V_i/V_o)	SVRR	38	40	–	dB
IF counter inputs						
Frequency counter sensitivity	minimum input voltage for a readout ± 1 bit;					
FM mode	10,7 MHz	$V_{i(FM)}$	–	–	60	μV
AM mode	10,7 MHz	$V_{i(AM)}$	–	–	60	μV
AM mode	460 kHz	$V_{i(AM)}$	–	–	45	μV
Maximum input voltage		V_i	–	–	1	V

DEVELOPMENT DATA

parameter	conditions	symbol	min.	typ.	max.	unit
FM level performance	see Fig. 9					
Output voltage adjustment range	$V_{i(FM)}$ = 0 V; pins 3 and 14	V_{LFM}	–	0,1 to 4,6	–	V
Maximum output voltage	pins 3 and 14	V_{LFM}	V_P–1,5	–	–	V
Adjustable gain	$V_{i(FM)}/V_{ADJ}$	G_{ADJ}	–	–2	–	dB
Level voltage slope	V_{ADJ} = 2,4 V; $V_{i(FM)}$ = 100 to 10 mV	$S_{i(FM)}$	1,4	1,6	1,8	V/dec *
Output impedance of level amplifier	$V_{LFM} > 1$ V	$\lvert Z_o \rvert$	–	100	–	Ω
AM level performance	see Fig. 10					
Output voltage adjustment range	$V_{i(AM)}$ = 0 V; pins 5 and 14	V_{LFM}	–	0,1 to 4,6	–	V
	$V_{i(AM)}$ = 10 mV; pins 5 and 14	V_{LAM}	6	–	–	V
Adjustable gain	$V_{i(AM)}/V_{ADJ}$	G_{ADJ}	–	–2	–	dB
Level voltage slope	V_{ADJ} = 2,4 V; $V_{i(FM)}$ = 100 to 10 mV	$S_{i(AM)}$	1,3	1,5	1,7	V/dec *
IF soft muting	V_{LFM}; pin 3; see Fig. 11					
Mute operating range		V_{LFM}	–	0,1 to 2,5	–	V
Mute voltage	–3 dB output attenuation	V_{LFM}	1,20	1,45	1,75	V
Maximum muting	V_{LFM} = 0,1 V	V_{MUTE}	–	19	–	dB
IF hard muting	V_{MUTE}; pin 2					
Mute voltage	–60 dB output attenuation	V_{MUTE}	–	460	–	mV
Mute discharge current	V_{MUTE} = 1 V; V_{LEVEL} = 0 V; mute ON; pin 2	$+I_2$	–	270	–	μA
Mute charging current	V_{MUTE} = 0 V; mute OFF	$-I_2$	–	1,5	–	μA

* V/dec = voltage per decade.

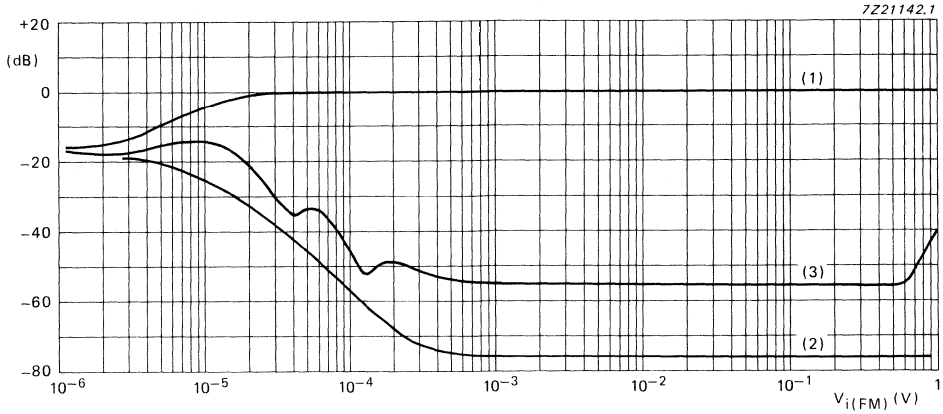
AC CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Rectifier/amplifier						
Input impedance	pin 4	$\|Z_i\|$	7	10	13	kΩ
Conversion gain AC to DC	pins 4 and 5; bandwith = 100 Hz to 120 kHz; 20 log $V_{O(MP)}$ (d.c.)/ $V_{i(MP)}$ (a.c.)	G_A	–	30	–	dB
DC output voltage range		$V_{O(MP)}$	–	0,2 to 6	–	V
Output characteristics	see Fig. 13; note 3					
Discharge current		I_o	–	200	–	μA
Output ripple in AM mode (peak-to-peak value)	f_m = 200 Hz; m = 0,8; $V_{i(AM)}$ range = 100 μV to 30 mV	V_{ripple}	–	300	400	mV
Multi-path output	see Fig. 12; note 4					
Reference voltage output	pin 15, FM only					
Output voltage		V_{ref}	–	4,4	–	V
Output sink current		$+I_{15}$	–	–	1,5	mA
Output impedance		$\|Z_O\|$	–	–	10	Ω
Output charge current		$-I_{15}$	5	–	–	mA
Output voltage	AM mode	V_{ref}	–	0	–	V
Output impedance	AM mode	$\|Z_O\|$	–	14	–	kΩ
I^2C bus data format	see Figs 3 and 4; Table 2					
3-bit ADC	multi-path and level information, note 5					
Trip level LOW		V_{TL}	1,20	1,45	1,75	V
Trip level HIGH		V_{TH}	4,25	4,50	4,75	V
Reference frequency input	pin 6					
Reference range		F_{ref}	–	–	40	kHz
Input voltage LOW		V_{IL}	–	–	0,4	V
Input current HIGH		I_{IH}	5	–	–	μA

Notes to the characteristics

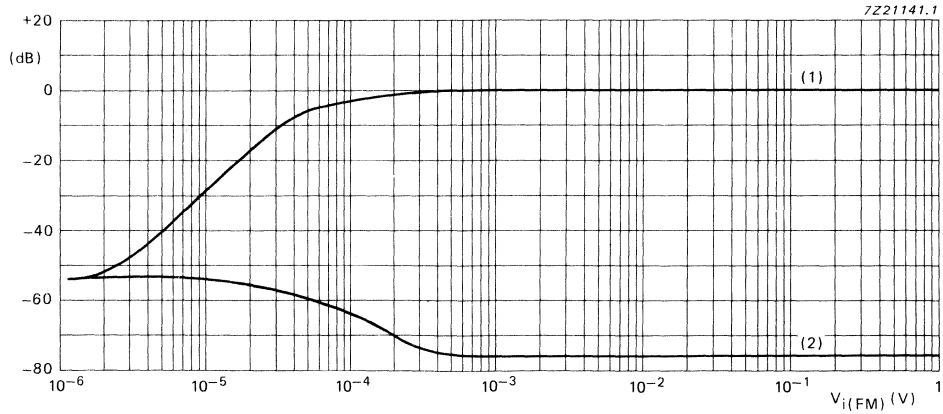
1. All characteristics are measured from the circuit shown in Fig. 13.
2. Conditions for this parameter are:
   20 log $V_{o(FM)}$; m = 0,3 or 20 log $V_{o(AM)}$; m = 0,3.
3. Voltage source followed by diode and resistor.
4. A DC shift can be achieved by connecting a 1,8 MΩ resistor between pin 4 and pin 15.
5. Step size between trip levels:
   $(V_{TH} - V_{TL})/6 \pm 0{,}07$ V.

DEVELOPMENT DATA



(1) Audio (Δf = 22,5 kHz and f_{mod} = 1 kHz) for V_{ADJ} = 0 V.
(2) Noise (with dBA filter) for V_{ADJ} = 0 V.
(3) AM suppression (m = 0,3 and f_{mod} = 1 kHz) for V_{ADJ} = 0 V.

Fig. 8(a) Audio output voltage performance plotted against input signal, $V_{i(FM)}$.



(1) Audio (Δf = 22,5 kHz and f_{mod} = 1 kHz) for V_{ADJ} = 2,4 V.
(2) Noise (with dBA filter) for V_{ADJ} = 2,4 V.

Fig. 8(b) Audio output voltage performance plotted against input signal, $V_{i(FM)}$.

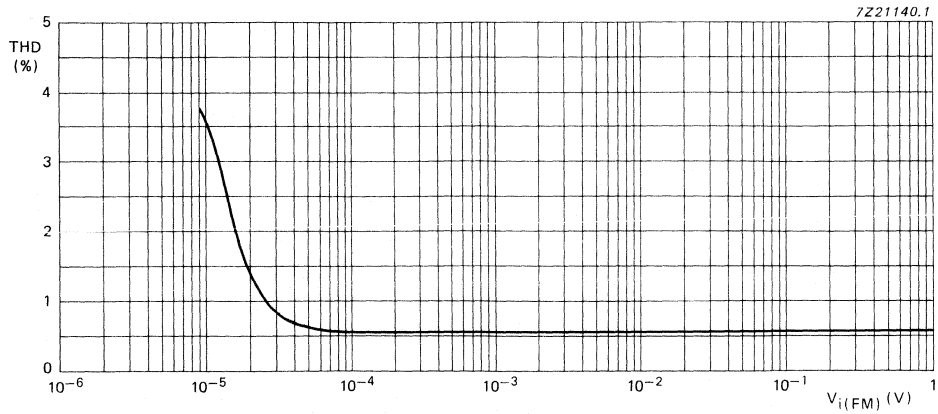
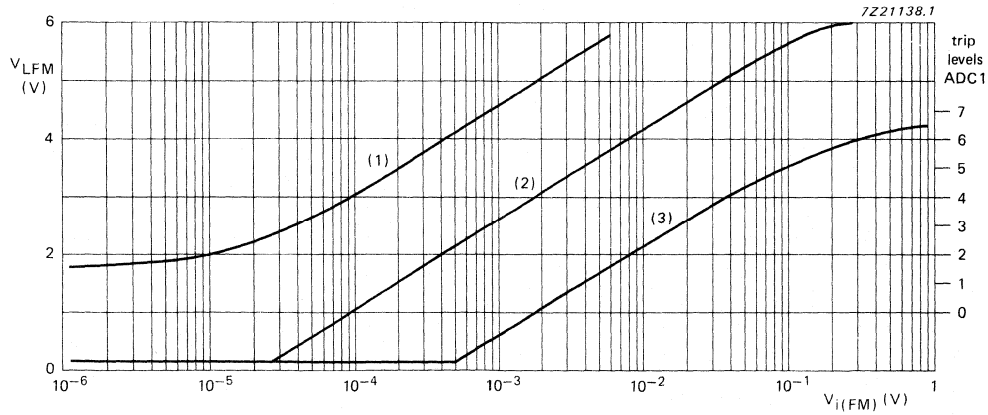
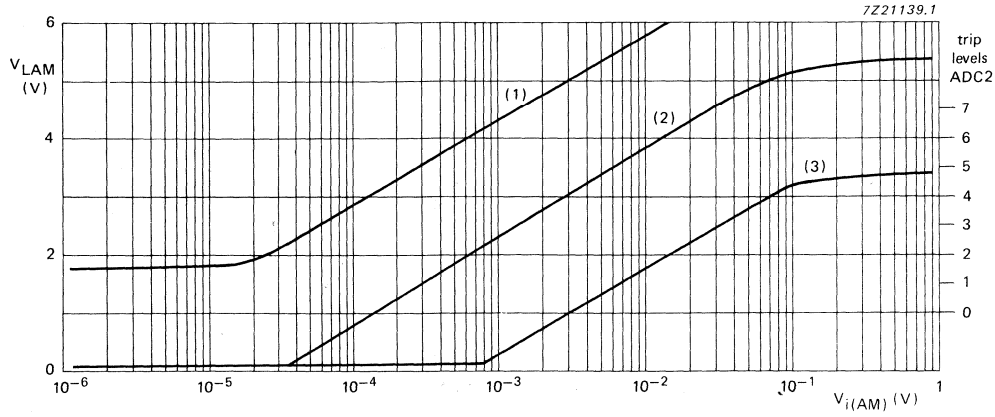


Fig. 8(c) Total harmonic distortion; Δf = 75 kHz, f_{mod} = 1 kHz and V_{ADJ} = 0 V.



(1) V_{ADJ} = 1,4 V.
(2) V_{ADJ} = 2,4 V.
(3) V_{ADJ} = 3,4 V.

Fig. 9 Level voltage output (V_{LFM}) plotted against IF input signal, $V_{i(FM)}$; IF = 10,7 MHz.



(1) V_{ADJ} = 1,4 V.
(2) V_{ADJ} = 2,4 V.
(3) V_{ADJ} = 3,4 V.

Fig. 10 Level voltage output (V_{LAM}) plotted against IF input signal, $V_{i(AM)}$; IF = 10,7 MHz or 460 kHz.

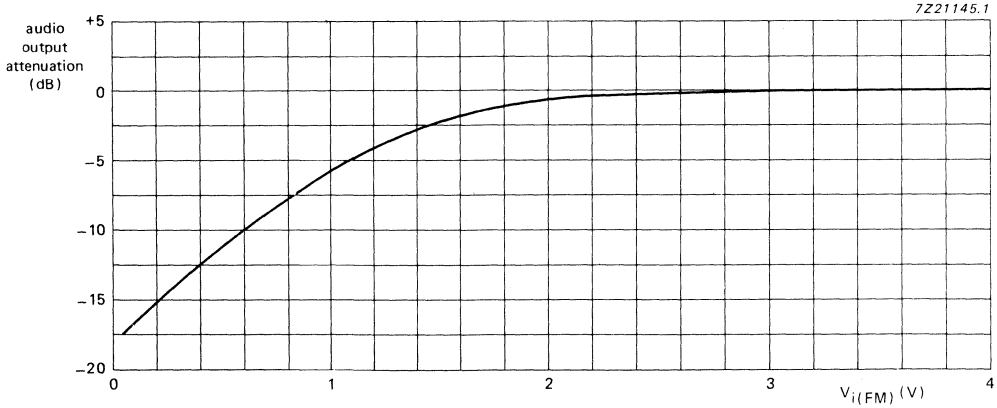
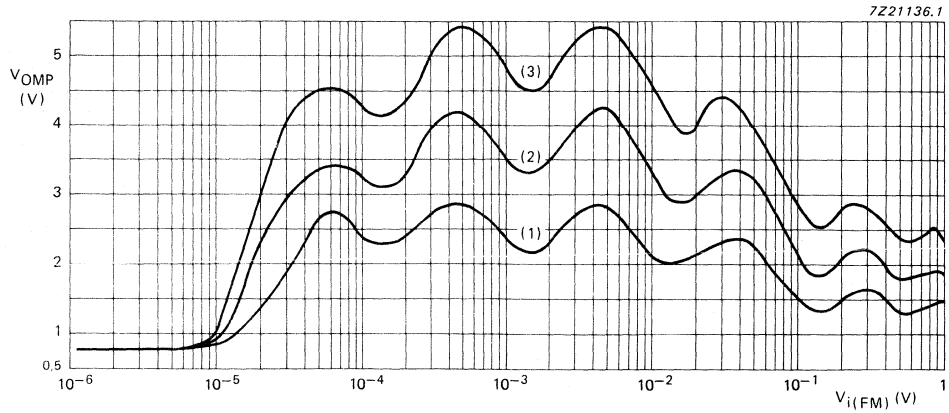


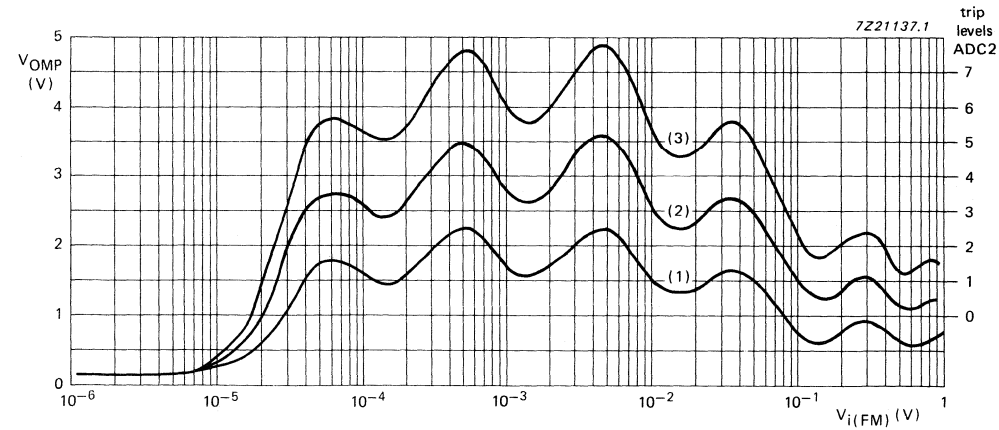
Fig. 11 Soft muting plotted against level output voltage; $V_{i(FM)}$ = 1 mV and Δf = 22,5 kHz.



(1) mod = 0,2
(2) mod = 0,3
(3) mod = 0,4

Fig. 12(a) Multi-path output plotted against IF input signal, $V_{i(FM)}$; f_{mod} = 3 kHz (AM, no FM modulation), V_{ADJ} = 2,4 V and 1,8 MΩ resistor connected between pin 4 and pin 15.

DEVELOPMENT DATA



(1) mod = 0,2
(2) mod = 0,3
(3) mod = 0,4

Fig. 12(b) Multi-path output plotted against IF input signal, $V_{i(FM)}$; f_{mod} = 3 kHz (AM, no FM modulation), V_{ADJ} = 2,4 V.

APPLICATION INFORMATION

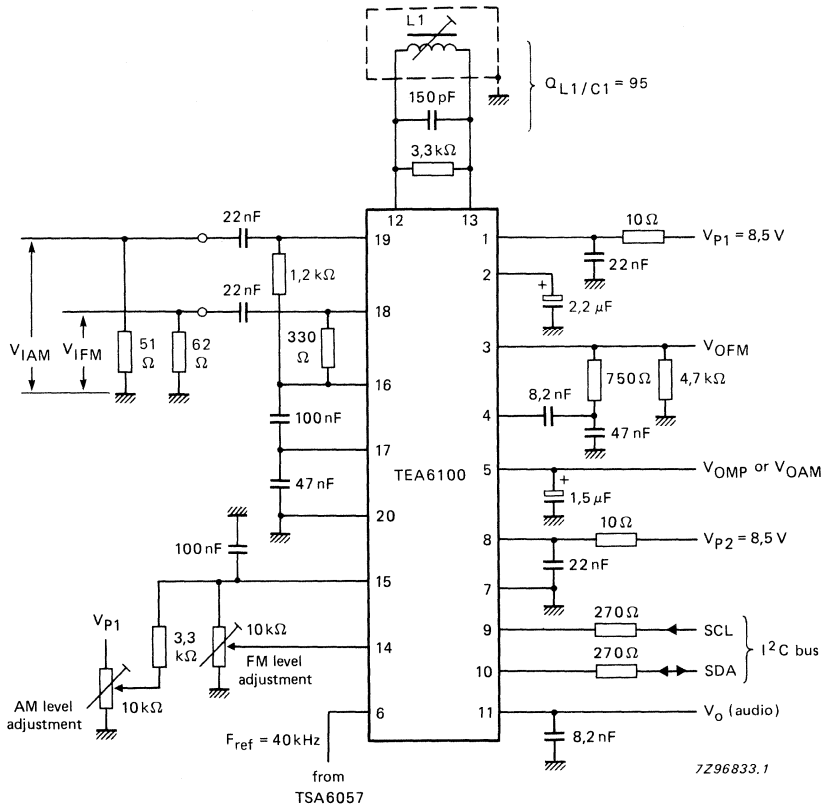


Fig. 13 Application diagram.

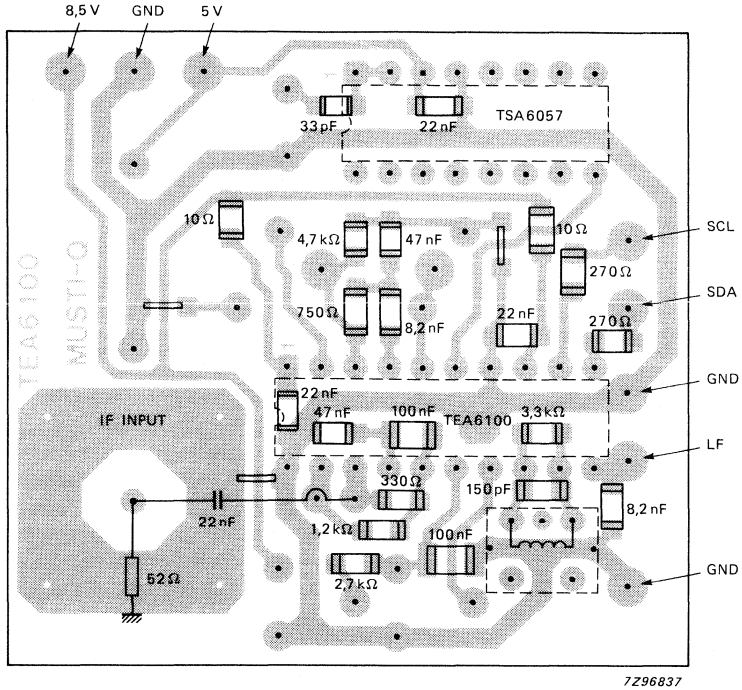


Fig. 14 Track side of printed circuit board.

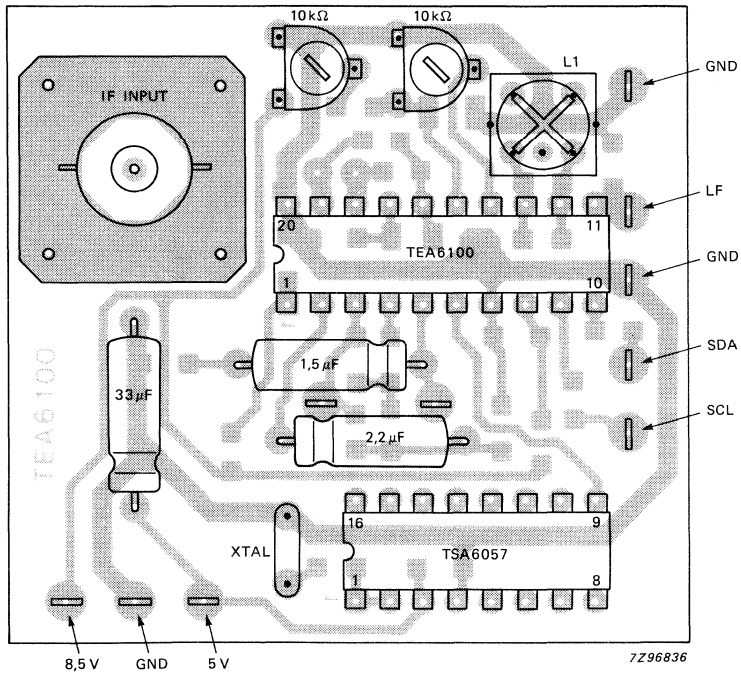
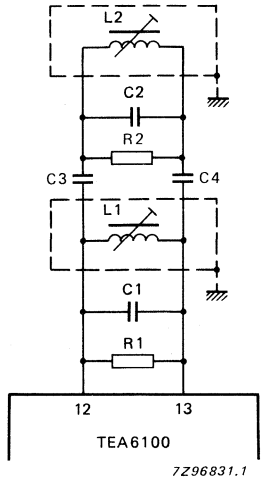


Fig. 15 Component side of printed circuit board.

Double tuned circuit



R1 = 5,1 kΩ, R2 = 1,5 kΩ
C1 = C2 = 150 pF (n = 220)
C3 = C4 = 10 pF
L1 = L2 = 1,6 μH

Fig. 16 Double tuned demodulator circuit.

Alignment of the circuit is obtained with an IF input signal > 200 μV. Tuning the circuit is performed by, detuning L2, adjusting L1 to obtain a minimum distortion level and then adjusting L2 to obtain a minimum distortion level.

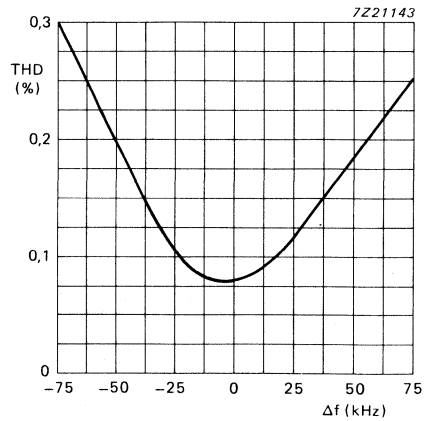


Fig. 17 Total harmonic distortion plotted against IF detuning; for $\Delta f = \pm 75$ kHz, $f_{mod} = 1$ kHz and $V_O = 500$ mV.

PROGRAMMING INFORMATION

Converting the read out of the counters into frequency

The counter resolution at the input is defined as:

- resolution = divider ratio of N2/window

For every increment of the counter the counted frequency increases relative to the resolution in Hertz, as shown in example:

- window = 20 ms; N2 = 128; IF frequency = 10,7 MHz; resolution = 128/0,02 = 6,4 kHz per count

The counter consists of 8 bits. Therefore, the maximum frequency range that can be counted is 256 x resolution = 1,6384 MHz. In the example the frequency to be counted is 10,7 MHz, therefore, the counter will overflow (in the example above, 7 times). The real measured frequency is:

- f_{real} = (read out + overflow x 256) x resolution

The overflow indicates the off-set on the frequency scale which must be added to the read out. Due to the bandwidth of the IF filter, the frequencies at the input to the TEA6100 are known, for example:

- IF filter for FM has a center frequency of 10,7 MHz and −3 dB bandwidth of 300 kHz. Only the frequencies of 10,7 MHz ± 150 kHz occur at the input of the TEA6100. For this reason it is not necessary to count the overflow.

The read out of the counter has to be translated into frequency. This translation depends upon the counter resolution. The preferred way to calculate the input frequency is to:

- calculate the read out of the target IF frequency. Compare this value with that of the measured read out and multiply the difference by the resolution.

The formulae for calculating the target IF read out and the resolution are as follows (A, D, E, F and G refer to the bits of the I^2C bus input data as shown in Figs 3 and 4 and to the counter/timer block diagram shown in Fig. 6. An, Dn, En, Fn and Gn are inverted values of the variables A, D, E, F and G. Table 3 shows the following formulae calculated for a reference frequency of 40 kHz):

- N1 = (An x 4 + A x 5) x (En x 4 + E x 5) x 8 x ($2^{[E \times 2 + G \times 1]}$) x (F x 1 + Fn x 8)
- Window (T) = $N1/F_{ref}$
- N2 = (E x 16 x 8 + En x [Dn x 1 + D x 16]) x (G x 2 + Gn x 1)
- Target decimal read out (TDEC) = T x (TIFF/N2 + (E x 247 + En x 79). TIFF is the symbol for target IF frequency
- Target read out hexadecimal (THEX), convert the target decimal read out to hexadecimal and use the 2 least significant digits (Do not use overflow value). The symbol for measured hexadecimal is MHEX
- Resolution (R) = N2/T
- Measured frequency (F_1) = (TIFF) + R x (MHEX − THEX)

Note

Care should be taken if TIFF + $\frac{1}{2}$ filter bandwidth is greater than the frequency for the read out of hexadecimal value FF, or if TIFF − $\frac{1}{2}$ filter bandwith is less than the frequency at read out for hexadecimal value 00.

- Counter accuracy (AW and AN), with bit 7 (G) the accuracy can be chosen with the same resolution. If bit 7 is logic 1 the accuracy is HIGH and if bit 7 is logic 0 then the accuracy is LOW.

  bit 7 = 0, AN = ± (N2/T)
  bit 7 = 1, AW = ± ($\frac{1}{2}$ x N2/T)

DEVELOPMENT DATA

Example

The example uses the following values:

TIFF = 10,7 MHz; accuracy = LOW (G = 0); F_{ref} = 40 kHz (A = 1); IF frequency = 10, 7 MHz (D = 1); resolution = N1 (F = 1) and counter mode = FM (E = 1)

N1 = (0 x 4 + 1 x 5) x (0 x 4 + 1 x 5) x 8 x ($2^{[1 \times 2 + 0 \times 1]}$) x (1 x 1 + 0 x 8) = 800

T = 800/40 = 20 ms

N2 = (1 x 16 x 8 + 0 x [1 x 1 + 0 x 16]) x (0 x 2 + 1 x 1) = 128

TDEC = 20 x 10,7/128 + (1 x 247 + 0 x 79) = 1919

THEX; 1919 is hexadecimal 77F and the least significant 2 digits are 7F, so THEX = 7 F

R = 128/20 = 6400 Hz/count

Assume the readout is '6E', the measured frequency will be:

- F_I = 10,7 + (6E − 7F) x 6400 = 10,59 MHz

Assume the readout is '83', the measured frequency will be:

- F_I = 10,7 + (83 − 7F) x 6400 = 10,726

SOUND FADER CONTROL CIRCUIT

GENERAL DESCRIPTION

The Sound Fader Control circuit (SOFAC) is an I²C bus controlled preamplifier for car radios.

Features

- Source selector for three stereo inputs
- Inputs and outputs for noise reduction circuits
- Volume and balance control; control range of 86 dB in steps of 2 dB
- Bass and treble control; from + 15 dB (treble 12 dB) to −12 dB in steps of 3 dB
- Fader control; from 0 dB to −30 dB in steps of 2 dB
- Fast muting
- Low noise suitable for DOLBY* noise reduction
- Signal handling suitable for compact disc
- Pop-free on/off switching
- I²C bus control for all functions

QUICK REFERENCE DATA

parameter	symbol	min.	typ.	max.	unit
Supply voltage	V_{CC}	7,0	8,5	13,2	V
Input sensitivity for full power at the output stage	$V_{i(rms)}$	–	50	–	mV
Input signal handling	$V_{i(rms)}$	–	1,65	–	V
Frequency response	f_r	35	–	20 000	Hz
Channel separation f = 250 Hz to 10 kHz	α_{CS}	–	70	–	dB
Total harmonic distortion	THD	–	0,05	–	%
Signal plus noise-to-noise ratio	(S+N)/N	–	80	–	dB
Operating ambient temperature range	T_{amb}	−40	–	+ 85	°C

* Dolby is a registered trademark of Dolby Laboratories Licencing Corporation, San Fransisco, California (U.S.A.).

PACKAGE OUTLINES

28-lead dual in-line; plastic (with internal heat spreader) (SOT-117).
28-lead mini-pack; plastic (SO-28; SOT-136A).

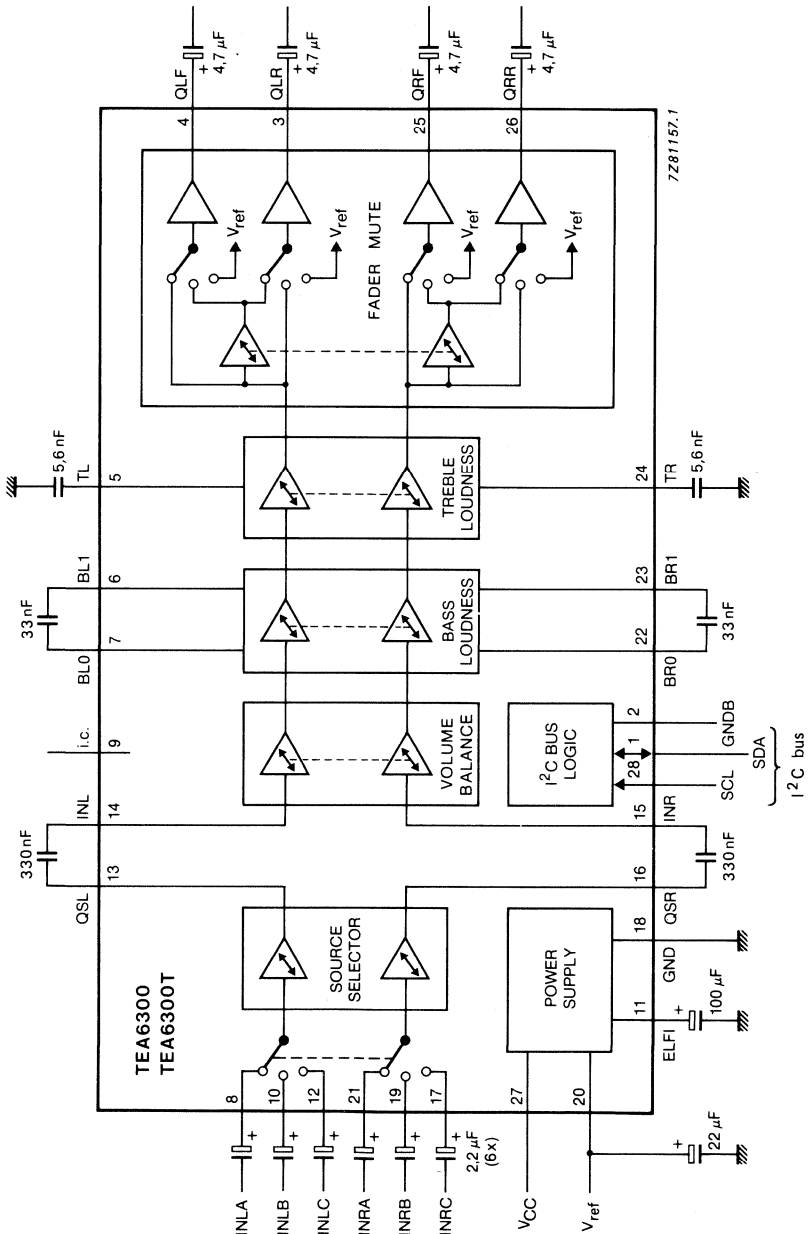


Fig. 1 Block diagram.

DEVELOPMENT DATA

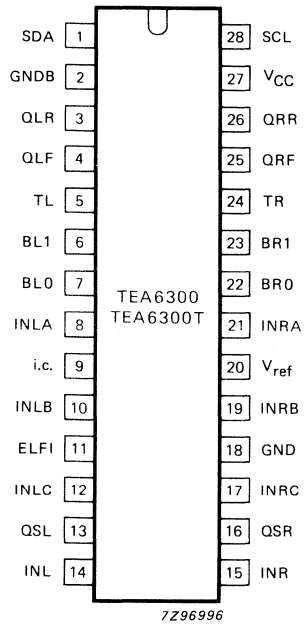


Fig. 2 Pinning diagram.

PINNING

1	SDA	serial data input/output (I^2C bus)
2	GNDB	ground for I^2C bus terminals
3	QLR	output left rear
4	QLF	output left front
5	TL	treble control capacitor; left channel
6	BL1	bass control capacitor; left channel
7	BL0	bass control capacitor; left channel
8	INLA	input left source A
9	i.c.	internally connected
10	INLB	input left source B
11	ELFI	electronic filtering for supply
12	INLC	input left source C
13	QSL	output source selector left
14	INL	input left control part
15	INR	input right control part
16	QSR	output source selector right
17	INRC	input right source C
18	GND	ground
19	INRB	input right source B
20	V_{ref}	reference voltage (1/2 V_{CC})
21	INRA	input right source A
22	BR0	bass control capacitor; right channel
23	BR1	bass control capacitor; right channel
24	TR	treble control capacitor; right channel
25	QRF	output right front
26	QRR	output right rear
27	V_{CC}	supply voltage
28	SCL	serial clock input (I^2C bus)

FUNCTIONAL DESCRIPTION

The source selector selects three stereo channels —RF part (AM/FM), recorder and compact disc. As the outputs of the source selector and the inputs of the main control part are available, additional circuits such as compander and equalizer systems may be inserted into the signal path. The AC signal setting is performed by resistor chains in combination with multi-input operational amplifiers. The advantage of this principle is the combination of low noise, low distortion and a high dynamic range for the circuit.

The separate volume controls of the left and the right channel facilitate correct balance control. The range and balance control is software programmable.

Because the TEA6300 has four outputs a low-level fader is included. The fader control is independent of the volume control and an extra mute position is built in for the front, the rear or for all channels. The last function may be used for muting during preset selection. An extra pop suppression circuit is available for pop-free switching on and off. As all switching and control functions are controllable via the two-line I^2C bus, no external interface between the microcomputer and the TEA6300 is required.

The on-chip power-on-reset sets the TEA6300 to the general mute mode.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	typ.	max.	unit
Supply voltage (pin 27-18)	V_{CC}	–	–	16	V
Maximum power dissipation	P_{tot}	–	–	2	W
Storage temperature range	T_{stg}	−55	–	+ 150	°C
Operating ambient temperature range	T_{amb}	−40	–	+ 85	°C

DEVELOPMENT DATA

CHARACTERISTICS

V_{CC} = 8,5 V; R_S = 600 Ω; R_L = 10 kΩ; f = 1 kHz; T_{amb} = 25 °C; test circuit Fig. 10; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply voltage	V_{CC}	7,0	8,5	13,2	V
Supply current	I_{CC}	–	26	–	mA
Internal reference voltage (pin 20) V_{ref} = 0,5 V_{CC}	V_{REF}	–	4,25	–	V
Maximum voltage gain bass and treble linear, fader off	G_v	–	20	–	dB
Output voltage level (r.m.s. value)					
for P_{max} at the output stage	$V_{o(rms)}$	–	500	–	mV
for start of clipping	$V_{o(rms)}$	–	1000	–	mV
Input sensitivity at V_o = 500 mV	$V_{i(rms)}$	–	50	–	mV
Frequency response bass and treble linear; roll-off frequency −1 dB	f_r	35	–	20 000	Hz
Channel separation G_v = 0 dB; bass and treble linear; frequency range 250 Hz to 10 kHz	α_{CS}	45	70	–	dB
Total harmonic distortion frequency range 20 Hz to 12,5 kHz					
V_i = 50 mV; G_v = 20 dB	THD	–	0,1	0,3	%
V_i = 500 mV; G_v = 0 dB	THD	–	0,05	0,2	%
V_i = 1,6 V; G_v = −10 dB	THD	–	0,2	0,5	%
Ripple rejection $V_{r(rms)} < 200$ mV; G_v = 0 dB; bass and treble linear;					
at f = 100 Hz	RR_{100}	–	70	–	dB
at f = 40 Hz to 12,5 kHz	RR_{range}	–	*	–	dB

* Value to be fixed.

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Signal plus noise-to-noise ratio bass and treble linear; notes 1 and 2 CCIR 468-2 weighted; quasi peak					
V_i = 50 mV; V_o = 46 mV; P_o = 50 mW	(S + N)/N	–	65	–	dB
V_i = 500 mV; V_o = 45 mV; P_o = 50 mW	(S + N)/N	–	67	–	dB
V_i = 50 mV; V_o = 200 mV; P_o = 1 W	(S + N)/N	*	70	–	dB
V_i = 500 mV; V_o = 200 mV; P_o = 1 W	(S + N)/N	*	78	–	dB
V_i = 50 mV; V_o = 500 mV; P_o = 6 W	(S + N)/N	–	70	–	dB
V_i = 500 mV; V_o = 500 mV; P_o = 6 W	(S + N)/N	–	85	–	dB
Noise output power mute position, only contribution of TEA6300; power amplifier for 25 W	P_{no}	–	–	10	nW
Crosstalk (20 log $V_{bus(p-p)}/V_{o(rms)}$) between bus inputs and signal outputs G_V = 0 dB; bass and treble linear	α_B	–	110	–	dB
Source selector					
Input impedance	Z_i	20	30	40	kΩ
Output impedance	Z_o	–	–	100	Ω
Allowable output load resistance	R_L	10	–	–	kΩ
Allowable output load capacity	C_L	0	–	200	pF
Input isolation not selected source; frequency range 40 Hz to 12,5 kHz	α_S	–	80	–	dB
Voltage gain $R_L \geqslant 10$ kΩ	G_v	–	0	–	dB
Internal bias voltage ratio	$V_{b\,int}/V_{ref}$	–	1	–	
Maximum input voltage level (r.m.s. value)					
THD < 0,5%	$V_{i(rms)}$	–	1,65	–	V
THD < 0,5%; V_{CC} = 7,5 V	$V_{i(rms)}$	–	1,5	–	V
Total harmonic distortion V_i = 500 mV; R_L = 10 kΩ	THD	–	–	0,1	%
Noise output voltage weighted CCIR 468-2, quasi peak	V_{no}	–	9	20	μV
DC offset voltage between any inputs	V_o	–	–	10	mV
Control part					
Source selector disconnected, source resistance 600 Ω					
Input impedance	Z_i	35	50	65	kΩ
Output impedance	Z_o	–	100	150	Ω
Allowable output load resistance	R_L	10	–	–	kΩ
Allowable output load capacity	C_L	0	–	1000	pF

parameter	symbol	min.	typ.	max.	unit
Maximum input voltage THD < 0,5%; G_v = −10 dB; bass and treble linear	$V_{i(rms)}$	–	2,0	–	V
Noise output voltage weighted acc CCIR 468-2, quasi peak, bass and treble linear, fader off					
G_v = 20 dB	V_{no}	–	110	220	μV
G_v = 0 dB	V_{no}	–	25	50	μV
G_v = −66 dB	V_{no}	–	19	38	μV
mute position	V_{no}	–	11	22	μV
Volume control					
Continuous control range	G_c	–	86	–	dB
Step resolution		–	2	–	dB
Attenuator set error (G_v = + 20 to −50 dB)	ΔG_a	–	–	2	dB
Attenuator set error (G_v = + 20 to −66 dB)	ΔG_a	–	–	3	dB
Gain tracking error balance in mid position, bass and treble linear	ΔG_t	–	–	2	dB
Mute attenuation	α_m	–	80	–	dB
Bass control					
Bass control range					
f = 40 Hz; maximum boost	$+G_b$	+14	+15	+16	dB
f = 40 Hz; maximum attenuation	$-G_b$	−11	−12	−13	dB
Step resolution		–	3	–	dB
Step error		–	–	0,5	dB
Treble control					
Treble control range					
f = 15 kHz; maximum boost	$+G_t$	+11	+12	+13	dB
f = 15 kHz; maximum attenuation	$-G_t$	−11	−12	−13	dB
f > 15 kHz; maximum boost	G_t	–	–	15	dB
Step resolution		–	3	–	dB
Step error		–	–	0,5	dB

DEVELOPMENT DATA

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Fader control					
Continuous attenuation fader control range	G_f	–	30	–	dB
Step resolution		–	2	–	dB
Attenuator set error		–	–	1,5	dB
Mute attenuation	α_m	–	80	–	dB
Digital part					
Bus terminals					
Input voltage					
HIGH	V_{IH}	3	–	12	V
LOW	V_{IL}	−0,3	–	1,5	V
Input current					
HIGH	I_{IH}	−10	–	10	μA
LOW	I_{IL}	−10	–	10	μA
Output voltage LOW I_L = 3 mA	V_{OL}	–	–	0,4	V
AC characteristics					
in accordance with the I^2C bus specification					
Power-on-Reset					
When RESET is active the GMU (general mute) bit is set and the I^2C bus receiver is in RESET position					
Increasing supply voltage					
start of reset	V_{CC}	–	–	2,5	V
end of reset	V_{CC}	5,2	6,0	6,8	V
Decreasing supply voltage					
start of reset	V_{CC}	4,2	5,0	5,8	V

Notes to the characteristics

1. The indicated values for output power assume a 6 W power amplifier with 20 dB gain, connected to the output of the circuit. Signal to noise ratios exclude noise contribution of the power amplifier.
2. Signal-to-noise ratios on a CCIR 468-2 average reading-meter are 4,5 dB better than on CCIR 468-2 quasi peak.

I²C BUS FORMAT

S	SLAVE ADDRESS	A	SUBADDRESS	A	DATA	A	P

S = start condition
SLAVE ADDRESS = 1000 0000
A = acknowledge, generated by the slave
SUBADDRESS = see Table 1
DATA = see Table 1
P = STOP condition

If more than 1 byte of DATA is transmitted, then auto-increment of the subaddress is performed.

Table 1 I²C bus; subaddress/data

function	subaddress	DATA							
		D7	D6	D5	D4	D3	D2	D1	D0
volume left	0 0 0 0 0 0 0 0	X	X	VL5	VL4	VL3	VL2	VL1	VL0
volume right	0 0 0 0 0 0 0 1	X	X	VR5	VR4	VR3	VR2	VR1	VR0
bass	0 0 0 0 0 0 1 0	X	X	X	X	BA3	BA2	BA1	BA0
treble	0 0 0 0 0 0 1 1	X	X	X	X	TR3	TR2	TR1	TR0
fader	0 0 0 0 0 1 0 0	X	X	MFN	FCH	FA3	FA2	FA1	FA0
switch	0 0 0 0 0 1 0 1	GMU	X	X	X	X	SCC	SCB	SCA

Function of the bits:

VL0 to VL5	volume control left
VR0 to VR5	volume control right
BA0 to BA3	bass control
TR0 to TR3	treble control
FA0 to FA3	fader control
FCH	select fader channel (front or rear)
MFN	mute control of the selected fader channel (front or rear)
SCA to SCC	source selector control
GMU	mute control (general mute) for the outputs QLF, QLR, QRF and QRR
X	don't care bits (logic 1 during testing)

DEVELOPMENT DATA

Table 2 Bass setting

G_V dB	DATA			
	BA3	BA2	BA1	BA0
+15	1	1	1	1
+15	1	1	1	0
+15	1	1	0	1
+15	1	1	0	0
+12	1	0	1	1
+ 9	1	0	1	0
+ 6	1	0	0	1
+ 3	1	0	0	0
0	0	1	1	1
− 3	0	1	1	0
− 6	0	1	0	1
− 9	0	1	0	0
−12	0	0	1	1
−12	0	0	1	0
−12	0	0	0	1
−12	0	0	0	0

Table 3 Treble setting

G_V dB	DATA			
	TR3	TR2	TR1	TR0
+12	1	1	1	1
+12	1	1	1	0
+12	1	1	0	1
+12	1	1	0	0
+12	1	0	1	1
+ 9	1	0	1	0
+ 6	1	0	0	1
+ 3	1	0	0	0
0	0	1	1	1
− 3	0	1	1	0
− 6	0	1	0	1
− 9	0	1	0	0
−12	0	0	1	1
−12	0	0	1	0
−12	0	0	0	1
−12	0	0	0	0

DEVELOPMENT DATA

Table 4 Volume setting LEFT

G_V dB	DATA					
	VL5	VL4	VL3	VL2	VL1	VL0
20	1	1	1	1	1	1
18	1	1	1	1	1	0
16	1	1	1	1	0	1
14	1	1	1	1	0	0
12	1	1	1	0	1	1
10	1	1	1	0	1	0
8	1	1	1	0	0	1
6	1	1	1	0	0	0
4	1	1	0	1	1	1
2	1	1	0	1	1	0
0	1	1	0	1	0	1
− 2	1	1	0	1	0	0
− 4	1	1	0	0	1	1
− 6	1	1	0	0	1	0
− 8	1	1	0	0	0	1
−10	1	1	0	0	0	0
−12	1	0	1	1	1	1
−14	1	0	1	1	1	0
−16	1	0	1	1	0	1
−18	1	0	1	1	0	0
−20	1	0	1	0	1	1
−22	1	0	1	0	1	0
−24	1	0	1	0	0	1
−26	1	0	1	0	0	0
−28	1	0	0	1	1	1
−30	1	0	0	1	1	0
−32	1	0	0	1	0	1
−34	1	0	0	1	0	0
−36	1	0	0	0	1	1
−38	1	0	0	0	1	0
−40	1	0	0	0	0	1
−42	1	0	0	0	0	0
−44	0	1	1	1	1	1
−46	0	1	1	1	1	0
−48	0	1	1	1	0	1
−50	0	1	1	1	0	0
−52	0	1	1	0	1	1
−54	0	1	1	0	1	0
−56	0	1	1	0	0	1
−58	0	1	1	0	0	0
−60	0	1	0	1	1	1
−62	0	1	0	1	1	0
−64	0	1	0	1	0	1
−66	0	1	0	1	0	0
mute left	0	1	0	0	1	1
mute left	0	1	0	0	1	0
.				.		
.				.		
.				.		
mute left	0	0	0	0	0	0

Table 5 Volume setting RIGHT

G_V dB	DATA					
	VR5	VR4	VR3	VR2	VR1	VR0
20	1	1	1	1	1	1
18	1	1	1	1	1	0
16	1	1	1	1	0	1
14	1	1	1	1	0	0
12	1	1	1	0	1	1
10	1	1	1	0	1	0
8	1	1	1	0	0	1
6	1	1	1	0	0	0
4	1	1	0	1	1	1
2	1	1	0	1	1	0
0	1	1	0	1	0	1
− 2	1	1	0	1	0	0
− 4	1	1	0	0	1	1
− 6	1	1	0	0	1	0
− 8	1	1	0	0	0	1
−10	1	1	0	0	0	0
−12	1	0	1	1	1	1
−14	1	0	1	1	1	0
−16	1	0	1	1	0	1
−18	1	0	1	1	0	0
−20	1	0	1	0	1	1
−22	1	0	1	0	1	0
−24	1	0	1	0	0	1
−26	1	0	1	0	0	0
−28	1	0	0	1	1	1
−30	1	0	0	1	1	0
−32	1	0	0	1	0	1
−34	1	0	0	1	0	0
−36	1	0	0	0	1	1
−38	1	0	0	0	1	0
−40	1	0	0	0	0	1
−42	1	0	0	0	0	0
−44	0	1	1	1	1	1
−46	0	1	1	1	1	0
−48	0	1	1	1	0	1
−50	0	1	1	1	0	0
−52	0	1	1	0	1	1
−54	0	1	1	0	1	0
−56	0	1	1	0	0	1
−58	0	1	1	0	0	0
−60	0	1	0	1	1	1
−62	0	1	0	1	1	0
−64	0	1	0	1	0	1
−66	0	1	0	1	0	0
mute right	0	1	0	0	1	1
mute right	0	1	0	0	1	0
.				.		
.				.		
.				.		
mute right	0	0	0	0	0	0

Table 6 Fader function

setting		DATA					
front dB	rear dB	MFN	FCH	FA3	FA2	FA1	FA0
		fader off					
0	0	1	1	1	1	1	1
0	0	0	1	1	1	1	1
		fader front					
− 2	0	1	1	1	1	1	0
− 4	0	1	1	1	1	0	1
− 6	0	1	1	1	1	0	0
− 8	0	1	1	1	0	1	1
−10	0	1	1	1	0	1	0
−12	0	1	1	1	0	0	1
−14	0	1	1	1	0	0	0
−16	0	1	1	0	1	1	1
−18	0	1	1	0	1	1	0
−20	0	1	1	0	1	0	1
−22	0	1	1	0	1	0	0
−24	0	1	1	0	0	1	1
−26	0	1	1	0	0	1	0
−28	0	1	1	0	0	0	1
−30	0	1	1	0	0	0	0
		mute front					
−80	0	0	1	1	1	1	0
.	.			.			
.	.			.			
.	.			.			
−80	0	0	1	0	0	0	0

setting		DATA					
front dB	rear dB	MFN	FCH	FA3	FA2	FA1	FA0
		fader off					
0	0	1	0	1	1	1	1
0	0	0	0	1	1	1	1
		fader rear					
0	− 2	1	0	1	1	1	0
0	− 4	1	0	1	1	0	1
0	− 6	1	0	1	1	0	0
0	− 8	1	0	1	0	1	1
0	−10	1	0	1	0	1	0
0	−12	1	0	1	0	0	1
0	−14	1	0	1	0	0	0
0	−16	1	0	0	1	1	1
0	−18	1	0	0	1	1	0
0	−20	1	0	0	1	0	1
0	−22	1	0	0	1	0	0
0	−24	1	0	0	0	1	1
0	−26	1	0	0	0	1	0
0	−28	1	0	0	0	0	1
0	−30	1	0	0	0	0	0
		mute rear					
0	−80	0	0	1	1	1	0
.	.			.			
.	.			.			
.	.			.			
0	−80	0	0	0	0	0	0

Table 7 Selected inputs

selected inputs	DATA SCC	SCB	SCA
data not allowable	1	1	1
data not allowable	1	1	0
data not allowable	1	0	1
INLC, INRC	1	0	0
data not allowable	0	1	1
INLB, INRB	0	1	0
INLA, INRA	0	0	1
data not allowable	0	0	0

Table 8 Mute control

MUTE control	DATA GMU	remarks
active	1	outputs QLF, QLR QRF and QRR are muted
passive	0	no general mute

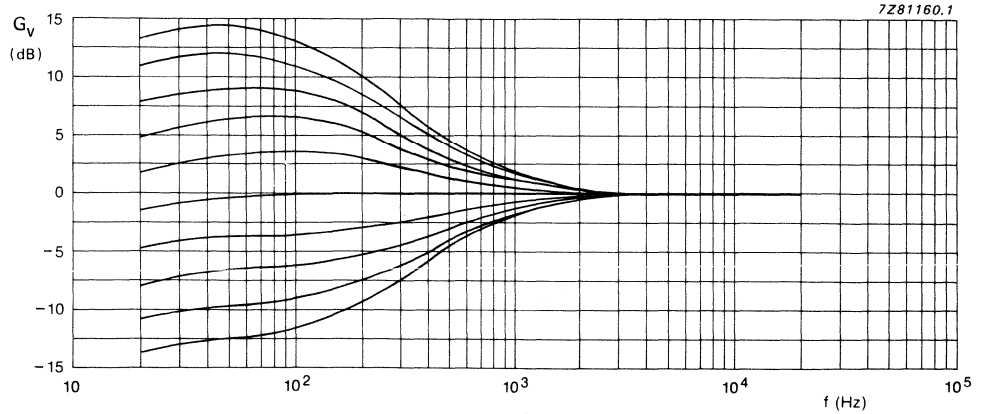


Fig. 3 Bass control without T-pass filter.

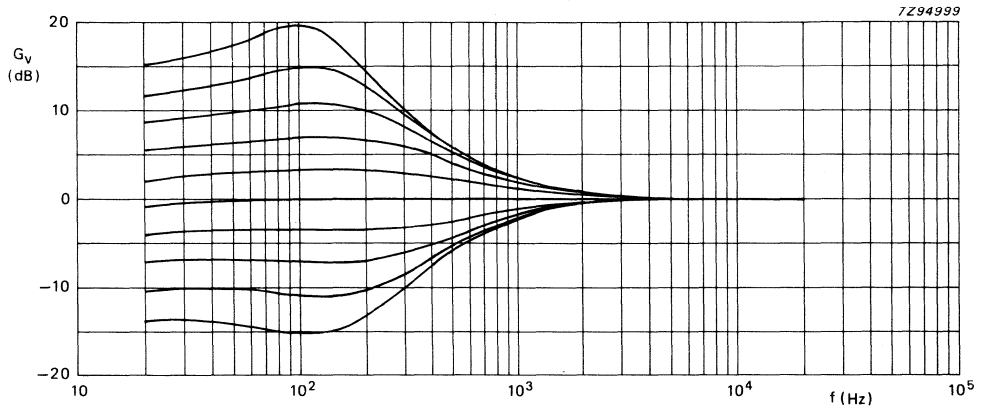
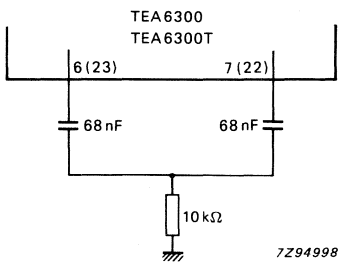


Fig. 4 Bass control with T-pass filter.



Pin numbers in parenthases refer to the bass control, right channel.

Fig. 5 T-pass filter.

DEVELOPMENT DATA

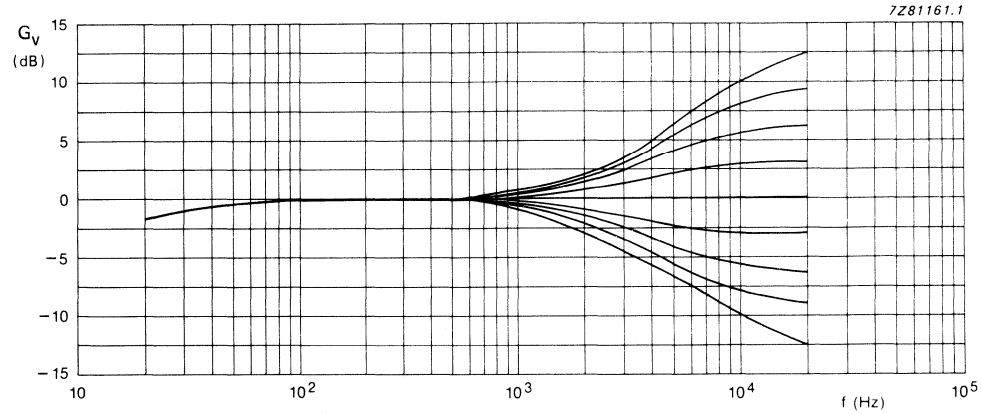


Fig. 6 Treble control.

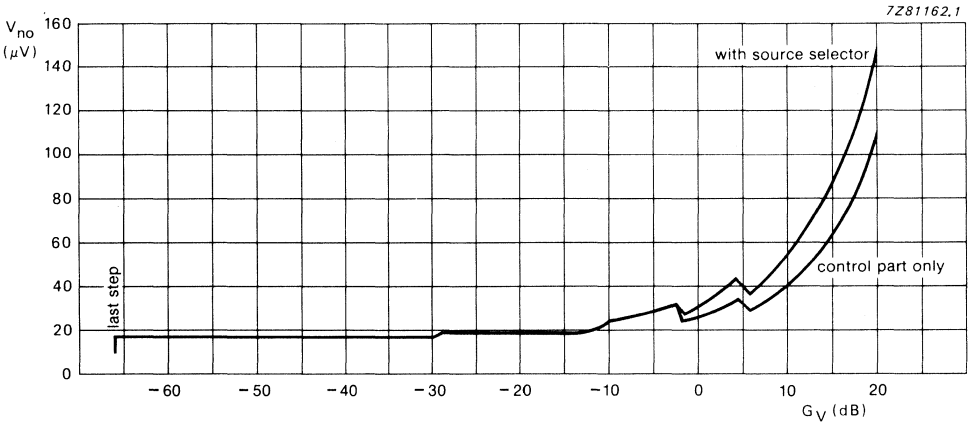


Fig. 7 Output noise voltage (CCIR 468-2 weighted: quasi peak).

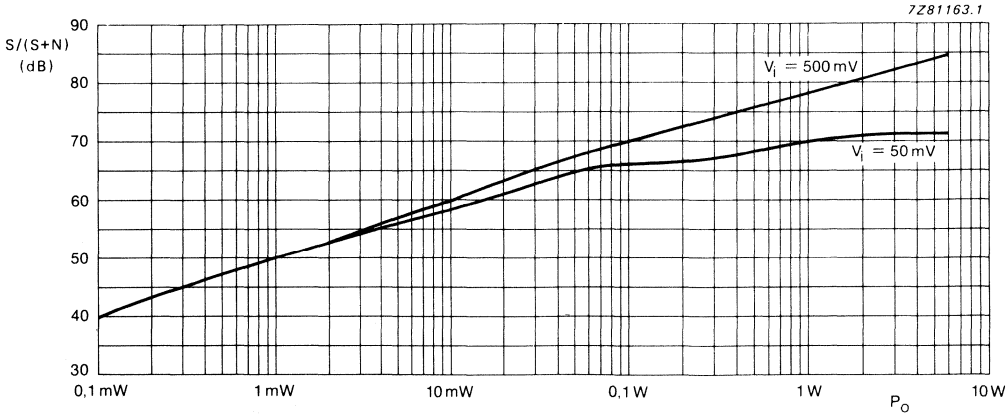


Fig. 8 Signal-to-noise ratio (CCIT 468-2 weighted; quasi peak) with a 6 W power amplifier (gain 20 dB) without noise contribution of the power amplifier (see Fig. 9).

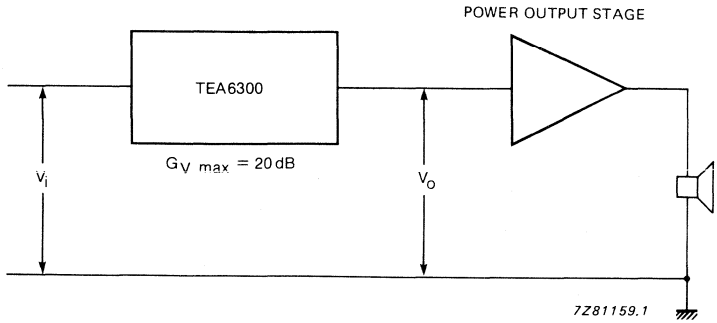


Fig. 9 Recommended level diagram. $V_{i\ min}$ = 50 mV; V_o = 500 mV for P_{max}.

DEVELOPMENT DATA

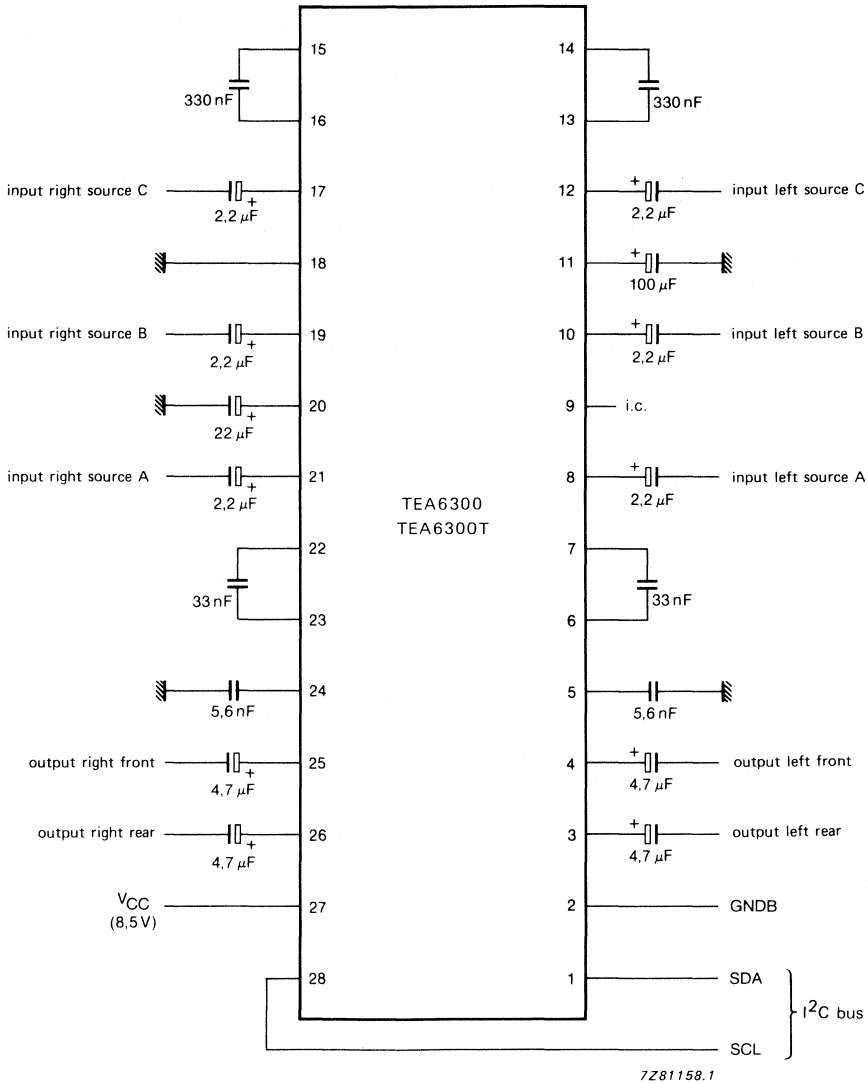


Fig. 10 Test and application circuit.

SOUND FADER CONTROL CIRCUIT

GENERAL DESCRIPTION

The Sound Fader Control circuit (SOFAC) is an I²C bus controlled tone and volume control circuit for car radios. It contains the following functions:

- Inputs and outputs for noise reduction circuits
- Volume and balance control
  Control range of 86 dB in 2 dB steps
- Bass and treble control
  from +15 dB (treble 12 dB) to −12 dB in 3 dB steps
- Fader control from 0 dB to −30 dB in 2 dB steps
- Fast muting
- Low noise suitable for Dolby* B and C NR (noise reduction)
- Signal handling suitable for compact disc
- Pop-free on/off switching
- I²C bus control for all functions

QUICK REFERENCE DATA

parameter	symbol	min.	typ.	max.	unit
Supply voltage	V_{CC}	7,0	8,5	13,2	V
Input sensitivity for full power at the output stage	$V_{i(rms)}$	–	50	–	mV
Input signal handling	$V_{i(rms)}$	–	1,65	–	V
Frequency response	f_r	35	–	20 000	Hz
Channel separation f = 250 Hz to 10 kHz	α_{CS}	45	70	–	dB
Total harmonic distortion	THD	–	0,05	–	%
Signal-to-noise ratio	(S+N)/N	–	80	–	dB
Operating ambient temperature range	T_{amb}	−40	–	+85	°C

PACKAGE OUTLINE

28-lead mini-pack; plastic (SO-28; SOT-136A)

* Available only to licensees of Dolby Laboratories Licensing Corporation, San Francisco, CA94111, U.S.A., from whom licensing and application information must be obtained.
Dolby is a registered trademark of Dolby Laboratories Licensing Corporation.

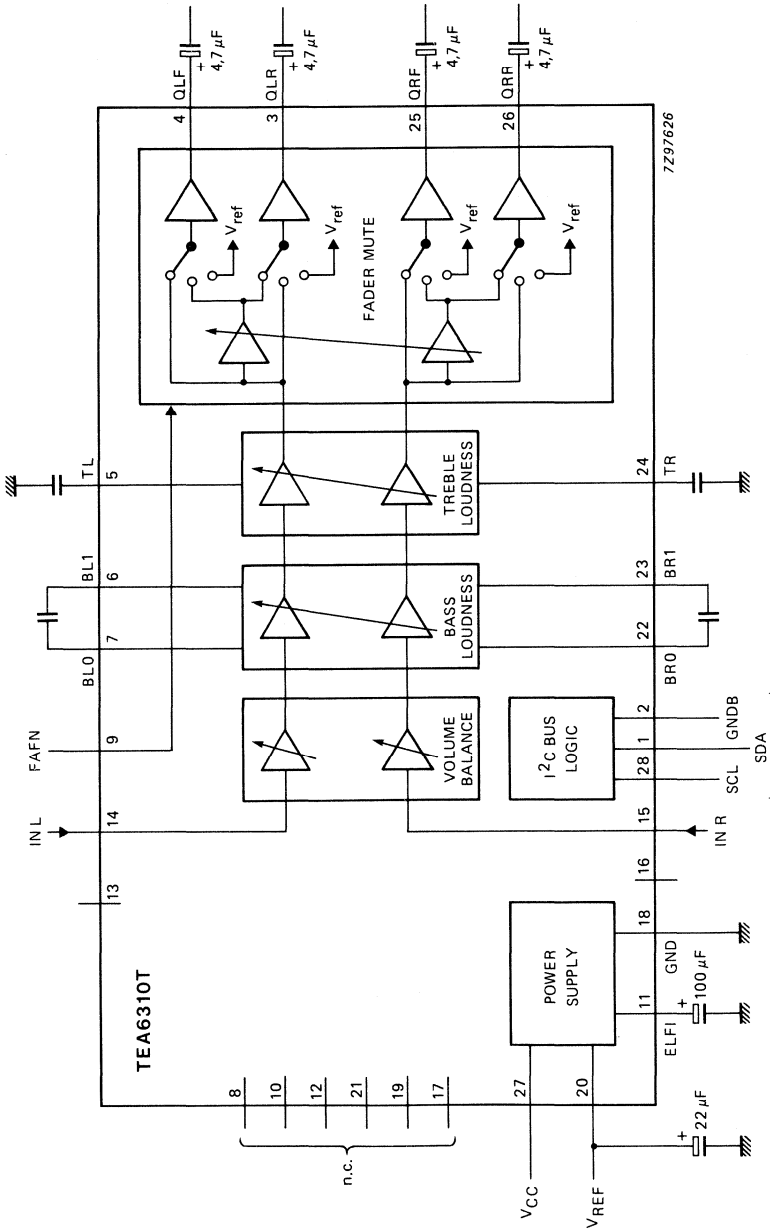


Fig. 1 Block diagram.

FUNCTIONAL DESCRIPTION

The a.c. signal setting is performed by resistor chains in combination with multi-input operational amplifiers. The advantage of this principle is the combination of low noise, low distortion and a high dynamic range for the circuit.
The separated Volume Controls of the left and the right channel make the Balance Control possible. By this the range and the characteristic of the Balance is software programmable. By setting an extra Bass (and optional Treble) Control depending on the actual volume position, the loudness function is performed by software in a microcomputer controlling both the switching points and the ranges.
Because the TEA6310T has four outputs a low level Fader is included. The Fader Control is independent of the Volume Control and an extra Mute position for the front or the rear or for all channels is built in. The last function may be used for muting during preset selection. The Fader function can be disabled by an input signal at FAFN (pin 9).
For pop-free switching, on and off, an extra pop suppression circuitry is built in. As all switching and control functions are controllable via the two wire I^2C bus, no external interface between the microcomputer and the TEA6310 is required.
The on-chip power on reset sets the device into the general Mute mode.

DEFINITION OF THE PINS

1.	SDA	Data input/output
2.	GNDB	Ground for BUS terminals
3.	QLR	Output left rear
4.	QLF	Output left front
5.	TL	Termination for treble control capacitor left channel
6.	BL1	Termination for bass control capacitor left channel
7.	BL0	Termination for bass control capacitor left channel
8.	n.c.	
9.	FAFN	Fader off not control input
10.	n.c.	
11.	ELFI	Electronic filtering for supply
12.	n.c.	
13.	n.c.	
14.	INL	Input left control part
15.	INR	Input right control part
16.	n.c.	
17.	n.c.	
18.	GND	Ground
19.	n.c.	
20.	VREF	Reference voltage (½ V_{CC})
21.	n.c.	
22.	BR0	Termination for bass control capacitor right channel
23.	BR1	Termination for bass control capacitor right channel
24.	TR	Termination for treble control capacitor right channel
25.	QRF	Output right front
26,	QRR	Output right rear
27.	VCC	Supply voltage
28.	SCL	Clock input

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	typ.	max.	unit
Supply voltage (pin 27-18)	V_{CC}	–	–	16	V
Maximum power dissipation	P_{tot}	–	–	2	W
Storage temperature	T_{stg}	–55	–	+ 150	°C
Operating ambient temperature	T_{amb}	–40	–	+ 85	°C

CHARACTERISTICS

V_{CC} = 8,5 V; R_S = 600 Ω; R_L = 10 kΩ; f = 1 kHz; T_{amb} = 25 °C (Fig. 7) unless otherwise specified.

parameter	symbol	min.	typ.	max.	unit
Supply voltage	V_{CC}	7,0	8,5	13,2	V
Supply current	I_{CC}	–	26	–	mA
Internal reference voltage (pin 20) V_{REF} = 0,5 V_{CC}	V_{REF}	–	4,25	–	V
Maximum gain bass and treble linear, fader off	G_v	–	20	–	dB
Output level					
for P_{max} at the output stage	$V_{o(rms)}$	–	500	–	mV
for start of clipping	$V_{o(rms)}$	–	1000	–	mV
Input sensitivity at V_o = 500 mV	$V_{i(rms)}$	–	50	–	mV
Frequency response bass and treble linear; roll-off frequency –1 dB	f_r	35	–	20 000	Hz
Channel separation G = 0 dB; bass and treble linear; frequency range 250 Hz to 10 kHz	α_{CS}	45	70	–	dB
Total harmonic distortion frequency range 20 Hz to 12,5 kHz					
V_{in} = 50 mV; G = 20 dB	THD	–	0,1	0,3	%
V_{in} = 500 mV; G = 0 dB	THD	–	0,05	0,2	%
V_{in} = 1,6 V; G = –10 dB	THD	–	0,2	0,5	%
Ripple rejection $V_{r(rms)} < 200$ mV; G = 0 dB; bass and treble linear;					
at f = 100 Hz	RR_{100}	–	70	–	dB
at f = 40 Hz to 12,5 kHz	RR_{range}	–	tbf	–	dB

DEVELOPMENT DATA

parameter	symbol	min.	typ.	max.	unit
Signal-to-noise ratio					
bass and treble linear; notes 1 + 2					
CCIR 468-2 weighted; quasi peak					
V_i = 50 mV; V_o = 46 mV; P_O = 50 mW	S/N	–	65	–	dB
V_i = 500 mV; V_o = 45 mV; P_O = 50 mW	S/N	–	67	–	dB
V_i = 50 mV; V_o = 200 mV; P_O = 1 W	S/N	tbf	72	–	dB
V_i = 500 mV; V_o = 200 mV; P_O = 1 W	S/N	tbf	78	–	dB
V_i = 50 mV; V_o = 500 mV; P_O = 6 W	S/N	–	72	–	dB
V_i = 500 mV; V_o = 500 mV; P_O = 6 W	S/N	–	86	–	dB
Noise power					
mute position, only contribution of					
TEA6310T, power amplifier for 25 W	P_N	–	–	10	nW
Crosstalk (20 log $V_{bus(p-p)}/V_{o(rms)}$					
between BUS inputs and signal outputs					
G = 0 dB; bass and treble linear	α_B	–	110	–	dB
CONTROL PART					
Input impedance	Z_I	35	50	65	kΩ
Output impedance	Z_O	–	100	150	Ω
Admissible output load resistance	R_L	10	–	–	kΩ
Admissible output load capacitance	C_L	0	–	1000	pF
Maximum input voltage					
THD < 0,5%; G = −10 dB;					
bass and treble linear	$V_{i(rms)}$	–	2,0	–	V
Noise voltage					
weighted acc CCIR 468-2, quasi peak,					
bass and treble linear, fader off					
gain 20 dB	N_W	–	110	220	μV
gain 0 dB	N_W	–	25	50	μV
gain −66 dB	N_W	–	19	38	μV
mute position	N_W	–	11	22	μV
VOLUME CONTROL					
Continuous control range	G_c	–	86	–	dB
Step resolution	–	–	2	–	dB
Attenuator set error					
(G = +20 to −50 dB)	ΔG_a	–	–	2	dB
Attenuator set error					
(G = +20 to −66 dB)	ΔG_a	–	–	3	dB
Gain tracking error					
balance in mid position, bass					
and treble linear	ΔG_t	–	–	2	dB
Mute attenuation	α_M	–	80	–	dB
BASS CONTROL					
Bass control range					
f = 40 Hz; maximum boost	G_b	14	15	16	dB
f = 40 Hz; maximum attenuation	$-G_b$	11	12	13	dB
Step resolution	–	–	3	–	dB
Step error	–	–	–	0,5	dB

parameter	symbol	min.	typ.	max.	unit
TREBLE CONTROL					
Treble control range					
f = 15 kHz; maximum boost	G_t	11	12	13	dB
f = 15 kHz; maximum attenuation	$-G_t$	11	12	13	dB
f > 15 kHz; maximum boost	G_t	–	–	15	dB
Step resolution		–	3	–	dB
Step error		–	–	0,5	dB
FADER CONTROL					
Continuous attenuation fader control range	G_f	–	30	–	dB
Step resolution	–	–	2	–	dB
Attenuator set error	–	–	–	1,5	dB
Mute attenuation	α_M	–	80	–	dB
FADER OFF NOT CONTROL					
Fader enabled input HIGH	$V_{9\text{-}18}$	3	–	12	V
Fader disabled input LOW	$V_{9\text{-}18}$	–0,3	–	1,5	V
Input current					
HIGH	I_9	–10	–	+10	μA
LOW	I_9	–10	–	+10	μA
DIGITAL PART					
Bus terminals					
Input voltage					
HIGH	V_{IH}	3	–	12	V
LOW	V_{IL}	–0,3	–	1,5	V
Input current					
HIGH	I_{IH}	–10	–	+10	μA
LOW	I_{IL}	–10	–	+10	μA
Output voltage LOW					
I_L = 3 mA	V_{OL}	–	–	0,4	V
A.C. CHARACTERISTICS					
according to the I^2C Bus specification					
Power-on Reset					
When RESET is active the GMU (general mute) bit is set and the BUS receiver is in RESET position					
Increasing supply voltage					
start of reset	V_{CC}	–	–	2,5	V
end of reset	V_{CC}	5,2	6,0	6,8	V
Decreasing supply voltage					
start of reset	V_{CC}	4,2	5,0	5,8	V

Notes to the characteristics

1. The indicated values for output power assume a 6 Watt power amp. with 20 dB gain, connected to the output of the circuit. Signal to noise ratios exclude noise contribution of the power amplifier.
2. Signal to noise ratios on a CCIR 468-2 average reading-meter are 4,5 dB better than on CCIR 468-2 quasi peak.

I^2C BUS FORMAT

S	SLAVE ADDRESS	A	SUB-ADDRESS	A	DATA	A	P

S = start condition
SLAVE ADDRESS = 1000 0000
A = acknowledge, generated by the slave
SUB-ADDRESS = see table 1
DATA = see table 1
P = STOP condition

If more than 1 byte DATA are transmitted, then auto-increment of the sub-address is performed.

Table 1

function	sub-address	DATA							
		D7	D6	D5	D4	D3	D2	D1	D0
volume left	0 0 0 0 0 0 0 0	X	X	VL5	VL4	VL3	VL2	VL1	VL0
volume right	0 0 0 0 0 0 0 1	X	X	VR5	VR4	VR3	VR2	VR1	VR0
bass	0 0 0 0 0 0 1 0	X	X	X	X	BA3	BA2	BA1	BA0
treble	0 0 0 0 0 0 1 1	X	X	X	X	TR3	TR2	TR1	TR0
fader	0 0 0 0 0 1 0 0	X	X	MFN	FCH	FA3	FA2	FA1	FA0
switch	0 0 0 0 0 1 0 1	GMU	X	X	X	X	X	X	X

Function of the bits:

VL0 to VL5	volume control left
VR0 to VR5	volume control right
BA0 to BA3	bass control
TR0 to TR3	treble control
FA0 to FA3	fader control
FCH	select fader channel (front or rear)
MFN	mute control of the selected fader channel
SCA to SCC	source selector control
GMU	general mute control for the outputs QLF, QLR, QRF and QRR
X	do not care bits (1 during testing)

DEVELOPMENT DATA

Table 2

Bass setting

G dB	DATA			
	BA3	BA2	BA1	BA0
+ 15	1	1	1	1
+ 15	1	1	1	0
+ 15	1	1	0	1
+ 15	1	1	0	0
+ 12	1	0	1	1
+ 9	1	0	1	0
+ 6	1	0	0	1
+ 3	1	0	0	0
0	0	1	1	1
− 3	0	1	1	0
− 6	0	1	0	1
− 9	0	1	0	0
−12	0	0	1	1
−12	0	0	1	0
−12	0	0	0	1
−12	0	0	0	0

Table 3

treble setting

G dB	DATA			
	TR3	TR2	TR1	TR0
+ 12	1	1	1	1
+ 12	1	1	1	0
+ 12	1	1	0	1
+ 12	1	1	0	0
+ 12	1	0	1	1
+ 9	1	0	1	0
+ 6	1	0	0	1
+ 3	1	0	0	0
0	0	1	1	1
− 3	0	1	1	0
− 6	0	1	0	1
− 9	0	1	0	0
−12	0	0	1	1
−12	0	0	1	0
−12	0	0	0	1
−12	0	0	0	0

DEVELOPMENT DATA

Table 4 Volume setting LEFT

G dB	DATA					
	VL5	VL4	VL3	VL2	VL1	VL0
20	1	1	1	1	1	1
18	1	1	1	1	1	0
16	1	1	1	1	0	1
14	1	1	1	1	0	0
12	1	1	1	0	1	1
10	1	1	1	0	1	0
8	1	1	1	0	0	1
6	1	1	1	0	0	0
4	1	1	0	1	1	1
2	1	1	0	1	1	0
0	1	1	0	1	0	1
− 2	1	1	0	1	0	0
− 4	1	1	0	0	1	1
− 6	1	1	0	0	1	0
− 8	1	1	0	0	0	1
−10	1	1	0	0	0	0
−12	1	0	1	1	1	1
−14	1	0	1	1	1	0
−16	1	0	1	1	0	1
−18	1	0	1	1	0	0
−20	1	0	1	0	1	1
−22	1	0	1	0	1	0
−24	1	0	1	0	0	1
−26	1	0	1	0	0	0
−28	1	0	0	1	1	1
−30	1	0	0	1	1	0
−32	1	0	0	1	0	1
−34	1	0	0	1	0	0
−36	1	0	0	0	1	1
−38	1	0	0	0	1	0
−40	1	0	0	0	0	1
−42	1	0	0	0	0	0
−44	0	1	1	1	1	1
−46	0	1	1	1	1	0
−48	0	1	1	1	0	1
−50	0	1	1	1	0	0
−52	0	1	1	0	1	1
−54	0	1	1	0	1	0
−56	0	1	1	0	0	1
−58	0	1	1	0	0	0
−60	0	1	0	1	1	1
−62	0	1	0	1	1	0
−64	0	1	0	1	0	1
−66	0	1	0	1	0	0
mute left	0	1	0	0	1	1
mute left	0	1	0	0	1	0
.				.		
.				.		
.				.		
mute left	0	0	0	0	0	0

Table 5 Volume setting RIGHT

G dB	DATA					
	VR5	VR4	VR3	VR2	VR1	VR0
20	1	1	1	1	1	1
18	1	1	1	1	1	0
16	1	1	1	1	0	1
14	1	1	1	1	0	0
12	1	1	1	0	1	1
10	1	1	1	0	1	0
8	1	1	1	0	0	1
6	1	1	1	0	0	0
4	1	1	0	1	1	1
2	1	1	0	1	1	0
0	1	1	0	1	0	1
− 2	1	1	0	1	0	0
− 4	1	1	0	0	1	1
− 6	1	1	0	0	1	0
− 8	1	1	0	0	0	1
−10	1	1	0	0	0	0
−12	1	0	1	1	1	1
−14	1	0	1	1	1	0
−16	1	0	1	1	0	1
−18	1	0	1	1	0	0
−20	1	0	1	0	1	1
−22	1	0	1	0	1	0
−24	1	0	1	0	0	1
−26	1	0	1	0	0	0
−28	1	0	0	1	1	1
−30	1	0	0	1	1	0
−32	1	0	0	1	0	1
−34	1	0	0	1	0	0
−36	1	0	0	0	1	1
−38	1	0	0	0	1	0
−40	1	0	0	0	0	1
−42	1	0	0	0	0	0
−44	0	1	1	1	1	1
−46	0	1	1	1	1	0
−48	0	1	1	1	0	1
−50	0	1	1	1	0	0
−52	0	1	1	0	1	1
−54	0	1	1	0	1	0
−56	0	1	1	0	0	1
−58	0	1	1	0	0	0
−60	0	1	0	1	1	1
−62	0	1	0	1	1	0
−64	0	1	0	1	0	1
−66	0	1	0	1	0	0
mute right	0	1	0	0	1	1
mute right	0	1	0	0	1	0
.				.		
.				.		
.				.		
mute right	0	0	0	0	0	0

Table 6 Fader function

setting		DATA					
front rear							
dB	dB	MFN	FCH	FA3	FA2	FA1	FA0
				fader off			
0	0	1	1	1	1	1	1
0	0	0	1	1	1	1	1
				fader front			
− 2	0	1	1	1	1	1	0
− 4	0	1	1	1	1	0	1
− 6	0	1	1	1	1	0	0
− 8	0	1	1	1	0	1	1
−10	0	1	1	1	0	1	0
−12	0	1	1	1	0	0	1
−14	0	1	1	1	0	0	0
−16	0	1	1	0	1	1	1
−18	0	1	1	0	1	1	0
−20	0	1	1	0	1	0	1
−22	0	1	1	0	1	0	0
−24	0	1	1	0	0	1	1
−26	0	1	1	0	0	1	0
−28	0	1	1	0	0	0	1
−30	0	1	1	0	0	0	0
				mute front			
−80	0	0	1	1	1	1	0
.	.			.			
.	.			.			
.	.			.			
−80	0	0	1	0	0	0	0

setting		DATA					
front rear							
dB	dB	MFN	FCH	FA3	FA2	FA1	FA0
				fader off			
0	0	1	0	1	1	1	1
0	0	0	0	1	1	1	1
				fader rear			
0	− 2	1	0	1	1	1	0
0	− 4	1	0	1	1	0	1
0	− 6	1	0	1	1	0	0
0	− 8	1	0	1	0	1	1
0	−10	1	0	1	0	1	0
0	−12	1	0	1	0	0	1
0	−14	1	0	1	0	0	0
0	−16	1	0	0	1	1	1
0	−18	1	0	0	1	1	0
0	−20	1	0	0	1	0	1
0	−22	1	0	0	1	0	0
0	−24	1	0	0	0	1	1
0	−26	1	0	0	0	1	0
0	−28	1	0	0	0	0	1
0	−30	1	0	0	0	0	0
				mute rear			
0	−80	0	0	1	1	1	0
.	.			.			
.	.			.			
.	.			.			
0	−80	0	0	0	0	0	0

Table 7

MUTE control	DATA GMU	remarks
active	1	outputs QLF, QLR QRF and QRR are muted
passive	0	no general mute

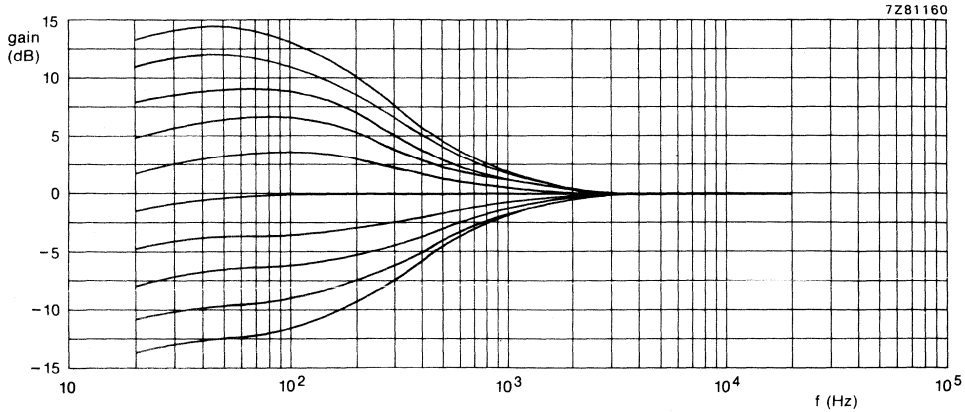


Fig. 2 Bass control.

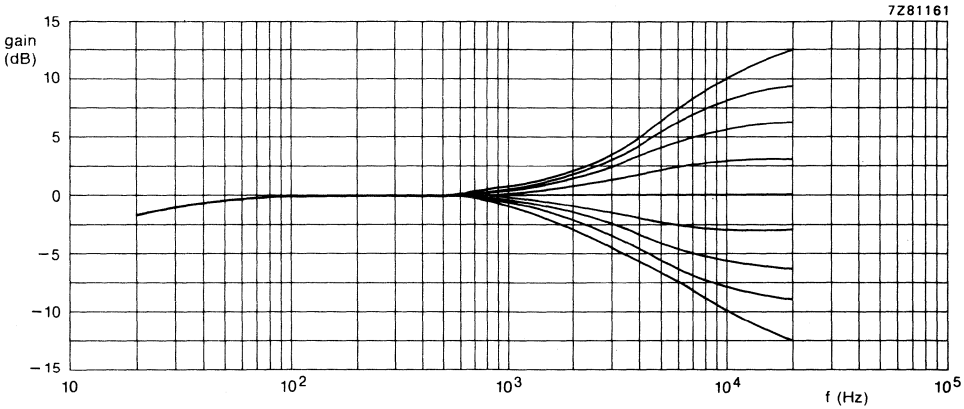


Fig. 3 Treble control.

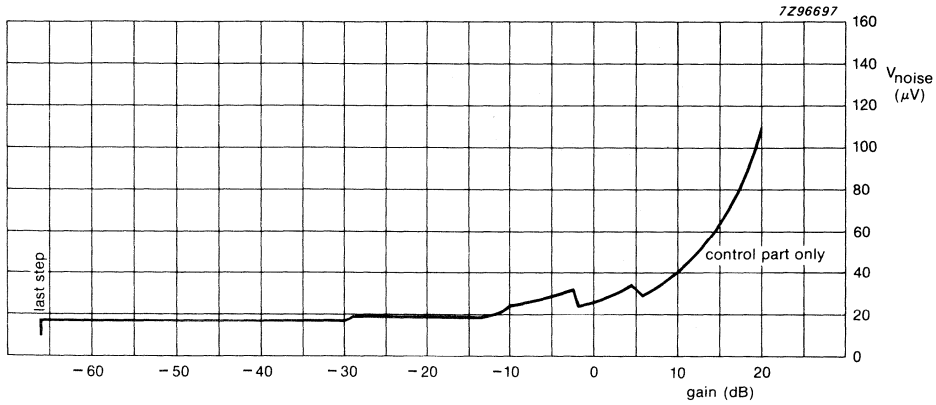


Fig. 4 Output noise voltage (CCIR 468-2 weighted; quasi peak).

DEVELOPMENT DATA

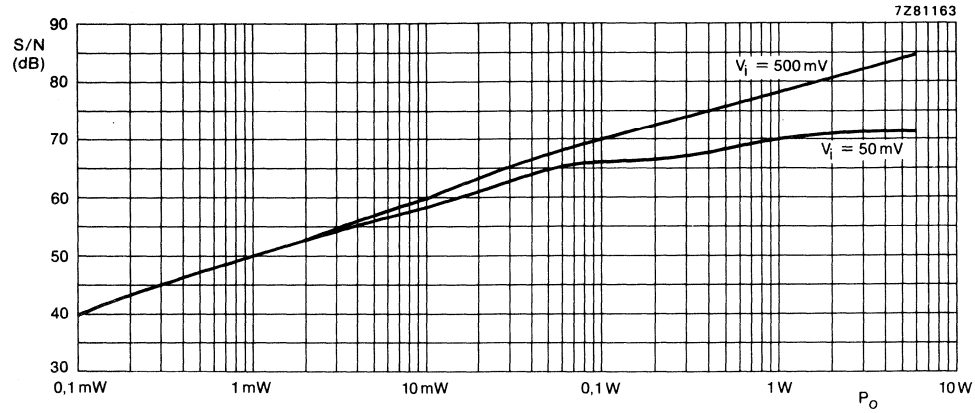


Fig. 5 Signal to noise ratio (CCIR 468-2 weighted; quasi peak) with a 6 W power amplifier (gain 20 dB) without noise contribution of the power amplifier (See Fig. 6).

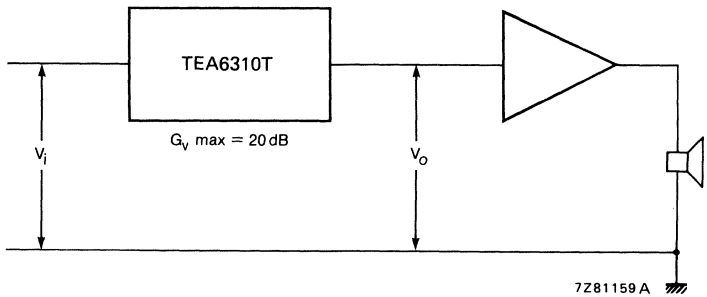


Fig. 6 Recommended level diagram. $V_{i\ min}$ = 50 mV; V_o = 500 mV for P_{max}.

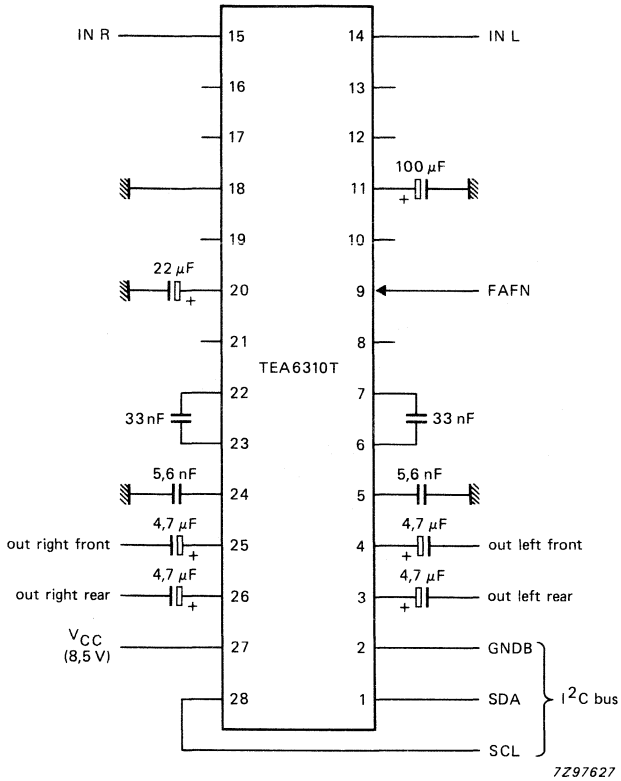


Fig. 7 Test and application circuit.

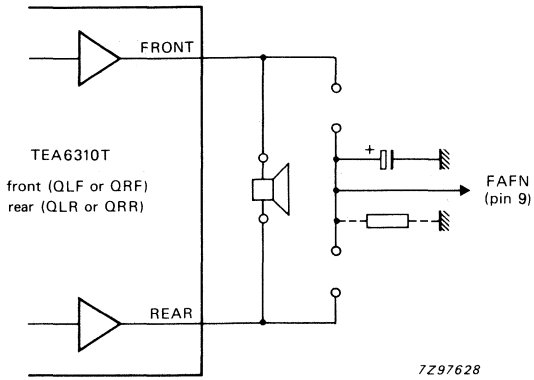


Fig. 8a Automatic FADER control.
P_O = 24 W; $V_{9\text{-}18}$ = 0 V (FADER disabled)

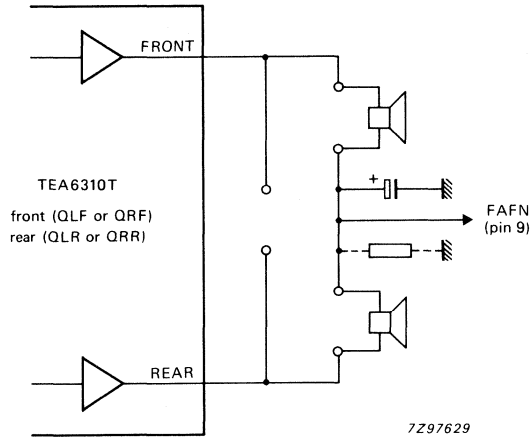


Fig. 8b Automatic FADER control.
P_O = 2 x 6 W; $V_{9\text{-}18}$ = 7 V (FADER enabled)

RADIO TUNING PLL FREQUENCY SYNTHESIZER

GENERAL DESCRIPTION

The TSA6057 is a bipolar single chip frequency synthesizer manufactured in SUBILO-N technology (components vertically separated by oxide). It performs all the tuning functions of a PLL radio tuning system. The IC is designed for application in all types of radio receivers.

Features

- On-chip AM and FM prescalers with high input sensitivity
- On-chip high performance one input (two output) tuning voltage amplifier for the AM and FM loop filters
- On-chip 2-level current amplifier (charge pump) to adjust the loop gain
- Only one reference frequency (4 MHz) for both AM and FM
- High speed tuning due to a powerful digital memory phase detector
- 40 kHz output reference frequency for co-operation with the FM/IF system and microcomputer-based tuning interface IC (TEA6100)
- Oscillator frequency ranges of: 512 kHz to 30 MHz and 30 MHz to 150 MHz
- Three selectable reference frequencies of 1 kHz, 10 kHz or 25 kHz for both tuning ranges
- Serial 2-wire I^2C bus interface to a microcomputer and one programmable address input
- Software controlled bandswitch output

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage						
pin 3		$V_{CC1} = V_{3-4}$	4,5	5,0	5,5	V
pin 16		$V_{CC2} = V_{16-4}$	V_{CC1}	8,5	12	V
Supply current	no outputs loaded					
pin 3		I_3	12	20	28	mA
pin 16		I_{16}	0,2	0,5	1,0	mA
Max. input frequency on AM		f_{iAM}	30	–	–	MHz
Min. input frequency on AM		f_{iAM}	–	–	0,512	MHz
Max. input frequency on FM		f_{iFM}	150	–	–	MHz
Min. input frequency on FM		f_{iFM}	–	–	30	MHz
Input voltage on AM (r.m.s. value)	$V_{iFM} = 0$ V	$V_{iAM(rms)}$	30	–	500	mV
Input voltage on FM (r.m.s. value)	$V_{iAM} = 0$ V	$V_{iFM(rms)}$	20	–	300	mV
Total power dissipation		P_{tot}	–	0,14	–	W
Operating ambient temperature range		T_{amb}	–30	–	+ 85	°C

PACKAGE OUTLINE

16-lead DIL; plastic (SOT-38).

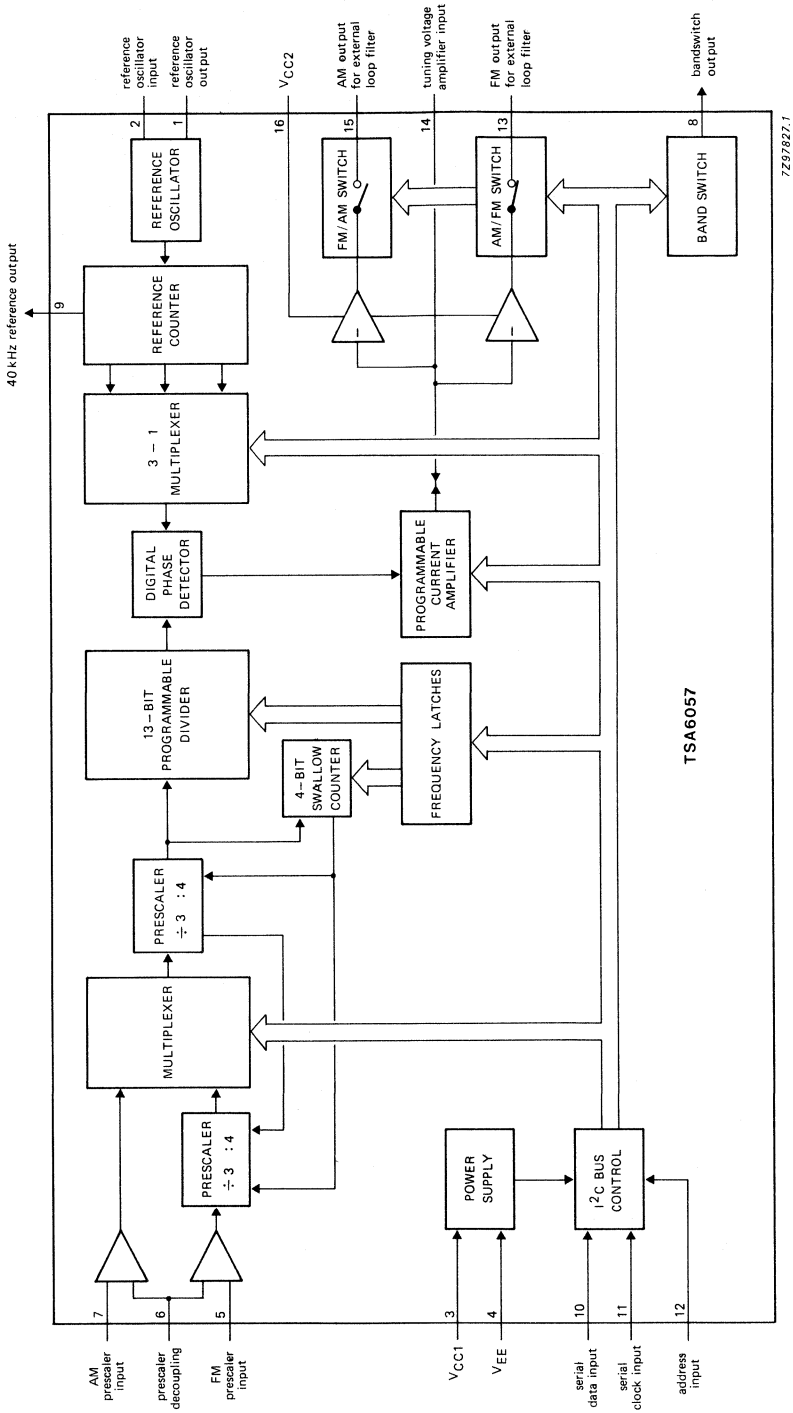


Fig. 1 Block diagram.

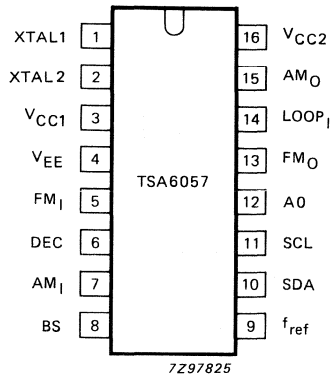


Fig. 2 Pinning diagram.

PINNING

1	XTAL1	reference oscillator output
2	XTAL2	reference oscillator input
3	V_{CC1}	positive supply voltage
4	V_{EE}	ground
5	FM_I	FM prescaler input
6	DEC	prescaler decoupling
7	AM_I	AM prescaler input
8	BS	bandswitch output
9	f_{ref}	40 kHz reference output
10	SDA	serial data input (I^2C bus)
11	SCL	serial clock input (I^2C bus)
12	A0	address input (I^2C bus)
13	FM_O	FM output for external loop filter
14	$LOOP_I$	tuning voltage amplifier input
15	AM_O	AM output for external loop filter
16	V_{CC2}	positive supply voltage

DEVELOPMENT DATA

FUNCTIONAL DESCRIPTION

The TSA6057 contains the following parts and facilities:

- Separate input amplifiers for the AM and FM VCO-signals.
- A prescaler with the divisors 3:4 on AM and 15:16 on FM, a multiplexer to select AM or FM and a 4-bit programmable swallow counter.
- A 13-bit programmable counter.
- A digital memory phase detector.
- A reference frequency channel comprised of a 4 MHz crystal oscillator followed by a reference counter. The reference frequency can be 1 kHz, 10 kHz or 25 kHz and is applied to the digital memory phase detector. The reference counter also outputs a 40 kHz reference frequency to pin 9 for co-operation with the FM/IF system and microcomputer-based tuning interface IC (TEA6100).
- A programmable current amplifier (charge pump) which consists of a 5 μA and a 450 μA current source. This allows adjustment of loop gain, thus providing high current-high speed tuning and low current-stable tuning.
- A one input – two output tuning voltage amplifier. One output is connected to the external AM loop filter and the other output to the external FM loop filter. The AM output is switched to a high impedance state by the FM/AM switch in the FM position and the FM output is switched to a high impedance state by the AM/FM switch in the AM position. The outputs can deliver a tuning voltage of up to 10,5 V.
- An I^2C bus interface with data latches and control logic. The I^2C bus is intended for communication between microcontrollers and different ICs or modules. Detailed information on the I^2C bus specification is available on request.
- A software-controlled bandswitch output.

FUNCTIONAL DESCRIPTION (continued)

Controls

The TSA6057 is controlled via the 2-wire I^2C bus. For programming there is one module address, a logic 0 R/W bit, a subaddress byte and four data bytes. The subaddress determines which one of the four data bytes is transmitted first. The module address contains a programmable address bit (D1) which with address input A0 (pin 12) makes it possible to operate two TSA6057s in one system.

The auto increment facility of the I^2C bus allows programming of the TSA6057 within one transmission (address + subaddress + 4 data bytes).

- The TSA6057 can also be partially programmed. Transmission must then be ended by a stop condition.

The bit organization of the 4 data bytes is shown in Fig. 3 and are described in sections (a) to (f).

(a) The bits S0 to S16 together with bit FM/$\overline{\text{AM}}$ are used to set the divisor of the input frequency at inputs AM_I (pin 7) or FM_I (pin 5). If the system in-lock the following is valid:

FM/$\overline{\text{AM}}$	input frequency (f_i)	input
0	$(S0 \times 2^0 + S1 \times 2^1 + S13 \times 2^{13} + S14 \times 2^{14}) \times f_{ref}$	AM_I
1	$(S0 \times 2^0 + S1 \times 2^1 + S15 \times 2^{15} + S16 \times 2^{16}) \times f_{ref}$	FM_I

Where

The minimum dividing ratio for AM mode is $2^6 = 64$
The minimum dividing ratio for FM mode is $2^8 = 256$

(b) The bit CP is used to control the charge pump current.

CP	current
0	low
1	high

(c) The bits REF1 and REF2 are used to set the reference frequency applied to the phase detector.

REF1	REF2	frequency (kHz)
0	0	1
0	1	10
1	0	25
1	1	none

(d) The bit $\overline{\text{FM}}$/AM OPAMP controls the switch AM/FM; FM/AM in the tuning voltage amplifier output circuitry.

$\overline{\text{FM}}$/AM OPAMP	switch FM/AM	switch AM/FM
1	closed	open
0	open	closed

(e) The bit BS controls the open collector bandswitch output.

BS	bandswitch output
1	sink current
0	floating

(f) The data byte DB3 must be set to 0 . . . . . 0. It is also used for test purposes.

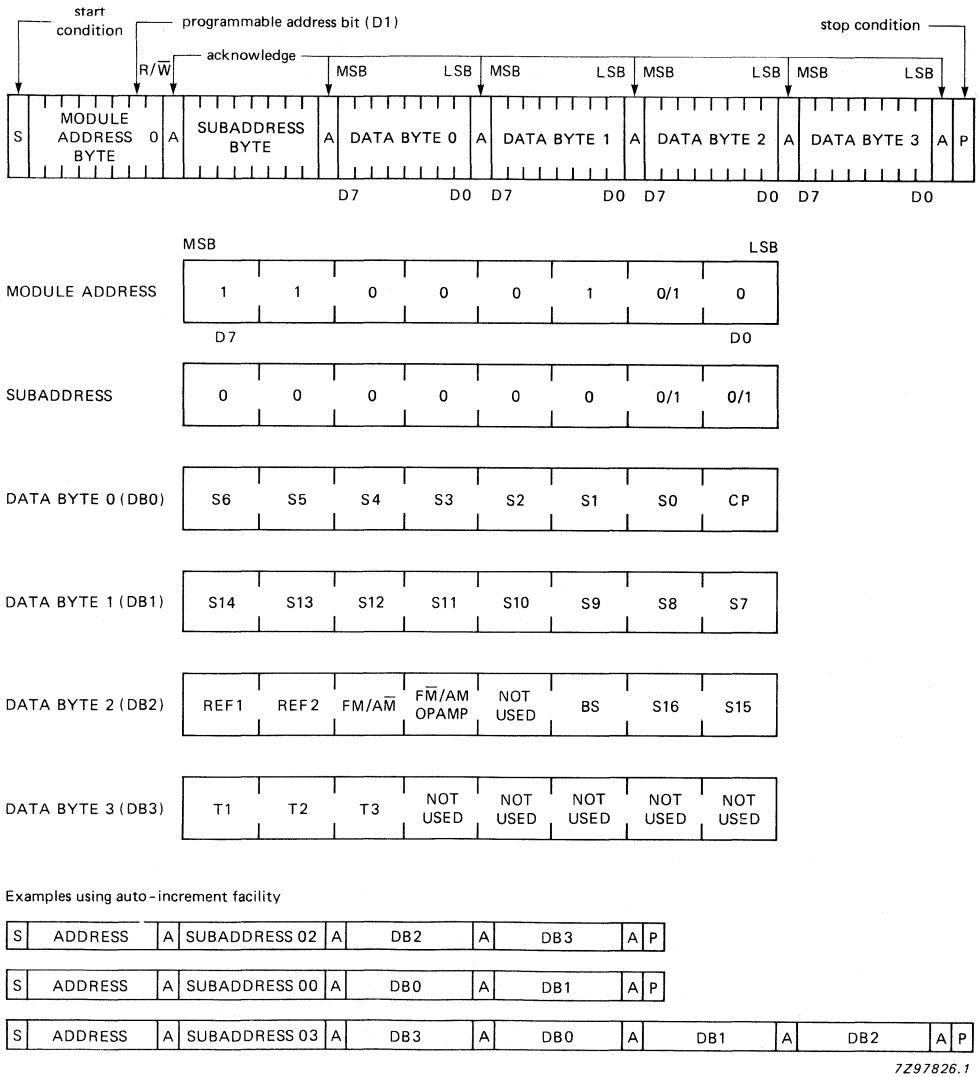


Fig. 3 Bit organization.

DEVELOPMENT DATA

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage (pin 3)	$V_{CC1} = V_{3-4}$	−0,3	5,5	V
Supply voltage (pin 16)	$V_{CC2} = V_{16-4}$	V_{CC1}	12,5	V
Total power dissipation	P_{tot}	−	0,85	W
Operating ambient temperature	T_{amb}	−30	+ 85	°C
Storage temperature range	T_{stg}	−65	+ 150	°C

CHARACTERISTICS

V_{CC1} = 5 V; V_{CC2} = 8,5 V; T_{amb} = 25 °C; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage (pin 3)		V_{CC1}	4,5	5,0	5,5	V
Supply voltage (pin 16)		V_{CC2}	V_{CC1}	8,5	12	V
Supply current	no outputs loaded					
pin 3		I_{CC1}	12	20	28	mA
pin 16		I_{CC2}	0,2	0,5	1,0	mA
I²C bus inputs (SDA; SCL; AO)						
Input voltage HIGH		V_{IH}	3,0	−	5,0	V
Input voltage LOW		V_{IL}	−0,3	−	1,5	V
Input current HIGH		I_{IH}	−	−	10	μA
Input current LOW		I_{IL}	−	−	10	μA
SDA output	open collector					
Output voltage LOW	I_{OL} = 3,0 mA	V_{OL}	−	−	0,4	V
RF input (AM; FM)						
Max. input frequency on AM		f_{iAM}	30	−	−	MHz
Min. input frequency on AM		f_{iAM}	−	−	0,512	MHz
Max. input frequency on FM		f_{iFM}	150	−	−	MHz
Min. input frequency on FM		f_{iFM}	−	−	30	MHz
Input voltage on AM (r.m.s. value)	V_{iFM} = 0 V measured in Fig. 4	$V_{iAM(rms)}$	30	−	500	mV
Input impedance AM						
resistance		R_{AM}	−	5,9	−	kΩ
capacitance		C_{AM}	−	2	−	pF
Input voltage on FM (r.m.s. value)	V_{iAM} = 0 V measured in Fig. 4	$V_{iFM(rms)}$	20	−	300	mV
Input impedance FM						
resistance		R_{FM}	−	3,6	−	kΩ
capacitance		C_{FM}	−	2	−	pF

parameter	conditions	symbol	min.	typ.	max.	unit
Oscillator (XTAL1; XTAL2)						
Crystal resonance resistance (4 MHz)	see Fig. 5	R_{XTAL}	–	–	150	Ω
Programmable charge pump						
Output current to loop filter						
bit CP = logic 0		I_{chp}	3	5	7	μA
bit CP = logic 1		I_{chp}	400	500	600	μA
Ripple rejection	f_{ripple} = 100 Hz					
20 log $\Delta V_{CC1}/\Delta V_O$		RR	40	50	–	dB
20 log $\Delta V_{CC2}/\Delta V_O$		RR	40	50	–	dB
Bandswitch output (pin 8)						
Output voltage HIGH		V_{OH}	–	–	12	V
Output voltage LOW	I_{OL} = 3 mA	V_{OL}	–	–	0,8	V
Output sink current		I_{sink}	–	–	3	mA
Output leakage current	V_{OH} = 12 V	I_{LO}	–	–	10	μA
Reference frequency output (pin 9)						
Output frequency	4 MHz crystal	f_{ref}	–	40	–	kHz
Output voltage HIGH	I_{source} = 5 μA	V_{OH}	1,2	1,4	1,7	V
Output voltage LOW		V_{OL}	–	0,1	0,2	V
Tuning voltage amplifier outputs						
AM output (pin 15)						
max. output voltage	I_{source} = 0,5 mA	$V_{O(max)}$	V_{CC2} −1,5	–	–	V
min. output voltage	I_{sink} = 1 mA	$V_{O(min)}$	–	–	0,8	V
max. output source current		I_{source}	0,5	–	–	mA
max. output sink current		I_{sink}	1,0	–	–	mA
FM output (pin 13)						
max. output voltage	I_{source} = 0,5 mA	$V_{O(max)}$	V_{CC2} −1,5	–	–	V
min. output voltage	I_{sink} = 1 mA	$V_{O(min)}$	–	–	0,8	V
max. output source current		I_{source}	0,5	–	–	mA
max. output sink current		I_{sink}	1,0	–	–	mA
Impedance of switched off output		$Z_{O(off)}$	5	–	–	MΩ
Input bias current (absolute value)		I_{bias}	–	1	5	nA

DEVELOPMENT DATA

APPLICATION INFORMATION

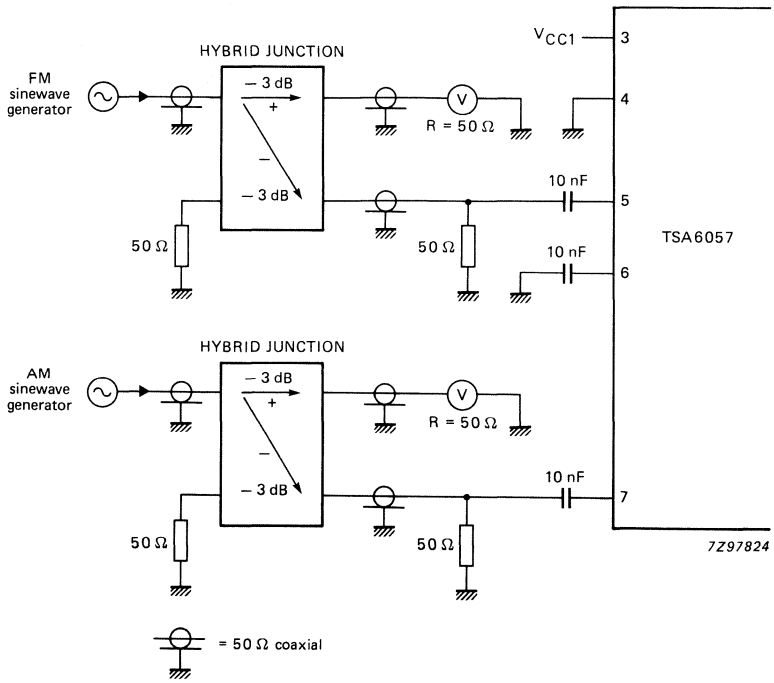


Fig. 4 Prescaler input sensitivity.

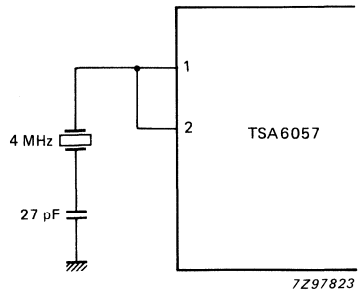


Fig. 5 Crystal connection (4 MHz).

DEVELOPMENT DATA

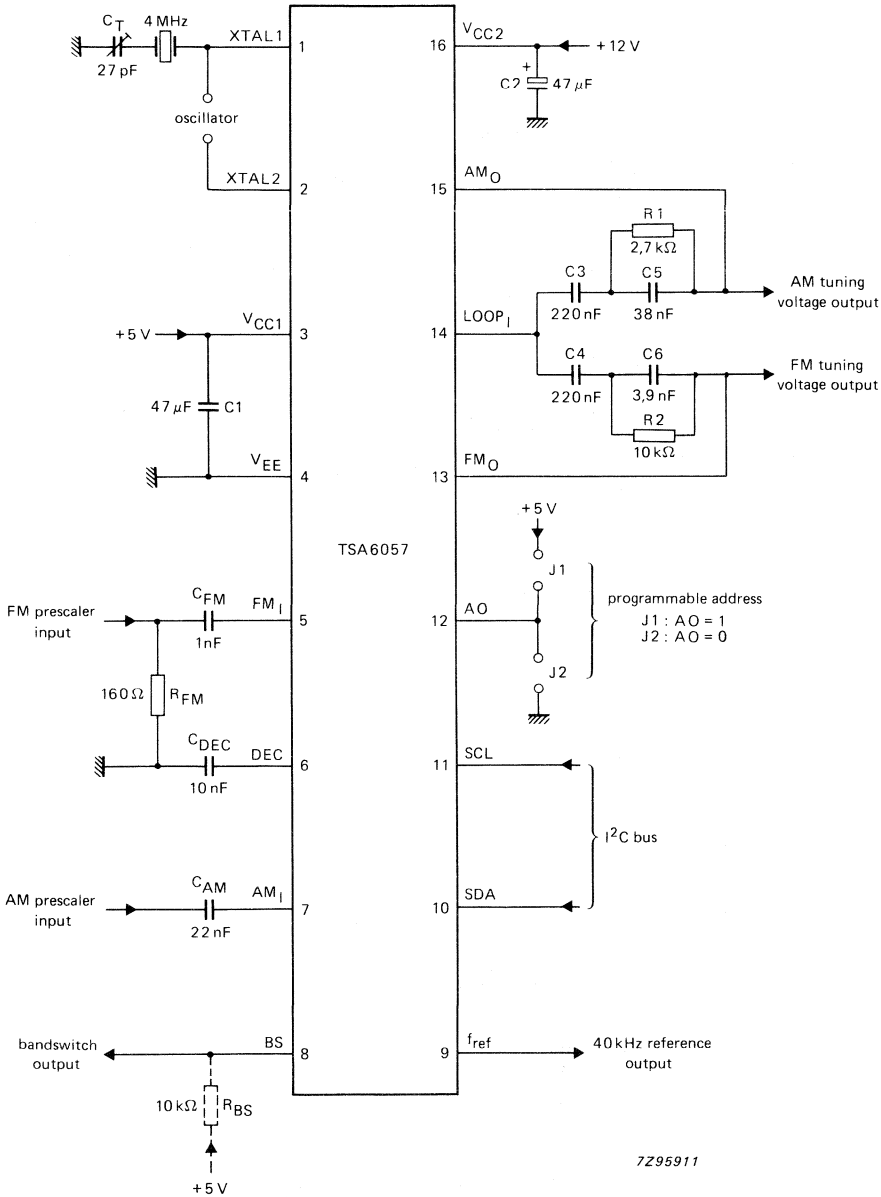


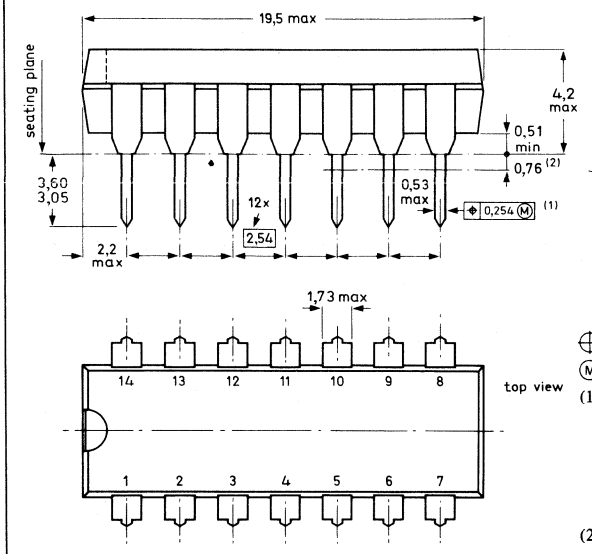
Fig. 6 Application diagram

PACKAGE INFORMATION

Package outlines

Soldering

14-LEAD DUAL IN-LINE; PLASTIC (SOT27)



Dimensions in mm

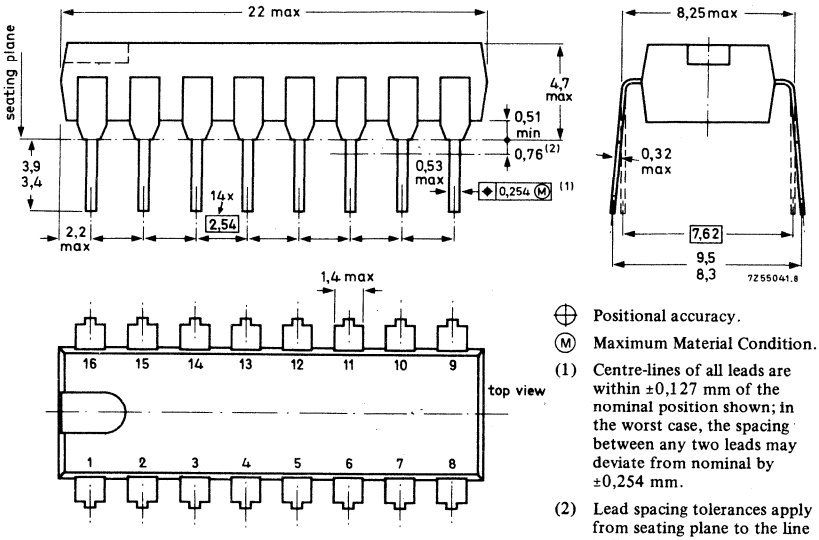
⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

16-LEAD DUAL IN-LINE; PLASTIC (SOT38)



Dimensions in mm

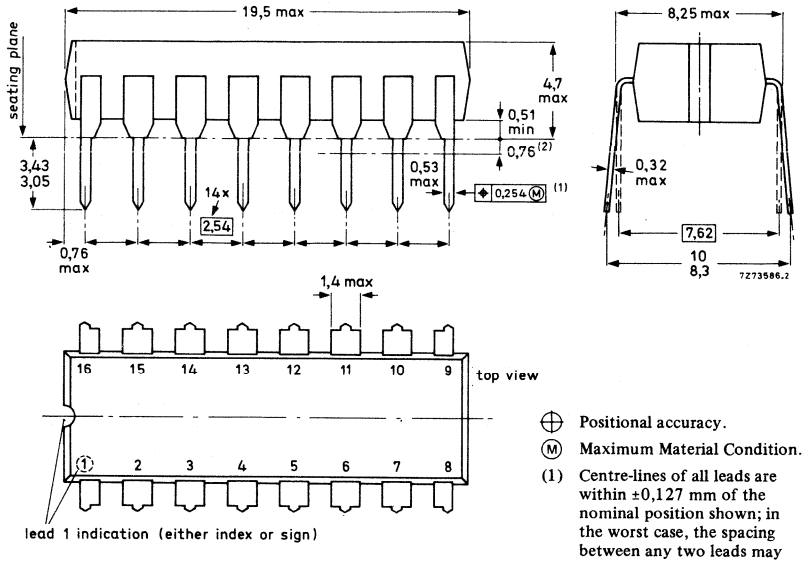
⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

16-LEAD DUAL IN-LINE; PLASTIC (SOT38Z)



⊕ Positional accuracy.

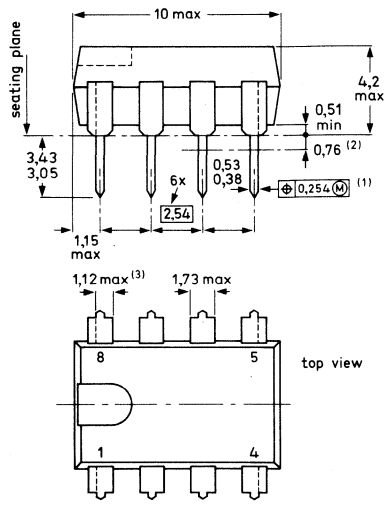
Ⓜ Maximum Material Condition.

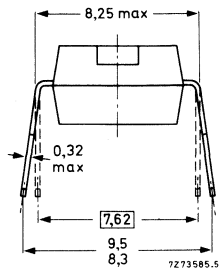
(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

Dimensions in mm

8-LEAD DUAL IN-LINE; PLASTIC (SOT97)





⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

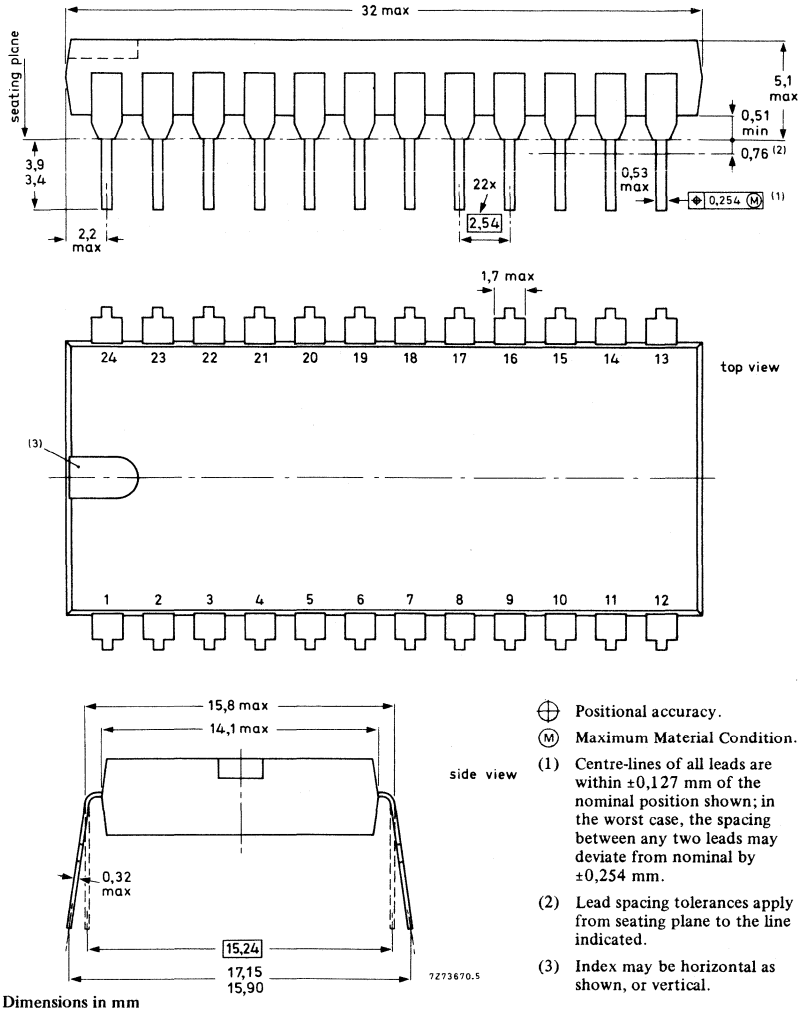
(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

(3) Only for devices with asymmetrical end-leads.

Dimensions in mm

24-LEAD DUAL IN-LINE; PLASTIC (SOT101A, B, F, G, L)



Dimensions in mm

⊕ Positional accuracy.

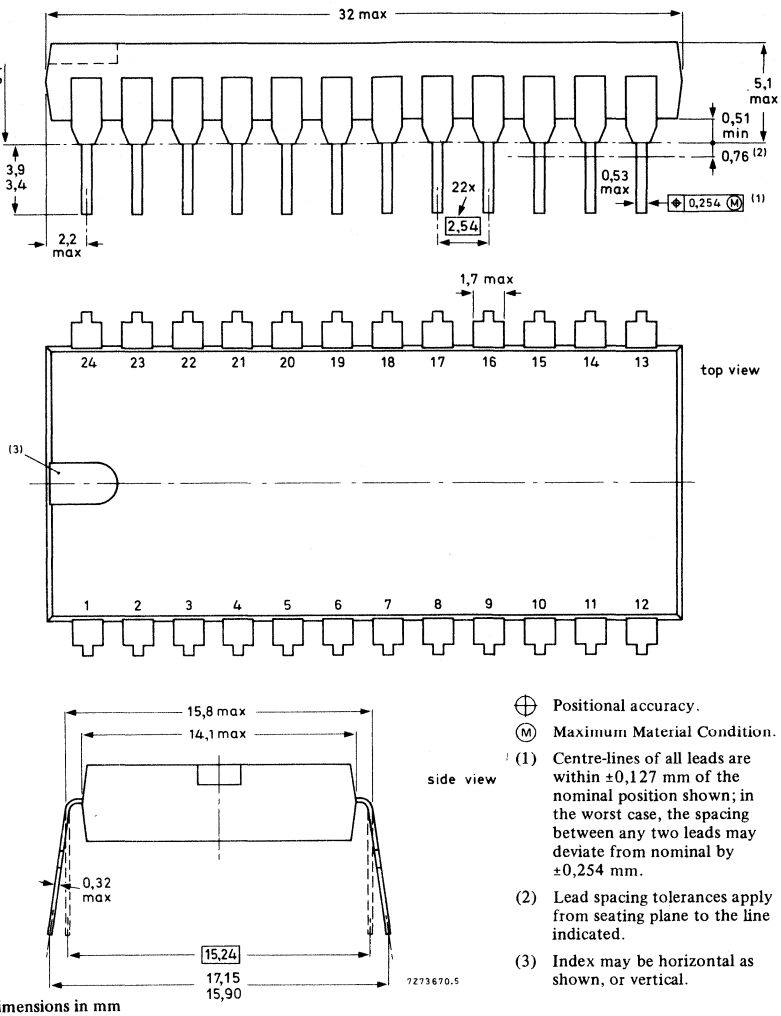
Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

(3) Index may be horizontal as shown, or vertical.

24-LEAD DUAL IN-LINE; PLASTIC WITH INTERNAL HEAT SPREADER (SOT101A, B, F, G, L)



⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

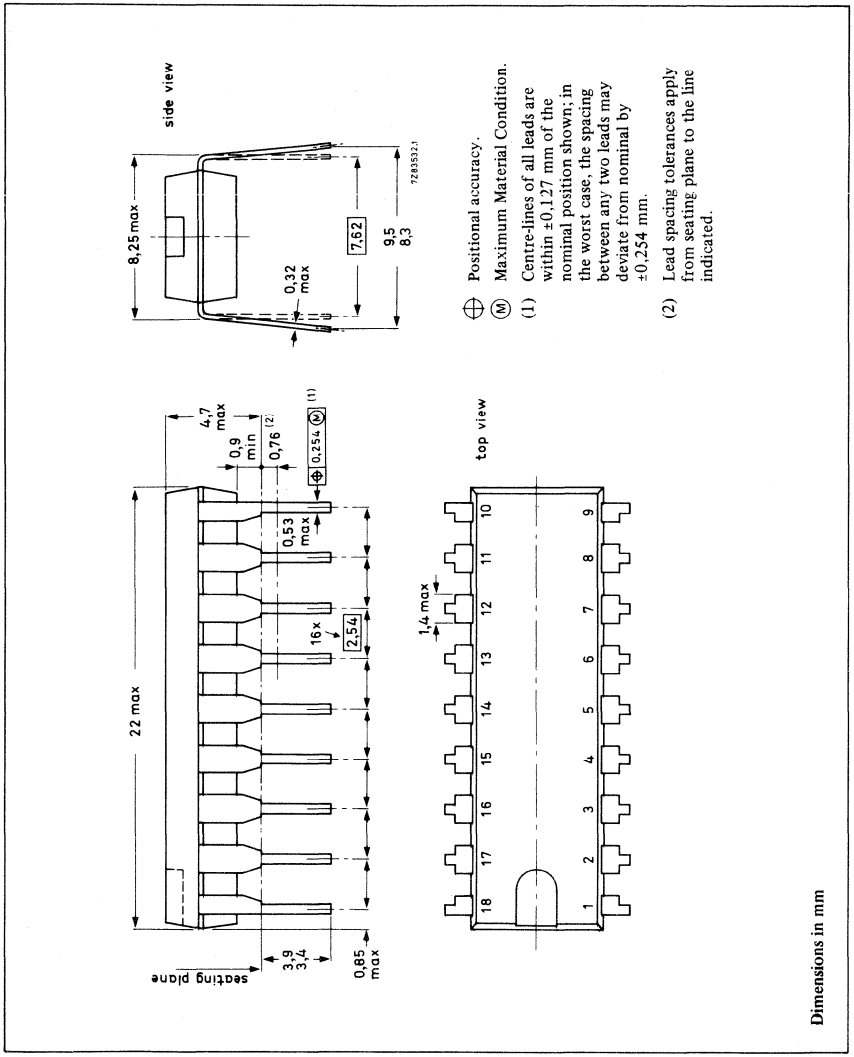
(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

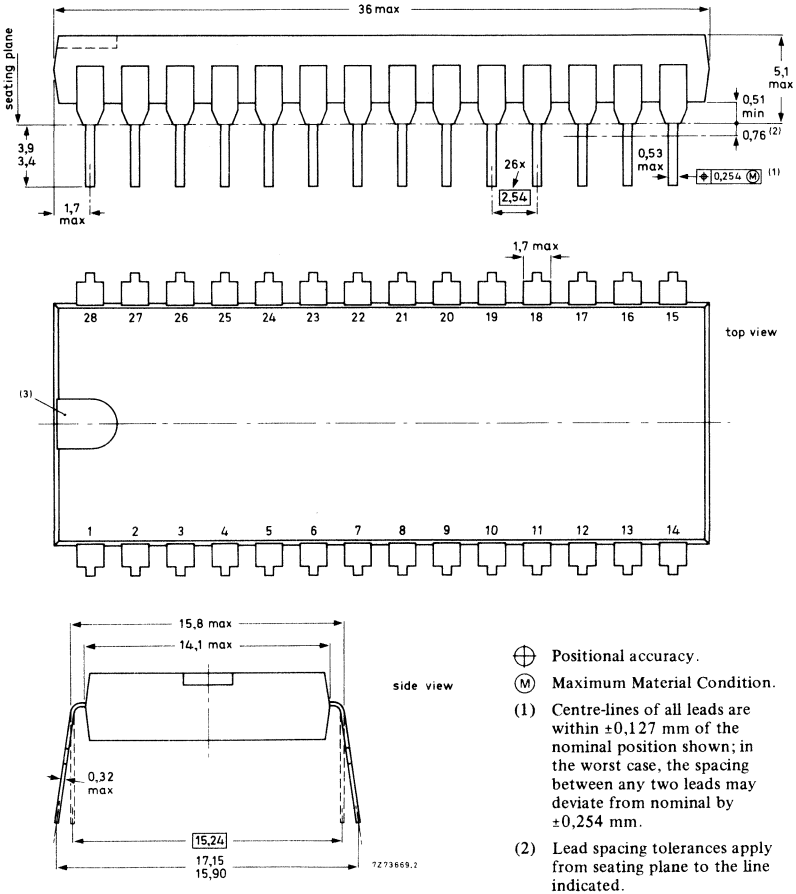
(3) Index may be horizontal as shown, or vertical.

Dimensions in mm

18-LEAD DUAL IN-LINE; PLASTIC (SOT102H, K, M, PG, RE)



28-LEAD DUAL IN-LINE; PLASTIC (SOT117)



⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

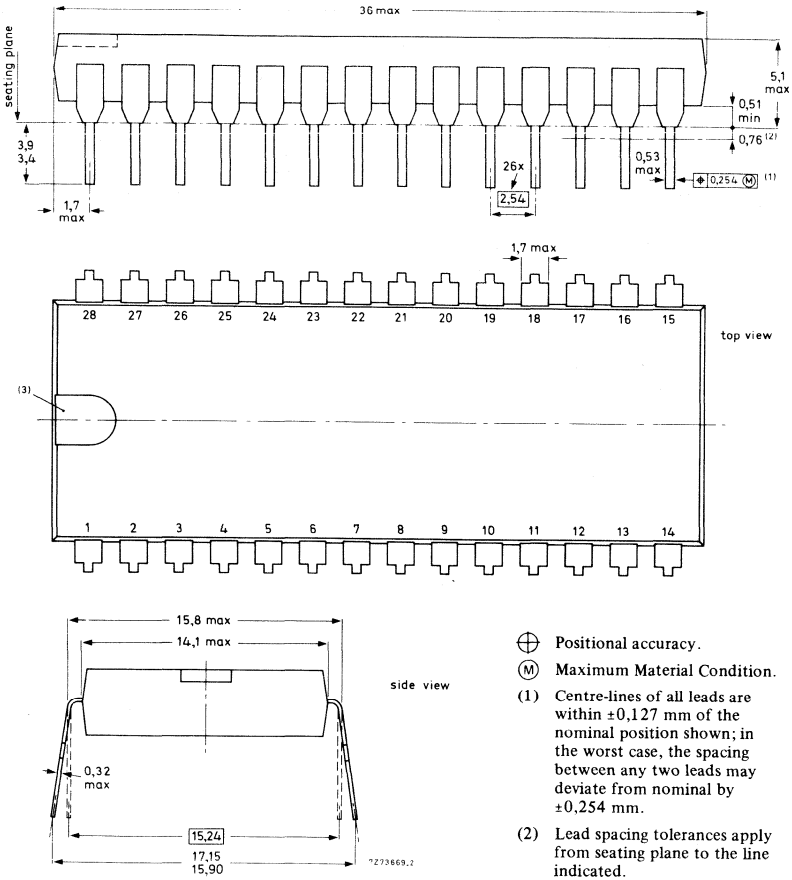
(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

(3) Index may be horizontal as shown, or vertical.

Dimensions in mm

28-LEAD DUAL IN-LINE; PLASTIC WITH INTERNAL HEAT SPREADER (SOT117)



⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

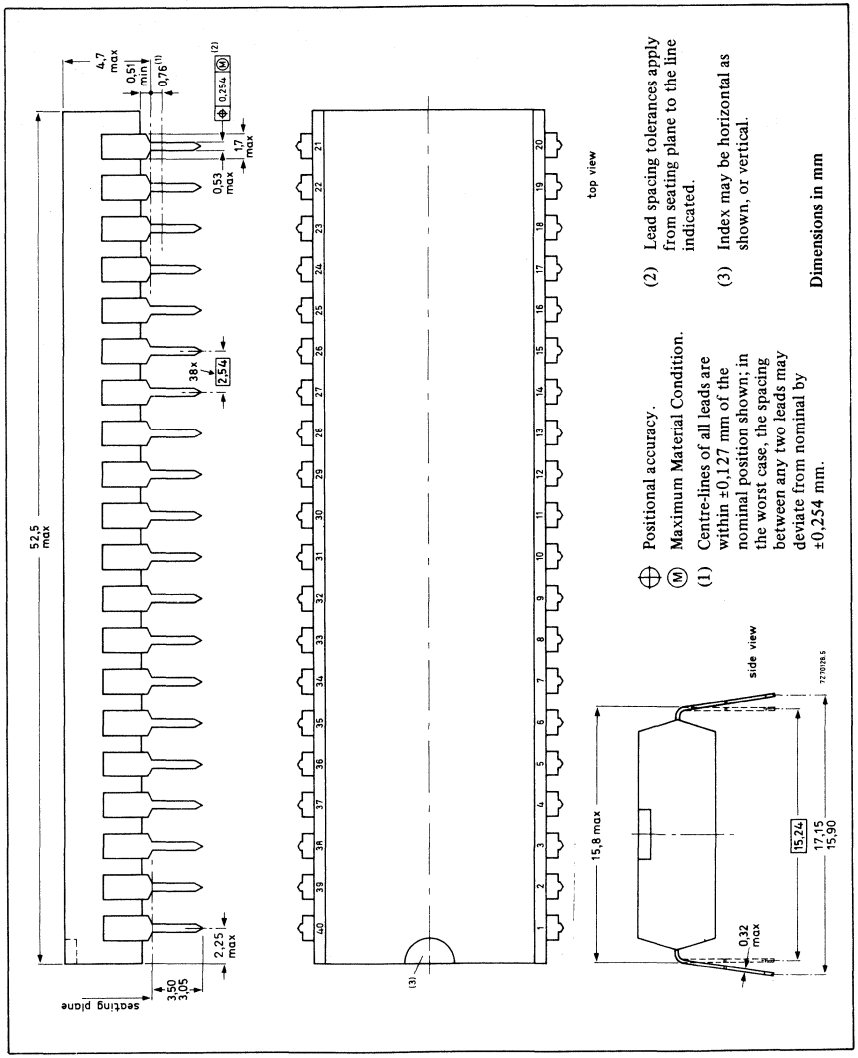
(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

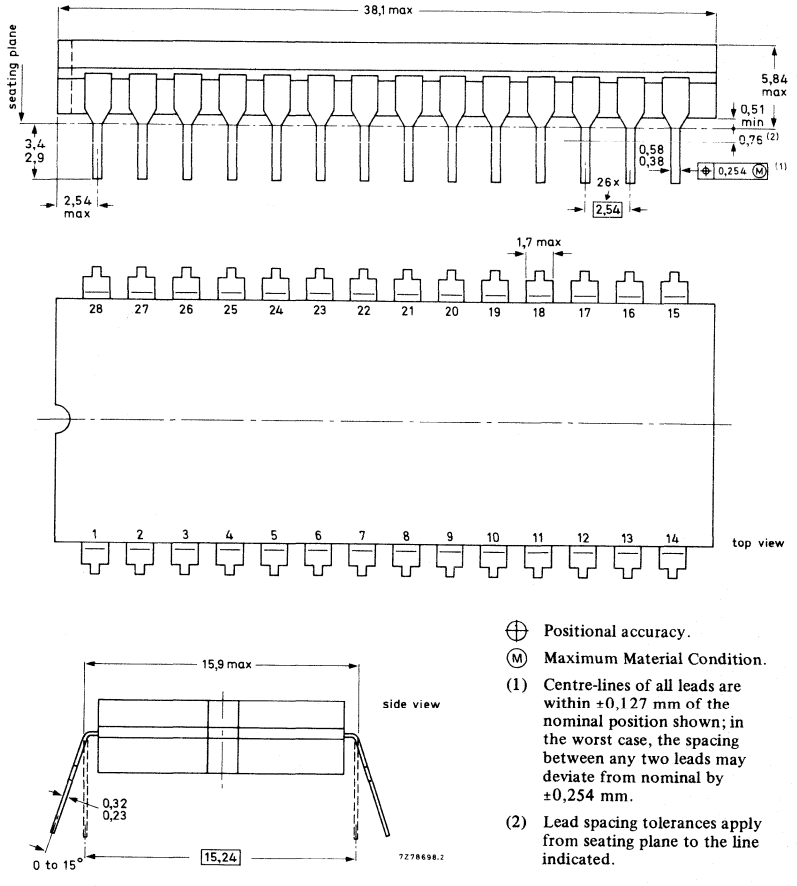
(3) Index may be horizontal as shown, or vertical.

Dimensions in mm

40-LEAD DUAL IN-LINE; PLASTIC (SOT129)



28-LEAD DUAL IN-LINE; CERAMIC (CERDIP) (SOT135A)



⊕ Positional accuracy.

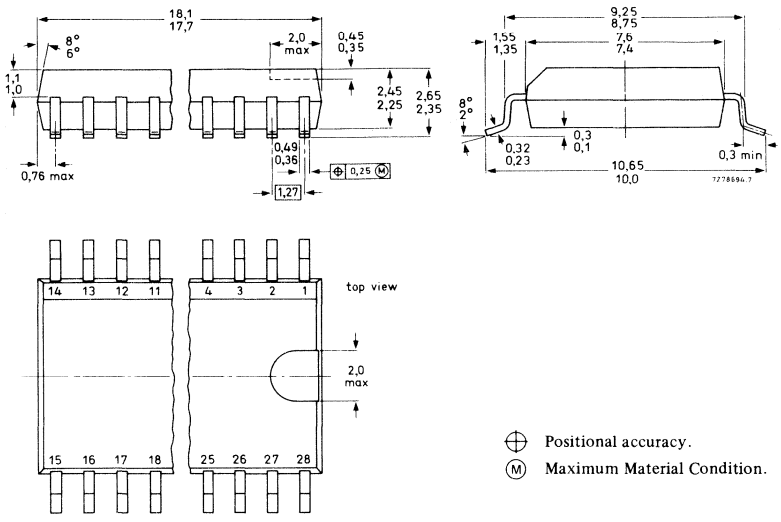
Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

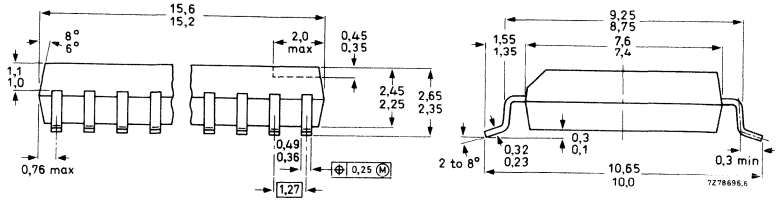
Dimensions in mm

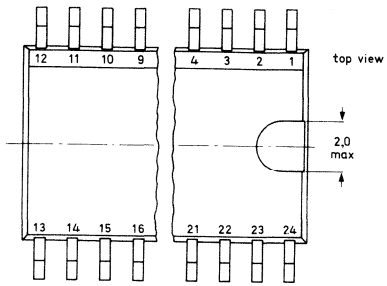
28-LEAD MINI-PACK; PLASTIC (SO28; SOT136A)



Dimensions in mm

24-LEAD MINI-PACK; PLASTIC (SO24; SOT137A)

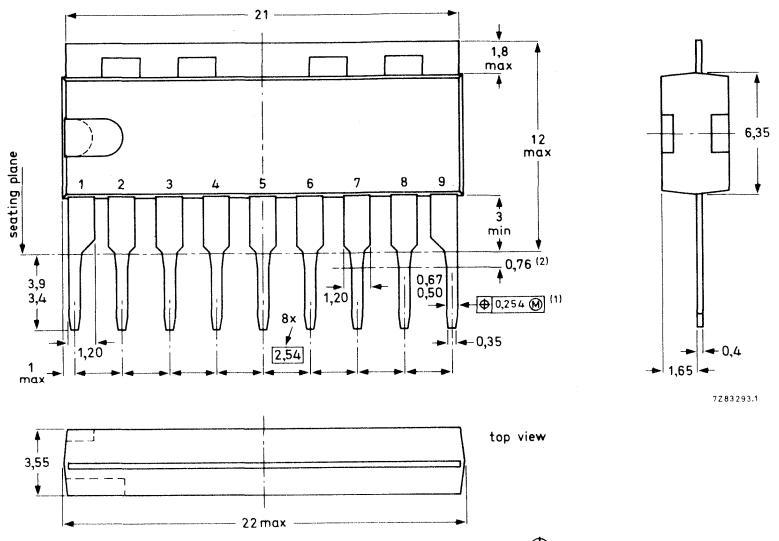




⊕ Positional accuracy.
Ⓜ Maximum Material Condition.

Dimensions in mm

9-LEAD SINGLE IN-LINE; PLASTIC (SOT142)



⊕ Positional accuracy.

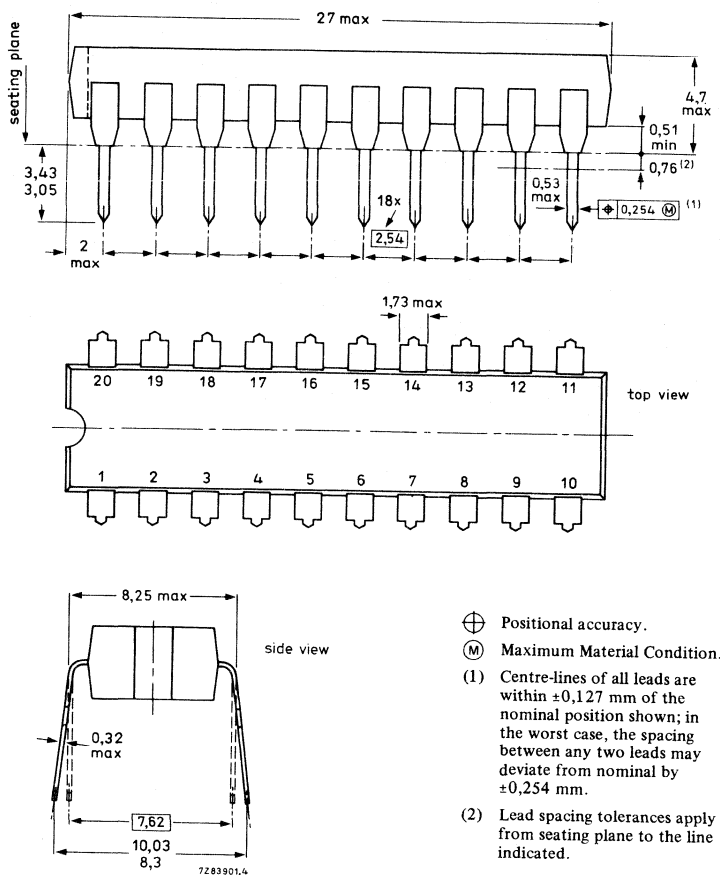
Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

Dimensions in mm

20-LEAD DUAL IN-LINE; PLASTIC (SOT146)



⊕ Positional accuracy.

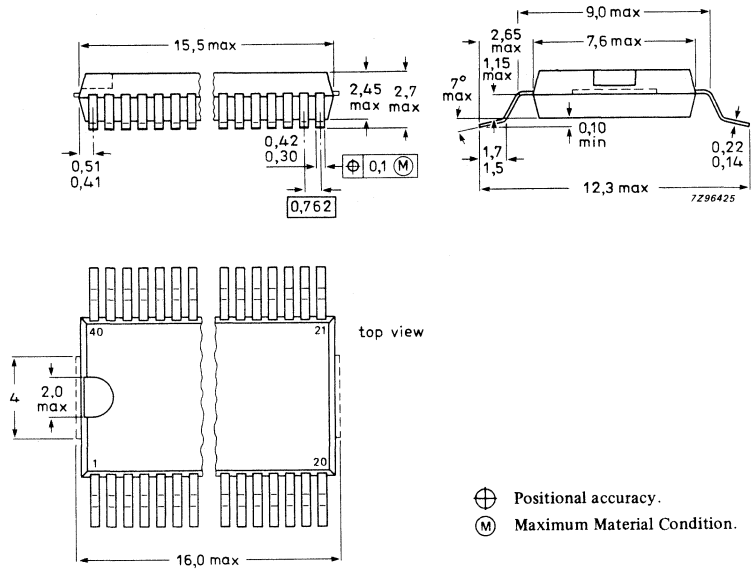
Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

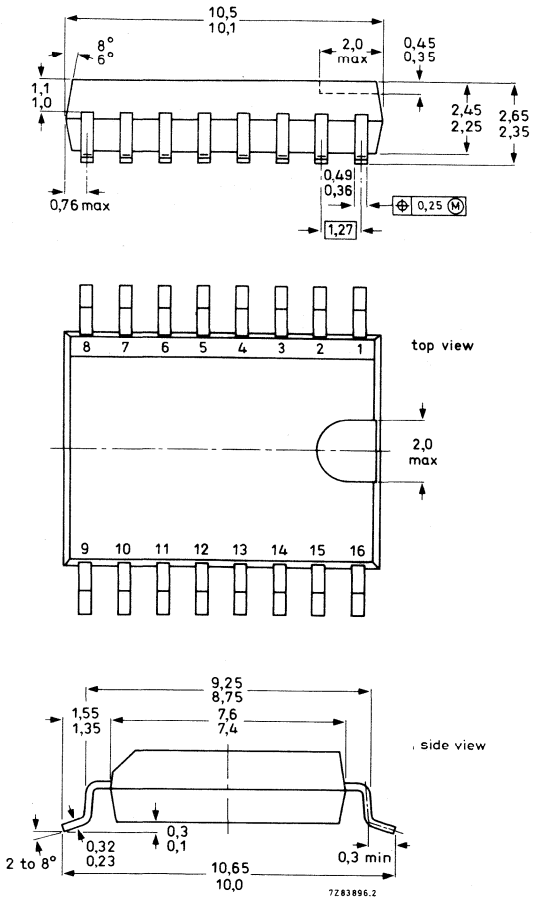
Dimensions in mm

40-LEAD MINI-PACK; PLASTIC (VSO40; SOT158A)



Dimensions in mm

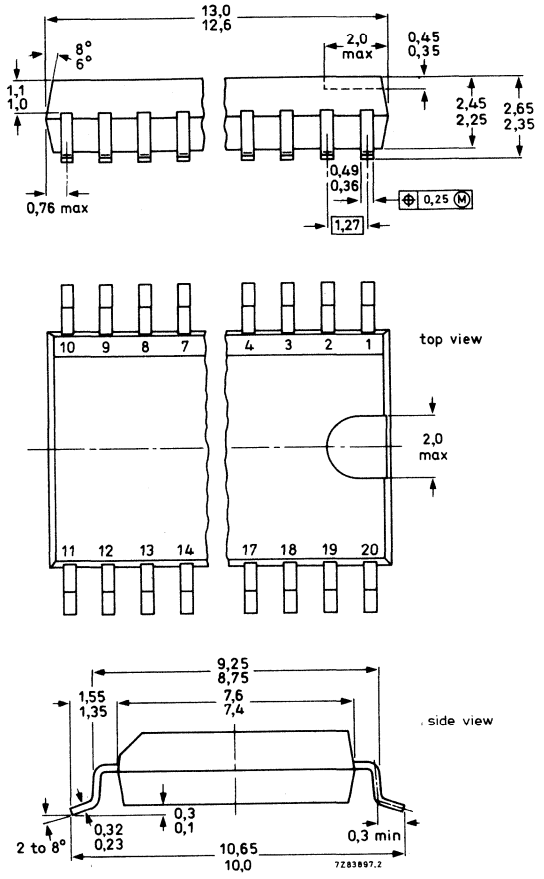
16-LEAD MINI-PACK; PLASTIC (SO16L; SOT162A)



Dimensions in mm

⊕ Positional accuracy.
Ⓜ Maximum Material Condition.

20-LEAD MINI-PACK; PLASTIC (SO20; SOT163A)

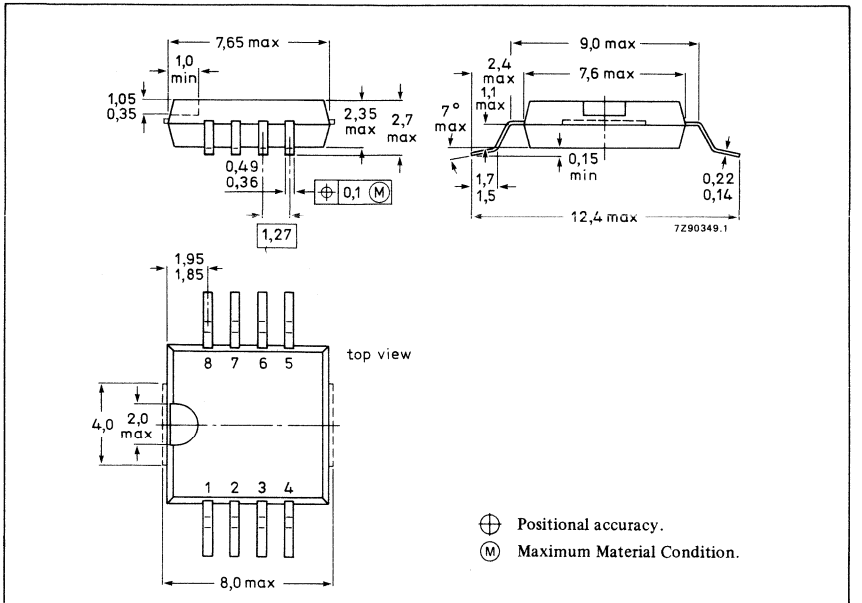


⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

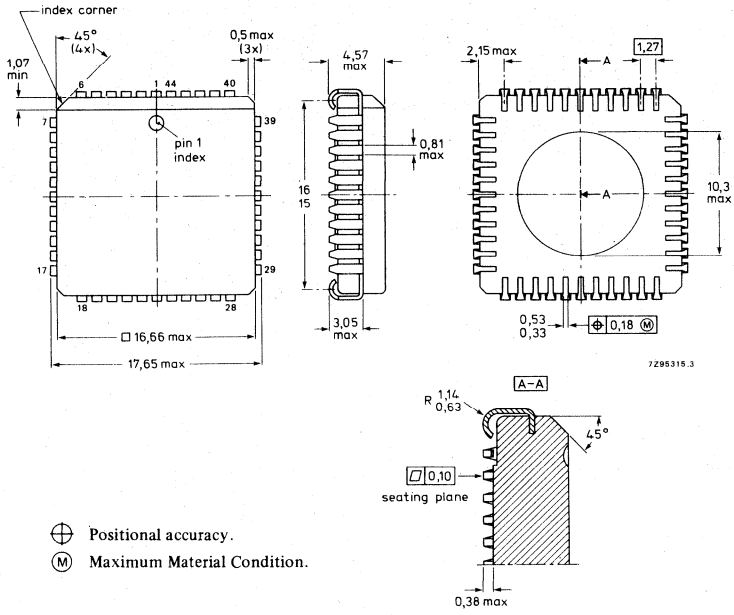
Dimensions in mm

8-LEAD MINI-PACK; PLASTIC (SO8L; SOT176)



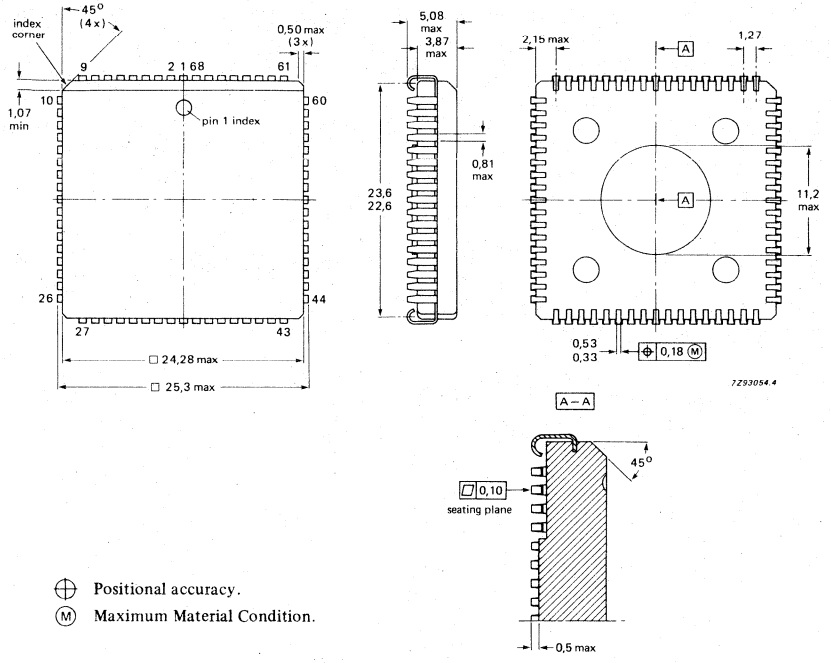
Dimensions in mm

44-LEAD PLASTIC LEADED CHIP CARRIER (PLCC) (SOT187)



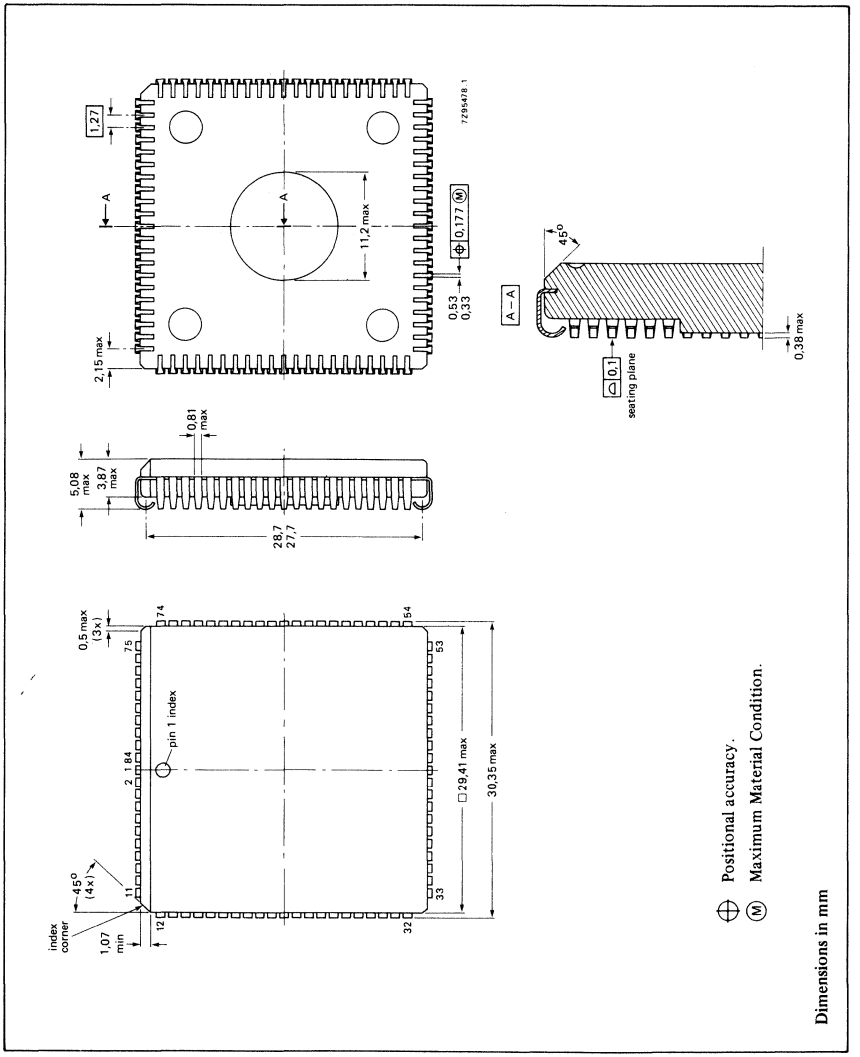
Dimensions in mm

68-LEAD PLASTIC LEADED CHIP CARRIER (PLCC) (SOT188)

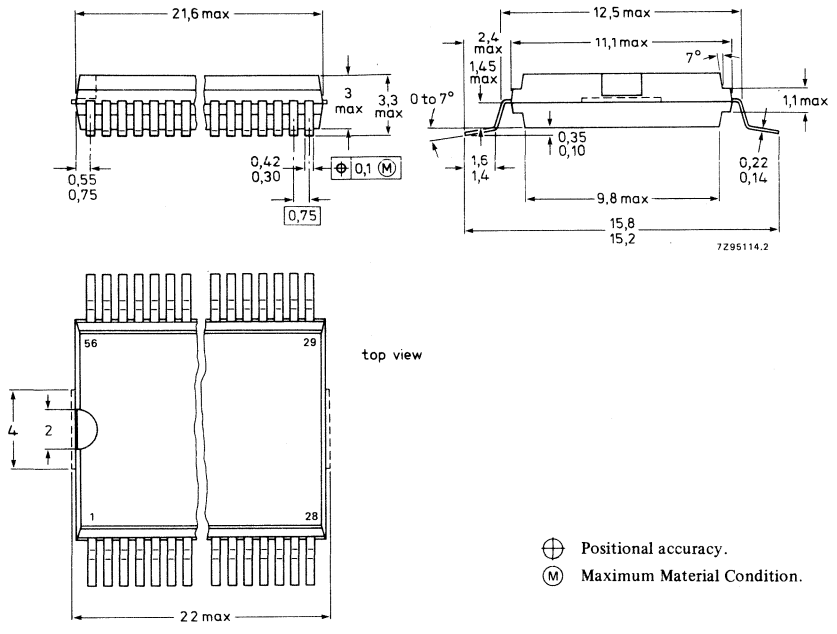


Dimensions in mm

84-LEAD PLASTIC LEADED CHIP CARRIER (PLCC) (SOT189)



56-LEAD MINI-PACK; PLASTIC (VSO56; SOT190)



SOLDERING PLASTIC MINI-PACKS

1. By hand-held soldering iron or pulse-heated solder tool

Fix the component by first soldering two, diagonally opposite end leads. Apply the heating tool to the flat part of the lead only. Contact time must be limited to 10 seconds at up to 300 °C. When using proper tools, all other leads can be soldered in one operation within 2 to 5 seconds at between 270 and 320 °C. (Pulse-heated soldering is not recommended for SO packages).

For pulse-heated solder tool (resistance) soldering of VSO packages, solder is applied to substrate by dipping or by an extra thick tin/lead plating before package placement.

2. By wave

During placement and before soldering, the component must be fixed with a droplet of adhesive. After curing the adhesive, the component can be soldered. The adhesive can be applied by screen printing, pin transfer or syringe dispensing.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder bath is 10 seconds, if allowed to cool to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

3. By solder paste reflow

Reflow soldering requires the solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the substrate by screen printing, stencilling or pressure-syringe dispensing before device placement.

Several techniques exist for reflowing, for example, thermal conduction by heated belt, infrared, and vapour-phase reflow. Dwell times vary between 50 and 300 seconds according to method. Typical reflow temperatures range from 215 to 250 °C.

Pre-heating is necessary to dry paste and evaporate binding agent.

Pre-heating duration: 45 minutes at 45 °C.

4. Repairing soldered joints

The same precaution and limits apply as in (1) above.

SOLDERING PLASTIC DUAL IN-LINE PACKAGES

1. By hand

Apply the soldering iron below the seating plane (or not more than 2 mm above it). If its temperature is below 300 °C it must not be in contact for more than 10 seconds; if between 300 and 400 °C, for not more than 5 seconds.

2. By dip or wave

The maximum permissible temperature of the solder is 260 °C; this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified storage maximum. If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

3. Repairing soldered joints

The same precautions and limits apply as in (1) above.

NOTES

DATA HANDBOOK SYSTEM

DATA HANDBOOK SYSTEM

Our Data Handbook System comprises more than 60 books with specifications on electronic components, subassemblies and materials. It is made up of four series of handbooks:

ELECTRON TUBES	BLUE
SEMICONDUCTORS	RED
INTEGRATED CIRCUITS	PURPLE
COMPONENTS AND MATERIALS	GREEN

The contents of each series are listed on pages iv to vii.

The data handbooks contain all pertinent data available at the time of publication, and each is revised and reissued periodically.

When ratings or specifications differ from those published in the preceding edition they are indicated with arrows in the page margin. Where application information is given it is advisory and does not form part of the product specification.

Condensed data on the preferred products of Philips Electronic Components and Materials Division is given in our Preferred Type Range catalogue (issued annually).

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Product specialists are at your service and enquiries will be answered promptly.

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T1 **Tubes for r.f. heating**

T2a **Transmitting tubes for communications, glass types**

T2b **Transmitting tubes for communications, ceramic types**

T3 **Klystrons**

T4 **Magnetrons for microwave heating**

T5 **Cathode-ray tubes**
Instrument tubes, monitor and display tubes, C.R. tubes for special applications

T6 **Geiger-Müller tubes**

T8 **Colour display systems**
Colour TV picture tubes, colour data graphic display tube assemblies, deflection units

T9 **Photo and electron multipliers**

T10 **Plumbicon camera tubes and accessories**

T11 **Microwave semiconductors and components**

T12 **Vidicon and Newvicon camera tubes**

T13 **Image intensifiers and infrared detectors**

T15 **Dry reed switches**

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Small-signal silicon diodes, voltage regulator diodes (< 1,5 W), voltage reference diodes, tuner diodes, rectifier diodes

S2a **Power diodes**

S2b **Thyristors and triacs**

S3 **Small-signal transistors**

S4a **Low-frequency power transistors and hybrid modules**

S4b **High-voltage and switching power transistors**

S5 **Field-effect transistors**

S6 **R.F. power transistors and modules**

S7 **Surface mounted semiconductors**

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S11 **Microwave transistors**

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S13 **Semiconductor sensors**

S14 **Liquid Crystal Displays**

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C6	Synchronous motors and gearboxes
C7	Variable capacitors
C8	Variable mains transformers
C9	Piezoelectric quartz devices
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C12	Potentiometers, encoders and switches
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